ND3060

A Multi-Format Card Reader/Writer Controller with USB Interface Specification

Neodio Technologies Corporation

14F-1, No.176, Chien-Yi Rd., Chung-Ho,
Taipei Hsien, 235, Taiwan, R.O.C.
TEL: 886-2-8227-1525
FAX: 886-2-8227-1530
E-Mail: sales@neodio.com.tw

Introduction

The ND3060 is a complete integrated system LSI, providing the supports of multi-format FLASH devices, as well as the implementations of USB interface. It will enable the most advanced design flexibility on such applications as multi-format FLASH card reader, USB/IDE interface adapter, and so on.

Features

- Standard 8051 instruction compatible CPU core
- 4-cycle instruction with 2.5X performance improvement
- 10 vectors interrupt structure
- 2 sets of data pointers (DPTR) to speed up the transfer of large amount data
- Built-in Watch-dog timer
- 12Mbps Full-speed USB interface complies with ver. 1.1 standard
- Implementations of USB control and bulk transfers
- USB bus power capability
- Internal PLL function provides 48MHz frequency for USB operation
- 512-byte x 2 buffer control unit with hardwired Error Correction Code (ECC) function
- High-performance, time-interleaving Direct Channel Access (DCA) for data exchange
- Software configurable I^2C/SPI Bus interface for flexible peripheral circuit control
- FLASH interfaces supporting built-in/external connected FLASH device, such as NAND-type Flash Memory, Smart Media Card/Compact Flash Card/IBM Micro Driver/Multimedia Card/SD Memory Card/Memory Stick Card/Memory Stick PRO Card and xD-Picture Card.
- Fully independent FLASH interfaces allowing insertion of one type of card while accessing the others without extra TTL logic
- Advanced clock management scheme to save the overall power consumption, e.g. USB suspend mode
- Extra 16-bit general-purpose I/O pins improve the flexibility of system design, i.e. port4, and port5
- 128-pin (14x20mm) LQFP package
- 3.3V low power operating voltage

Block Diagram

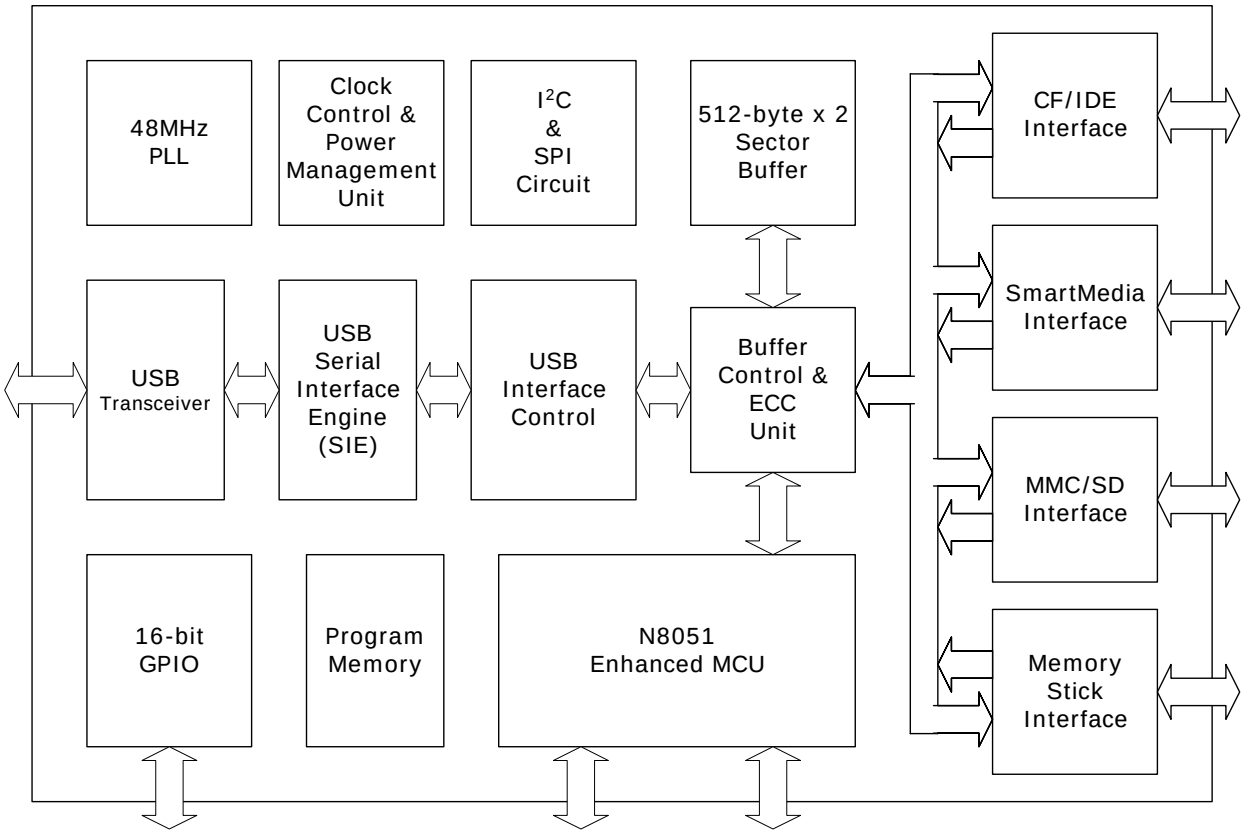


Figure 1: ND3060 block diagram

Pin Descriptions

Pin No.	Name	I/O	Descriptions
105	EA_N	I	External access enable. It will enable the N8051 to fetch code from external program memory if this pin is held low externally.
103	PSEN_N	O	Program strobe enable. PSEN_N is the read strobe signal to external program memory.
104	ALE	O	Address latch enable. ALE of N8051outputs pulse for latching the low byte of the address during an access to external memory.
19	RSTI_N	I	Reset input. A low on this pin for two machine cycles while the oscillator is running that resets the device.(1,2)
68	RSTO_N	O	Reset output. This signal is used to reset externally connected hardware. It is an active-low signal.
16	XTAL1	I	Crystal 1 (12MHz). Input to the inverting oscillator amplifier.
17	XTAL2	O	Crystal 2 (12MHz). Output from the inverting oscillator amplifier.
27,28,29,30, 35,36,37,38	P0.0~P0.7	I/O	Port0. Port 0 is an 8-bit open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory. (2)
24,25,106,107 58,67,7,8	P1.0~P1.7	I/O	Port1. Port 1 is an 8-bit bi-directional I/O port with internal 75K pull-ups. They are the general-purpose I/O pins.(2)
50,51,52,53, 54,55,56,57	P2.0~P2.7	I/O	Port2. Port 2 is an 8-bit bi-directional I/O port with internal 75K pull-ups. This port also provides the upper address bits for accesses to external memory.(2)
39,126,32,14, 20,21,22,23	P3.0~P3.7	I/O	Port3. Port 3 is an 8-bit bi-directional I/O port with internal 75K pull-ups. All bits have alternate functions are described below: (2) RxD(P3.0) : Serial Port 0 input TxD(P3.1) : Serial Port 0 output INT0_N (P3.2) : External Interrupt 0 INT1_N(P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input WR_N(P3.6) : External Data Memory Write Strobe RD_N(P3.7) : External Data Memory Read Strobe
9,12,13,40, 114,115,127, 128	P4.0~P4.7	I/O	Port4. Port 4 is an 8-bit bi-directional I/O port. The higher 2 bits are implemented the same with Port 1. The lower 6 bits are implemented as the I^2C and SPI interfaces respectively, which are described below.(2) SCL(P4.5) : I^2C bus serial clock output SDA(P4.4) : I^2C bus serial data input/output (open-drain) SS_N(P4.3) : SPI slave select input SCK(P4.2) : SPI master clock output/slave clock input MOSI(P4.1) : SPI master data output/slave data input MISO(P4.0) : SPI master data input/slave data output SS_N, MOSI, MISO 3 pins are implemented with internal pull-ups. When used in the I^2C-related applications, SCL and SDA must be connected with external 4.7K pull-ups. And when used in the

			SPI-related applications, SCK has to be set to push-pull mode (by clear P4WOR register). In the other cases, it is recommended to connect these 3 pins, SCL, SDA, and SCK, to external 75K pull-ups to avoid the signal floating.
93,94,95,96, 97,98,99,100	P5.0~P5.7	I/O	Port5: Port 5 is an 8-bit bi-directional I/O port with internal 75K pull-ups. This port also provides the lower address bits for accesses to external memory.(2)
47	IOR_N	O	CompactFlash/IDE I/O read signal.
80	IOW_N	O	CompactFlash/IDE I/O write signal.
44,45,46	A0~A2	O	CompactFlash/IDE address bus. These bits are asserted to access a register or data port in the CompactFlash/IDE device.
81,82,83,84, 85,86,87,88, 116,117,118, 119,120,122, 123,124	FD0~FD15	I/O	CompactFlash/IDE data bus with internal 75K pull-downs.(2)
41	SALE	O	NAND-type Flash/SmartMedia address latch enable.
42	SCLE	O	NAND-type Flash/SmartMedia command latch enable.
43	SRE_N	O	NAND-type Flash/SmartMedia read enable.
71	SWE_N	O	NAND-type Flash/SmartMedia write enable.
72,73,74,75, 76,77,78,79	SD0~SD7	I/O	NAND-type Flash/SmartMedia data I/O bus with internal 75K pull-downs.(2)
108	MCLK	O	MMC/SD host to card clock signal.
113	MCMD	I/O	MMC/SD command/response signal.(2)
109,110,111, 112	MD0~MD3	I/O	MMC/SD data bus with internal 75K pull-ups.(2)
5	SCLK	O	Memory Stick serial protocol clock signal.
6	BS	O	Memory Stick serial protocol bus state signal.
4	SDIO	I/O	Memory Stick serial data signal with internal 75K pull-down.(2)
63	DP	A	USB D+ data line.
62	DM	A	USB D- data line.
1,2,33,34,61, 89,90,	VCCD	P	Digial Power Supply.
15	VCCA	P	Analog Power Supply.
10,11,26,31, 49,59,60,64, 91,92,101,121	GNDD	P	Digital Ground.
18	GNDA	P	Analog Ground.
70	TEST	I	Test input pin. These pins are used only in the IC test mode, and should be connected to GND when in normal mode.

I: digital input; O: digital output with 2mA drive; I/O: digital bi-direction with 2mA drive; A: analog signal; P: power/ground

Note (1) Schmitt triggered input buffer

Note (2) 5V tolerant input(bi-directional) buffer

Pin Assignment

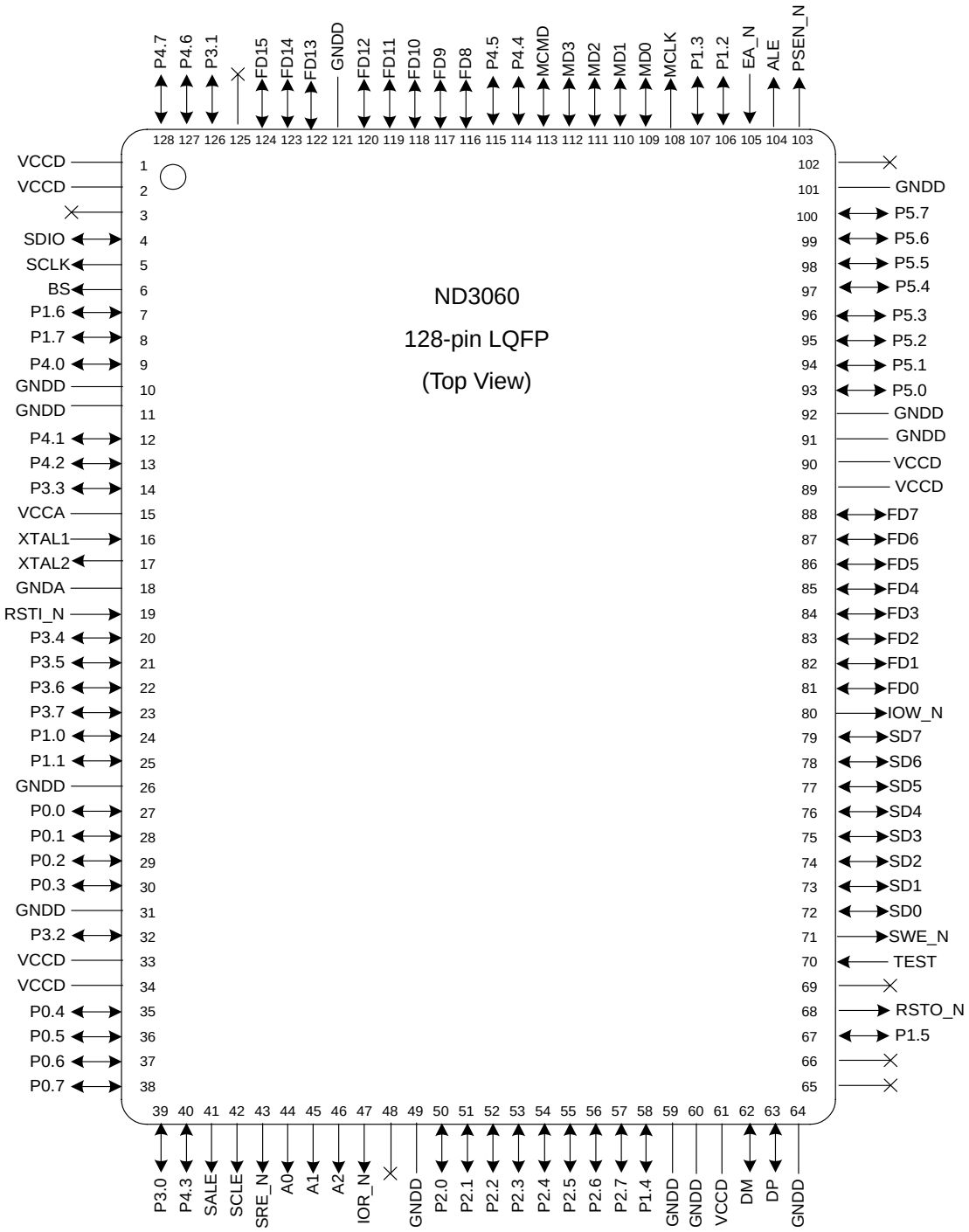


Figure 2: ND3060 pin assignment

Instruction Set Summary

Legends:

A - Accumulator

Rn - Register R7-R0

direct - Internal Register address

@Ri - Internal Register pointed-to by R0 or R1 (except MOVX)

rel - 2's complement offset byte

bit - direct bit-address

#data - 8-bit constant

#data 16 - 16-bit constant

addr 16 - 16-bit destination address

addr 11 - 11-bit destination address

Instruction	Byte	N8051 Cycles	Std. 8051 Cycles	Instruction	Byte	N8051 Cycles	Std. 8051 Cycles
Arithmatic Instructions							
ADD A, Rn	1	4	12	INC A	1	4	12
ADD A, direct	2	8	12	INC Rn	1	4	12
ADD A, @Ri	1	4	12	INC direct	2	8	12
ADD A, #data	2	8	12	INC @Ri	1	4	12
ADDC A, Rn	1	4	12	INC DPTR	1	8	12
ADDC A, direct	2	8	12	DEC A	1	4	12
ADDC A, @Ri	1	4	12	DEC Rn	1	4	12
ADDC A, #data	2	8	12	DEC direct	2	8	12
SUBB A, Rn	1	4	12	DEC @Ri	1	4	12
SUBB A, direct	2	8	12	MUL AB	1	12	48
SUBB A, @Ri	1	4	12	DIV AB	1	12	48
SUBB A, #data	2	8	12	DA A	1	4	12
Logical Instructions							
ANL A, Rn	1	4	12	XRL A, Rn	1	4	12
ANL A, direct	2	8	12	XRL A, direct	2	8	12
ANL A, @Ri	1	4	12	XRL A, @Ri	1	4	12
ANL A, #data	2	8	12	XRL A, #data	2	8	12
ANL direct, A	2	8	12	XRL direct, A	2	8	12
ANL direct, #data	3	12	24	XRL direct, #data	3	12	24
ORL A, Rn	1	4	12	CLR A	1	4	12
ORL A, direct	2	8	12	CPL A	1	4	12
ORL A, @Ri	1	4	12	RL A	1	4	12
ORL A, #data	2	8	12	RLC A	1	4	12
ORL direct, A	2	8	12	RR A	1	4	12
ORL direct, #data	3	12	24	RRC A	1	4	12

Electrical Specification:

Absolute Maximum Rating

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	DC supply voltage	-0.3	3.6	V
V_{IN}	DC input voltage	-0.3	V_{CC}+0.3	V
V_{OUT}	DC output voltage	-0.3	V_{CC}+0.3	V
T_{STG}	Storage temperature range	-55	150	^{o}C

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	3.0	3.3	3.6	V
V_{IN}	DC input voltage	0.0		V_{CC}	V
Tj	Commercial junction operating temperature	0	25	115	^{o}C

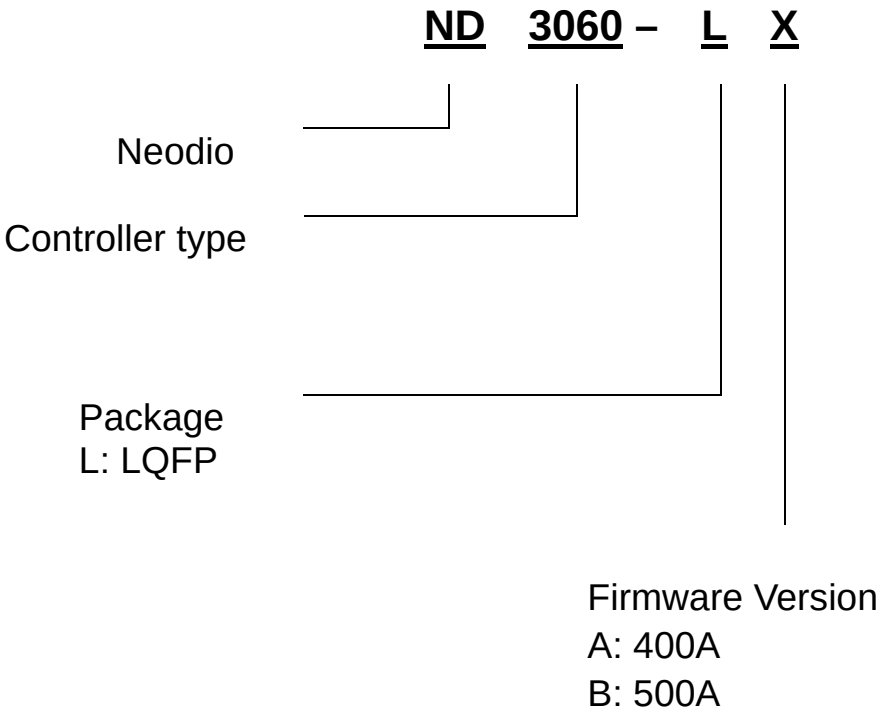
DC Characteristics

(Measured under the recommended operation conditions V_{CC}=3.0V~3.6V, Tj=0 ^{o}C ~115 ^{o}C)

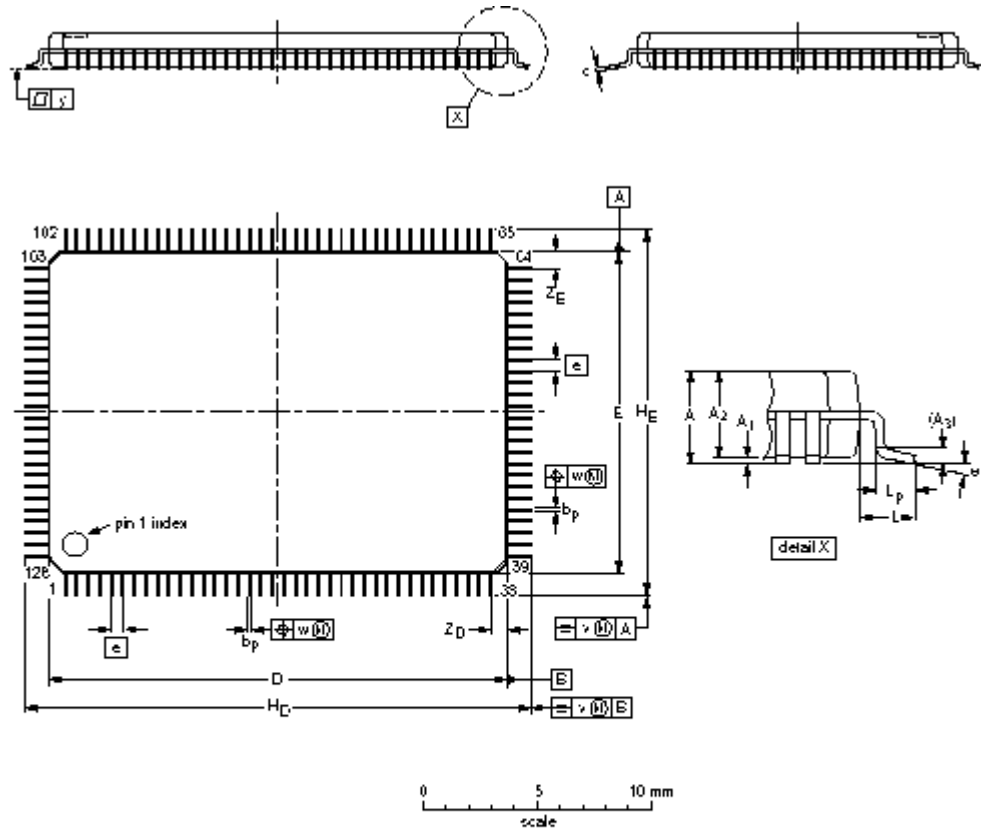
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{IL}	Input leakage current	w/o pull-up/down	-1.0		1.0	uA
I_{OZ}	Tri-state leakage current		-1.0		1.0	uA
C_{IN}	Input capacitance			3.3		pF
C_{OUT}	Output capacitance		3.2		5.4	pF
C_{BID}	Bi-direction buffer capacitance		3.2		5.4	pF
V_{IL}	Input low voltage				0.3*V_{CC}	V
V_{IH}	Input high voltage		0.7*V_{CC}			V
V_{t-}	Schmitt trigger negative going threshold voltage			1.2		V
V_{t+}	Schmitt trigger positive going threshold voltage			2.1		V
V_{OL}	Output low voltage	I_{OL}=2mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=2mA	2.4			V
R_I	Input pull-up/down resistance	V_{IL}=0V or V_{IH}=V_{CC}		75		KOhm
I_{OP}	Operating current	(1)		TBD		mA
I_{PWD}	Power down current	V_{IH}=V_{CC} V_{IL}=0.0V(1)		TBD		uA

Note (1) Measured within the assembled application circuits operating in internal 12MHz frequency, including EPROM, SRAM, Bus Transceiver etc.

Ordering Information



Package Information



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1.0	0.75 0.45	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7° 0°

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.