PIM-TB10-Z

10MHz Mainboard
User Manual

PIM-TB10-Z

10MHz Mainboard
User Manual

Edition 1.02

Checklist

Your PIM-TB10-Z package contains the following:

- One PIM-TB10-Z mainboard
- One PIM-TB10-Z user manual

The following does not apply to any country where such provisions are inconsistent with local law:

Datatech makes no warranties with respect to this documentation either express or implied and provides it "as is". This includes but is not limited to any implied warranties of merchantability and fitness for a particular purpose. The information in this document is subject to change without notice. **Datatech** assumes no responsibility for any errors that may appear in this document.

IBM, IBM PC and PC/XT are registered trademarks of International Business Machines Corporation. The typeface used in the text of this manual is 12 point Helvetica and is used under licence from the Allied Corporation, the owner of the typeface.

Contents

Introduction

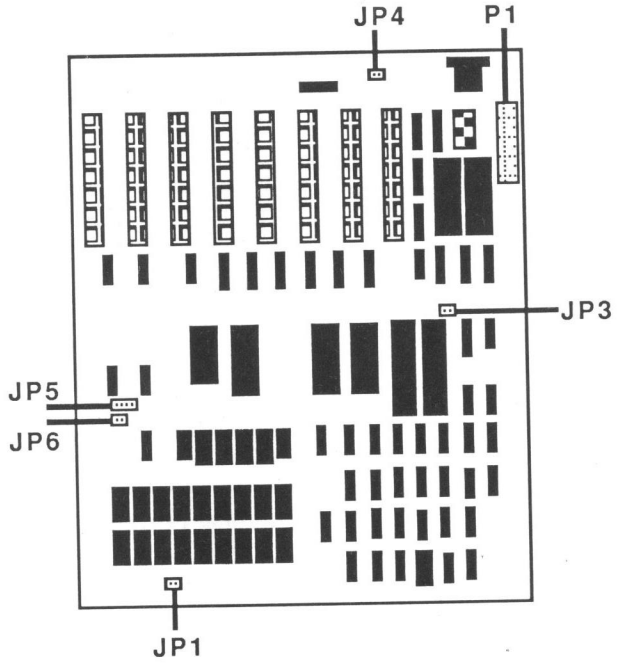
You can rest assured of having made a wise choice in buying the PIM-TB10-Z motherboard for your personal computer. This motherboard is not only compatible with the PC/XT but provides you with these features:

- 16-bit 8088-10 CPU or qualified 8088-2 CPU (optional 8087-1 coprocessor).
- Switchable processing speed in 10MHz (110% faster than normal — 4.77MHz) and 4.77MHz.
- Turbo/Normal modes selectable by either a software switch or a hardware switch.
- Memory expandable to 640K on mainboard.
- ROM capacity — 8K BIOS.
- LEGAL BIOS from ERSO (Electronics Research & Organization).
- 8 expansion slots.
- 4-channel DMA for disk and special I/O.
- 3-channel timer for music and time.
- 8-level interrupt.
- IBM PC/XT® compatible.
- Operating systems : MS-DOS®, CPM/86®, CCP/M®.
- Speed test
  by Norton® Utility : 2.1
  by Landmark® Speed Test Program : 4.1

The clear, well-illustrated instructions in this manual ensure that even if you are a newcomer to the computer world, you will have your system installed and running with the minimum of effort.

Board layout

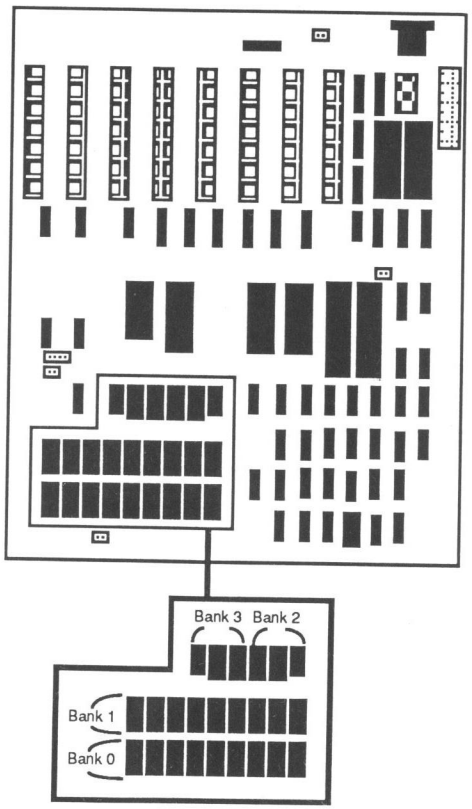
The illustration below will familiarize you with the layout of the PIM-TB10-Z motherboard and its onboard jumpers.



Installation

RAM installation

Four kinds of RAM size are possible with the PIM-TB10-Z motherboard. The figure below shows the location of the RAM banks. Remember that when inserting chips in their sockets, you must make sure that the notched end of the chip is lined up with the notched end of the socket.



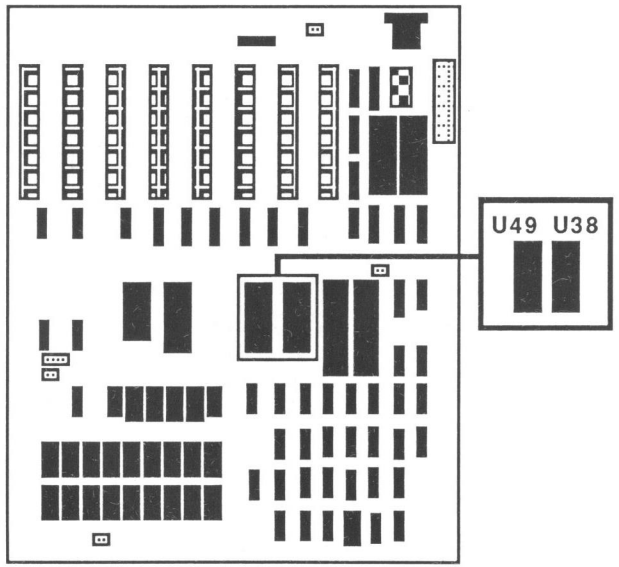
The following table allows you to configure the required RAM size:

	Bank 0	Bank 1	Bank 2	Bank 3
256K RAM	41256 x 9	No chips	No chips	No chips
512K RAM	41256 x 9	41256 x 9	No chips	No chips
576K RAM	41256 x 9	41256 x 9	4464 x 2 + 4164 x 1	No chips
640K RAM	41256 x 9	41256 x 9	4464 x 2 + 4164 x 1	4464 x 2 + 4164 x 1

Note that for the 576K RAM and the 640K RAM options, two different kinds of chips are used in banks 2 and 3. For 576K RAM, bank 2 will be filled with two 4464 chips in sockets U63 and U59, and one 4164 chip in socket U55. For 640K RAM, bank 2 will be filled with the same chips as were used for 576K RAM and bank 3 will be filled with two 4464 chips in sockets U72 and U67, and one 4164 chip in U76.

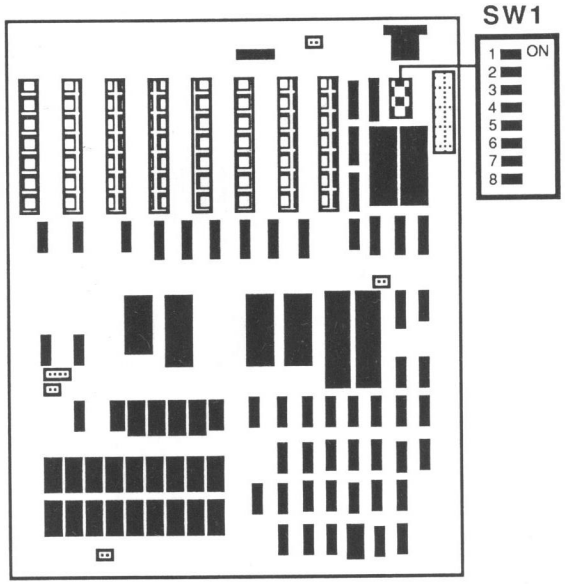
ROM installation

Two chips must be installed for the ROM of this system: a 2764 in socket U38 for the ROM BIOS and a 27256 chip in socket U49 for the ROM BASIC. Refer to the illustration below for the location of these two sockets.



DIP switch settings

DIP switch SW1 is used to set the system configuration. For the location of the switch and the settings, refer to the following illustrations:



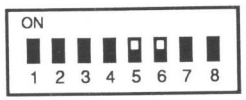
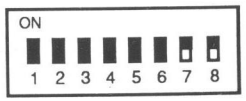
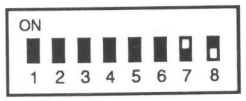
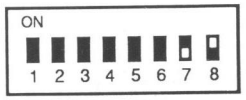
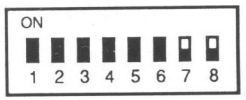
ON 1 2 3 4 5 6 7 8	normal operation
ON 1 2 3 4 5 6 7 8	operation without 8087 coprocessor
ON 1 2 3 4 5 6 7 8	operation with 8087 coprocessor
ON 1 2 3 4 5 6 7 8	for enhanced graphics adapter
ON 1 2 3 4 5 6 7 8	for color graphics adapter (40 x 20 mode)
ON 1 2 3 4 5 6 7 8	for color graphics adapter (80 x 25 mode)

NOTE:

indicates SW on

indicates SW off

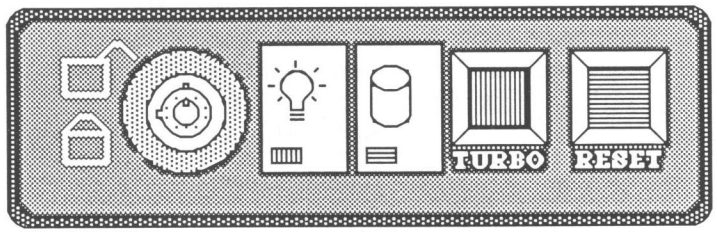
(Continued)

	for monochrome display adapter
	for one disk drive
	for two disk drives
	for three disk drives
	for four disk drives

Panel indicators and switches

How you attach the mainboard to the case of your system unit is fairly up to you. This is because the PIM-TB10-Z Turbo mainboard can be used in a variety of 80286-type system unit cases.

Under typical conditions, your system unit will have all the indicators and switches shown below and preferably even a reset switch, a Turbo hardware switch and a Turbo LED. If not, you can either install a new panel display or omit some of these items from your system. Your computer dealer offers an accessory which allows you to add the two switches and the LED to your system. An example of an "ideal" display panel for your computer is pictured below:



Functions of panel indicators and switches

The PIM-TB10-Z motherboard provides the following connectors for your control panel:

- **Keylock connector** The keylock connector is located at JP3 on the motherboard. By using a keylock device on your control panel to put the two pins at JP3 in a closed circuit, the keyboard is unlocked. When the two pins are in an open circuit, the keyboard is locked.

- **Reset connector** The reset connector is located at JP4 on the motherboard. If you connect a switch to these two pins, your computer will operate normally while the switch is open. Closing and again opening the switch will cause the system to reset. This is a useful function if you are stuck in the middle of an unfamiliar program and have no other means of escaping from it. Using the reset function will start the computer from the RAM test stage. Be warned, however, that any files which have not been saved will be lost once you press the reset button.

- **Power LED and Turbo LED** The power LED and Turbo LED connector is located at JP5 on the motherboard. The pinouts for the connector are as follows:

Pin	Assignment
1	+ Turbo LED
2	- Turbo LED
3	Power LED (+)
4	Ground

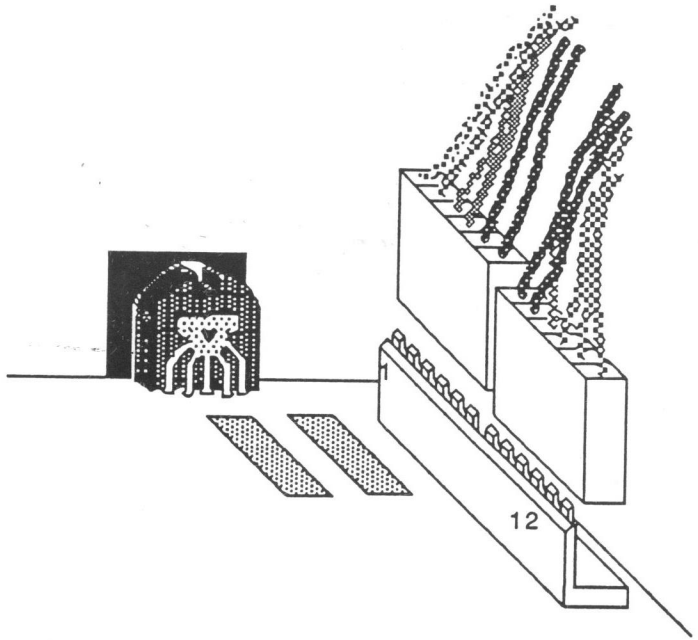
- **Hardware switch connector** Turbo hardware switch connector is located at JP6 on the motherboard. By using a switch connected to it, operation of the computer can be switched between Turbo and Normal modes. For more information on the Turbo switch, refer to the **Hardware switch** section.

In addition to the connectors for the control panel switches and indicators, there are three other connectors remain to be finished:

- **Speaker connector** A speaker may be connected to JP1 on the motherboard. The pinouts for the speaker are as follows:

Pin	Assignment
1	+ 5V DC
2	Data out

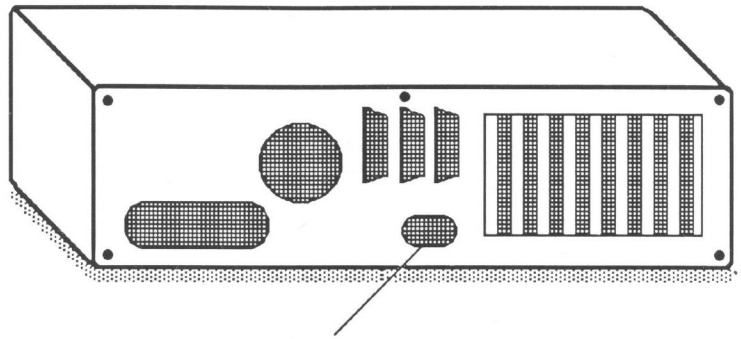
- **Power supply connector** The power supply connector is located at P1 in the upper right corner of the motherboard. To connect the power supply to the motherboard, find the 12-pin connector from the power supply (the other connectors are smaller) and plug it into the connector on the motherboard. There is only one way to plug in the power supply connector: a plastic flange on the connector from the power supply fits inside the connector on the motherboard (refer to the figure below).



The pinouts for the power supply connector are as shown below:

Pin	Assignment
1	Power good
2	Not used
3	+ 12V DC
4	- 12V DC
5	Ground
6	Ground
7	Ground
8	Ground
9	- 5V DC
10	+ 5V DC
11	+ 5V DC
12	+ 5V DC

- **Keyboard connector** The keyboard connector is located at the back of your system unit as shown in the figure below:



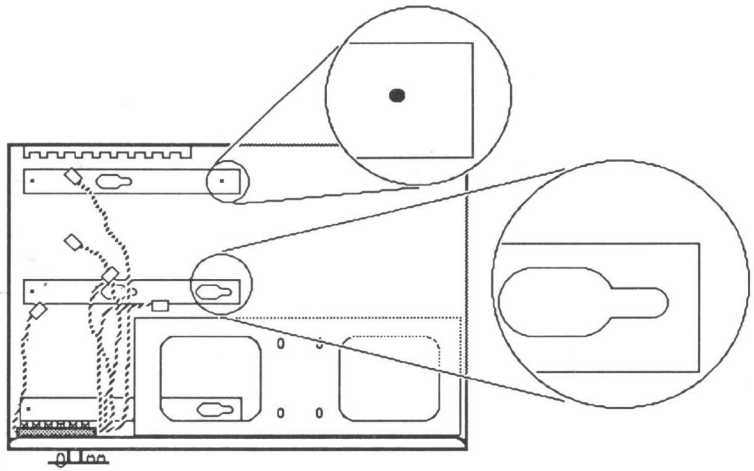
Location of keyboard connector from back panel

The keyboard connector is a five-pin DIN connector. The pinouts are give below:

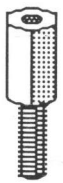
Pin	Assignments
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5 VDC

Fastening motherboard to case

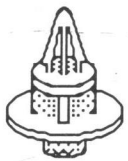
Open the case of your system unit. If it is an empty case, it should look something like the illustration below:



Notice the two types of fastening points circled. The slots may be used with plastic connectors inserted into the motherboard, or brass female connectors. Brass female connectors will be screwed into the holes in the case. The plastic and brass connectors are pictured below:

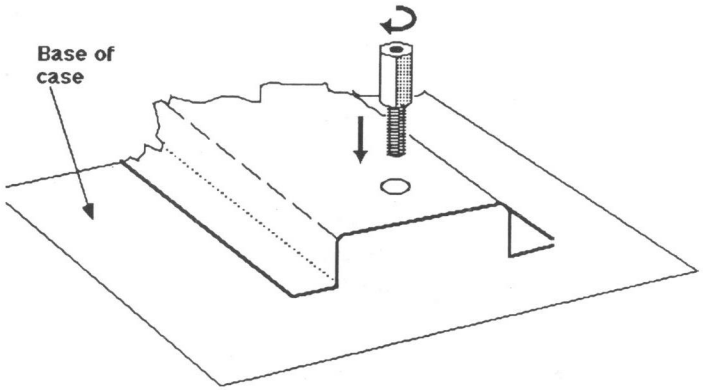


Brass connector



Plastic connector

Screw the brass connectors into the case as shown below:



Insert the plastic connectors into the holes on the motherboard which will be located above the slot-type connectors in your case. The pointed ends of the plastic connectors should be on the top side of the motherboard.

Note that using the plastic connectors is optional, but you should use the brass connectors in order to ground the motherboard to your case. If you have used the plastic connectors in the motherboard, slide them into the slots in the case. Next, fasten the motherboard to the brass connectors with screws. Otherwise, simply place the motherboard over the brass connectors in the case and screw the motherboard snugly down to them.

The motherboard is now fastened to the case.

Reconfiguring

Warning

To ensure the reliability of the computer, **NEVER** reconfigure the board while the power is **ON**.

If you wish to reconfigure the system board at any time, ensure that the power to the system is turned **OFF** before changing any hardware settings, such as DIP switches or jumpers.

Operation

The main advantage of the PIM-TB10-Z Turbo motherboard over ordinary PC/XT motherboards is its dual clock system. This innovation makes it possible for your computer to operate at either of two clock speeds: 4.77MHz or 10MHz. In the 10MHz Turbo mode, your computer will operate up to 110% faster than a conventional 8088-based computer.

NOTE: Do not use RAM memory on an expansion card because its design may not be compatible with the 10MHz CPU at access time. Use memory on the motherboard comprised of 4164 and 41256 and 4464 chips within 120ns. Refer to **RAM installation** section. Recommended chips are shown in the table below.

	4164	41256	4464
NEC	D4164C	D41256C	D4464C
Hitachi	HM4846	HM50256	HM50464
Mitsubishi	M5K4164	M5M4256P	M5M4464P
Panasonic	MN4164	MN41256	MN4464

NOTE: Use NEC® 70108-10 chips to achieve speeds up to 380% faster than an ordinary XT.

Obtaining 10MHz Turbo mode

This mainboard supports both a software switch and a hardware switch for changes between Normal and Turbo modes.

Setting default operation mode

The Turbo hardware switch, jumper JP6 (shown on page 3), gives you the choice of running the PIM-TB10-Z in either Normal or Turbo mode when the power is on. For default operation:

- In Normal mode ..... Place a jumper cap over JP6
- In Turbo mode ..... Take the jumper cap off JP6

Software switch

Before using the software switch, pay attention to whether default operation is in Normal or Turbo mode. If it is in Normal mode, do the following: press and hold down the control < Ctrl > and alternate < Alt > keys on the keyboard while you press the minus < - > key. The cursor on the screen will turn into a box. The Turbo LED on your panel, if you have installed one, will light. For more information on the Turbo LED, refer to the **Panel indicators and switches** section. Now the computer is in Turbo mode.

To return to Normal mode, press the same keys you used to enter Turbo mode. When you enter Normal mode, the cursor will return to the dash (_) form and the Turbo LED will turn off.

If default operation is in Turbo mode, press and hold down the control < Ctrl > and alternate < Alt > keys on the keyboard while you press the minus < - > key to go to Normal mode. The Turbo LED will turn off, and the cursor will turn into a box. To return to Turbo, press the same keys: the Turbo LED will light and the cursor will change into a dash.

Hardware switch

If you have a hardware switch on your panel, connect it to jumper JP6. More information on this is given in the **Panel indicators and switches** section.

Push the hardware switch on to enter Normal mode and push it off to enter Turbo mode.

Hardware switch off Hardware switch on

Using the hardware switch means that the only indication of the mode your computer is in will be the Turbo LED. It will turn on in the Turbo mode and turn off in the Normal mode. The cursor will always have the same appearance.

Alternate use of both switches

Both the hardware and the software switches may be used alternatively, but this is not advised because you may become confused about the mode of operation. When using both switches alternatively, the Turbo LED will be the only accurate indicator of the actual mode: the LED will be on in Turbo mode and off in Normal mode.

Turbo LED and hardware switch

Most 8088-type computer cases do not have a Turbo LED or a Turbo hardware switch. However, both of these items are very useful as you probably can already see. Therefore, it is highly recommended that you install both in your system if you do not already have them. For more information, refer to the **Panel indicators and switches** section.

Using software in Turbo mode

Most software, such as Lotus 1-2-3®, dBase III® and many other applications run flawlessly in Turbo mode. However, you may find that certain kinds of software, like Copy Writer®, runs only in Normal mode.

Technical information

The system board is a double-sided printed circuit board using direct current. The power supply is connected to the board by a 12-pin connector. Other connectors are for a control panel, a speaker and a keyboard. Eight 62-pin expansion slots are also mounted on the board. The I/O channel is bussed across these eight I/O slots.

An eight-switch Dual-In-Line Package (DIP) switch (SW1) is mounted on the board and can be read under program control. The DIP switch provides the system software with information about the installed options, how much storage the system has, what type of display adapter is installed, what operation modes are desired when power is switched on (color or black and white, 80- or 40-character lines) and the number of diskette drives attached.

The system board had five functions: the processor subsystem and its support elements, the Read Only Memory (ROM) subsystem, the Read/Write (R/W) Memory subsystem, the integrated I/O adapters and the I/O channel.

The heart of the 10MHz Turbo system board is the Intel® 8088-1 microprocessor. This processor is an 8-bit external bus version of Intel®'s 16-bit 8086 processor and is software-compatible with the 8086. Thus, the 8088 supports 16-bit operations including multiply and divide and supports 20 bits of addressable memory (1 megabyte of storage).

It also operates in a maximum mode so a coprocessor can be added as a feature. The processor operate in two modes which can be switched, namely the Normal mode and the Turbo mode. When the processor is operating in Normal mode (4.77MHz), the frequency which is derived from a 14.318MHz crystal, is divided by three for the processor clock, and by 4 to obtain the 3.58MHz color burts signal required for color television. When the processor is operating in Turbo mode (10MHz), the frequency is derived from 30MHz.

DMA

Three of the four DMA channels are available on the I/O bus and support high-speed data transfers between I/O devices and memory without processor intervention. The fourth DMA channel is programmed to refresh the system dynamic memory. This is done by programming a channel of the timer counter device to request periodically a dummy DMA transfer. This action creates a memory-read cycle which is available to refresh dynamic storage both on the system board and expansion slots. All DMA data transfers except the refresh channel take five processor clocks of 210ns or 1.05us if the processor ready line is not deactivated. Refreshing DMA cycles takes four clocks (840ns).

Timer

The three programmable timer/counters are used by the system as follows: Channel 0 is used as a general-purpose timer providing a constant time base for implementing a time-of-day clock; Channel 1 is used to time and request refresh cycles from the DMA channel; and Channel 2 is used to support the tone generation for the audio speaker. Each channel has a minimum timing resolution of 1.05us.

Interrupt

Of the eight prioritized levels of interrupts, six are bussed to the expansion slots for use by the interface cards. Two levels are used on the system board. Level 0, the highest priority, is attached to Channel 0 of the timer/counter and provides a periodic interrupt for the time-of-day clock. Level 1 is attached to the keyboard adapter circuits and receives an interrupt for each scan code sent by the keyboard. The Non-Maskable Interrupt (NMI) of the 8088 is used to report memory-parity errors.

Memory

The system board supports both ROM/EPROM and R/W memory. It has space for 32KB x 1 and 8KB x 1 of ROM or EPROM. This ROM contains a power-on self-test, I/O drivers, dot patterns for 128 characters in graphics mode and a diskette. The system board also has from 256KB to 640KB of R/W memory. A minimum system has 256KB of memory.

Keyboard

The system board contains the adapter circuits for attaching the serial interface from the keyboard. These circuits generate an interrupt to the processor when a complete scan code is received. The interface can request execution of a diagnostic test in the keyboard. The keyboard interface is a five-pin DIN connector on the system board that extends through the rear panel of the system unit.

Speaker

The system unit has a 2 1/4-inch audio speaker. The speaker's control circuits and driver are on the system board. The speaker connects through a two-wire interface that attached to a three-pin connector on the system board. The speaker drive circuit is capable of providing approximately 1/2 watt of power. The control circuits allow the speaker to be driven three different ways:

- A direct program control register bit may be toggled to generate a pulse train.
- The output from Channel 2 of the timer/counter may be programmed to generate a waveform to the speaker.
- The clock input of the timer/counter can be modulated with a program controlled by the I/O register bit. All three methods may be performed simultaneously.

Expansion I/O channel

The I/O channel is an extension of the 8088 microprocessor bus. It is, however, demultiplexed, repowered and enhanced by the addition of interrupts and Direct Memory Access (DMA) functions.

The I/O channel contains an 8-bit, bidirectional data bus with 20 address lines, six levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, three channels of DMA control lines, memory refresh timing control lines, a channel check line, a power line and a ground for the adapters. Four voltage levels are provided for the expansion cards: +5V DC, -5V DC, +12V DC and -12V DC. These functions are provided in a 62-pin connector with 100-mil card tab spacing.

A "ready" line is available on the I/O channel to allow operation with slow I/O or memory devices. If the channel's ready line is not activated by an addressed device, all processor-generated memory read and write cycles take four 210ns/clock or 840ns/byte. All processor-generated I/O read and write cycles require five clocks for a cycle time of 1.05us/byte. Refresh cycles occur once every 72 clocks (approximately 15us) and require four clocks or approximately 7% of the bus bandwidth.

I/O devices are addressed using I/O-mapped space. The channel is designed so that 768 I/O devices addressed are available to the I/O expansion cards.

A channel check line exists for reporting error conditions to the processor. Activating this line results in a Non-Masksable Interrupt (NMI) to the 8088 processor. Memory expansion options use this line to report parity errors.

The I/O channel is repowered to provide sufficient drive to power all eight (J1 through J8) expansion slots, under conditions of two Low-power Schottsky (LS) loads per slot. The I/O adapters typically use only one load.

I/O channel description

The following is a description of the PC/XT I/O channel. All lines are TTL compatible.

OSC, oscillator
It is a high-speed clock with a 70ns period (14.31818MHz). It has a 50% duty cycle.

CLK, system clock
It operates at one-third the frequency of the oscillator and has a period of 210ns (4.77MHz). The clock has a 33% duty cycle.

Reset
This line is used to reset or initialize system logic upon power up or during a low line voltage outage. This signal is synchronized to the falling edge of the clock and is active high.

A0-A19, address bits 0 to 19
These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the least significant bit (LSB) while A19 is the most significant bit (MSB). These lines are generated by either the processor or the DMA controller. They are active high.

D0-D7, data bits 0 to 7
These lines provide data bus bits 0 to 7 for the processor, memory and I/O devices. D0 is the least significant bit (LSB) while D7 is the most significant bit (MSB). These lines are active high.

ALE, address latch enable
This line is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the falling edge of ALE.

I/O CH CK, I/O channel check
This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is activated.

I/O CH RDY, I/O channel ready
This line, normally high (ready), can be pulled low (not ready) by a memory or an I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a real or write command. This line should **never** be held low more than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles.

IRQ2-IRQ7, interrupt requests 2 to 7
These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 having the highest priority and IRQ7 having the lowest. An interrupt request is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor (interrupt service routine).

IOR, I/O read command
This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

IOW, I/O write command
This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor for the DMA controller. This signal is active low.

MEMR, memory read command
This command line instructs the memory to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMW, memory write command
This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

DRQ1-DRQ3, DMA requests 1 to 9
These lines are for asynchronous channel requests used by peripheral devices to gain DMA services. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK line goes active.

DACK 0-3, DMA acknowledge 0 to 3
These lines are DACK 0 -3 used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK 0). They are active low.

AEN, address enable
This line is used to degate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active high, the DMA controller had control over the address bus, the data bus, the read command lines (memory and I/O) and the write command lines (memory and I/O).

T/C, terminal count
This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.

CARD SLCTD, card selected
This line is activated by cards in expansion slot J8. It signals the system board that the card had been selected and that appropriate drivers on the system board should be directed either to read from or to write to expansion slot J10. Connectors J3 through J10 are tied together at this pin, but the system board should be driven by an open collector device.

The following voltages are available on the system board I/O channel:

- +5V DC plus or minus 5% located on two connector pins.
- -5V DC plus or minus 10% located on one connector pin.
- +12V DC plus or minus 5% located on one connector pin.
- -12V DC plus or minus 10% located on one connector pin.
- GND (ground) located on three connector pins.

Speaker interface

The sound system has a small, permanent magnet, 2 1/4-inch speaker. The speaker can be driven from one or two sources:

- An 8255A-5 PPI output bit. The address and the bit are defined in the I/O address map.

- A timer clock channel, the output of which is programmable within the functions of the 8253-5 timer when using a 1.19MHz clock input. The timer gate is also controlled by an 8255A-5 PPI output port bit. Address and bit assignment are in the I/O address map.

The speaker connector is a two-pin 90-degree connector. See **Speaker connector** section for more information.