HOT-433 Version 4.0

486 PCI-Mainboard

NOTICE

Manual Version R3.0 (for 433Ver4.0)

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Preface

HOT-433 mainboard is a highly integrated IBM PC/AT compatible system board designed to accommodate 25MHz to 133MHz 486 processors, and features high-performance secondary cache memory architecture from 128KB up to 512KB.

HOT-433 mainboard features four PCI (Peripheral Component Interconnected) local bus and four ISA (Industry Standard Architecture) bus expansion slots.

HOT-433 mainboard also integrate one 2-channel PCI IDE controller, one floppy controller, one parallel port, two serial ports, and one PS/2 mouse port.

Chapter 1 Introduction

Specification

CPU Function

- CPU clock:25/33/40/50/66/80/100/120/133MHz
- Supports Intel 486SX/DX/2DX2/DX4,
  AMD Am486DX/DX2/DX4/Am5x86-P75,
  Cyrix 486S/DX/DX2/DX4/5x86

Chipset

- UMC 8881, 8886 and 8669/8663
- Supports L1 and L2 write back cache
- Supports PCI master and slave up to 33MHz
- Supports PCI burst mode access to local memory

Memory

- Supports Fast Page Mode and EDO DRAM
- Supports four banks of local DRAM system ranging from 1MB to 256MB of host memory
- Supports 1MB, 2MB, 4MB, 8MB, 16MB, 32MB and 64MB 72-pins SIMM

Cache Memory

- Supports 128/256/512KB write-back secondary cache.

Power Management Function

- Provides four power management modes : On, Doze, Standby and Suspend
- Supports Microsoft APM
- Provides EPMI (External Power Management Interrupt) pin

Expansions

- 32-bit PCI bus x 4
- 16-bit ISA bus x 4
- 2-channel PCI IDE port
  - Supports up to 4 IDE driver
  - Supports 32 and 16-bit data transfers
  - Supports buffers that operate read prefresh and write port transactions
  - Fully ANSI ATA spec. 3.X compatible
- One floppy port
- One parallel port
  Supports **SPP** (PS/2 compatible bidirectional Parallel Port), **EPP** (Enhanced Parallel Port), and **ECP** (Extended Capabilities Port) high performance parallel port.
- Two serial ports
  - Supports 16C550 compatible UARTS.
- One PS/2 mouse port (optional)

Board Design

- Dimension 22cm x 22cm

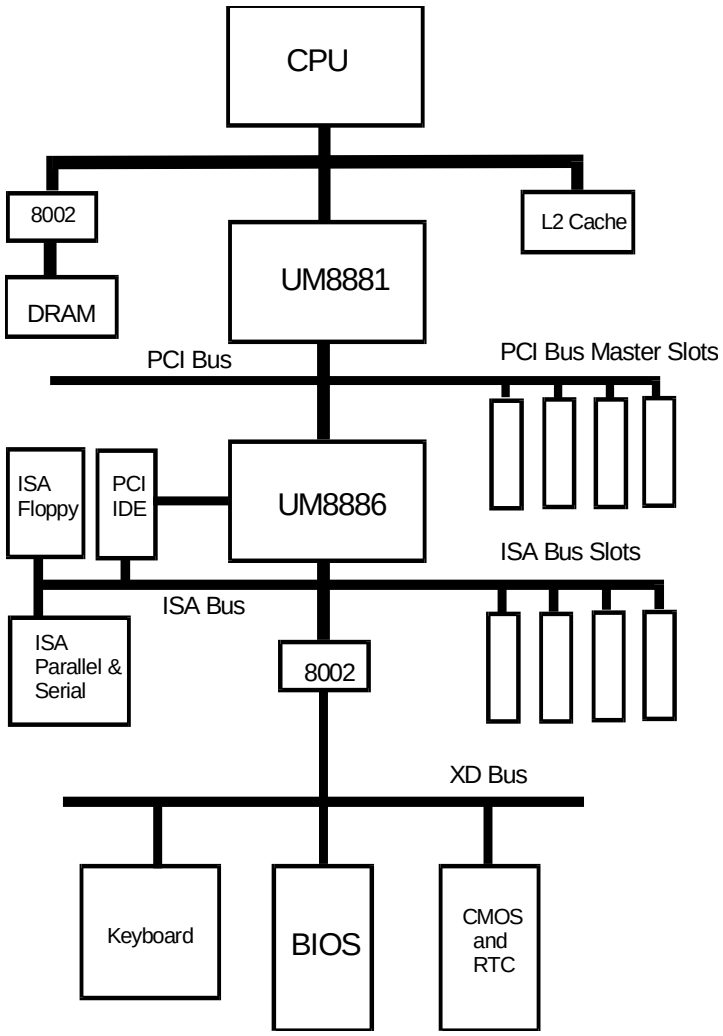
* Note :

1. HOT-433 main board with UMC8881F-Exx chip support EDO DRAM.

2. When EDO DRAM are using, please select "EDO" type in category of "On board DRAM option" of chipset BIOS setup. (please refer to page 42)

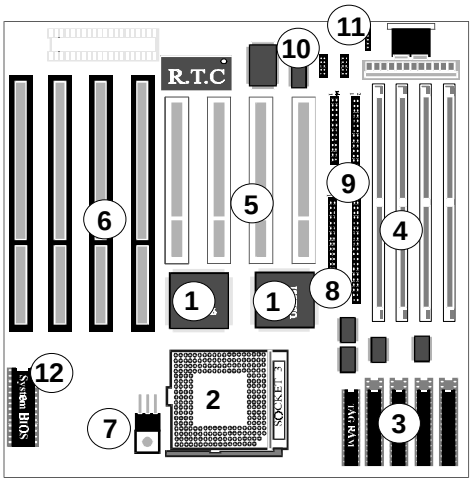
3. Please do not use Page mode and EDO mode DRAM simultaneously on board.

Block Diagram



433 Mainboard Description

The major components of 433 maniboard are illustrated and described right and below. Please take a minute to become familiar with the board design.



1. Chipset ASIC

433 mainboard is designed around a set of highly integrated UMC ASIC, which offers optimum performance on PCI and ISA base system for a cache controller, a local DRAM controller, and an integrated Peripherals controller.

2. System Microprocessor

433 mainboard accept member of the 486 family of high performance 32-bit microprocessors in PGA package. The mainboard is designed to run at a clock speed from 25 to 50MHz on CPU bus clock, and 25 to 133MHz on CPU core clock.

3. Secondary Cache Architecture

433 maniboard features a secondary cache memory architecture, which complements the 8KB or 16KB internal cache of the 486 family. It support secondary cache with size of 128KB, 256KB and 512KB.

4. Memory Architecture

433 mainboard features four 72-pin SIMM (Single In-line Memory Module) sockets organized into four banks, which allow flexible memory configuration and expansion. It may use 1MB, 2MB, 4MB, 8MB, 16MB, 32MB, or 64MB SIMM to expand memory from 1MB to 256MB.

5. PCI Expansion Slots

433 mainboard provides four 32-bit PCI expansion slots, which may accommodate many third-party expansion cards and increase flexibility in designing custom platforms.

6. ISA Expansion Slots

433 mainboard provides four 16-bit ISA expansion slots, which may accommodate many third-party expansion cards and enormous flexibility in designing custom platforms.

7. 5V- 3.3/3.45/3.6/4.0V Voltage Regulator

For Intel 486DX4 (P24C), AMD Am486DX2-80/DX4-100/Am5x86-P75, and Cyrix 486DX2-66,DX2-80,DX4-75/100, 5X86 CPU, 433 mainbaord provides a voltage regulator to regulate voltage from 5V to 3.3/3.45/3.6/4.0V.

8. On-board PCI IDE Controller

433 mainboard provides a onboard 2-channel IDE controller with high speed data transfer rate. It supports up to four IDE hard disk drives.

9. On-board Floppy Controller

433 mainboard provides a on-board floppy controller that support two floppy disk drives.

10. On-board Serial/Parallel Port

433 mainboard provides two serial (COM) ports and one parallel port.

11. On-board optional PS/2 mouse Port

433 provides an 6-pin PS/2 mouse port connector and optional onboard PS/2 keyboard & PS/2 mouse mini DIN connectors.

12. System BIOS

433 mainboard provides a licensed AMI system WinBIOS which is a particularly designed to offer optimum performance of the mainboard.

13. Attached Accessories

one 40-pin hard disk drive flat cable

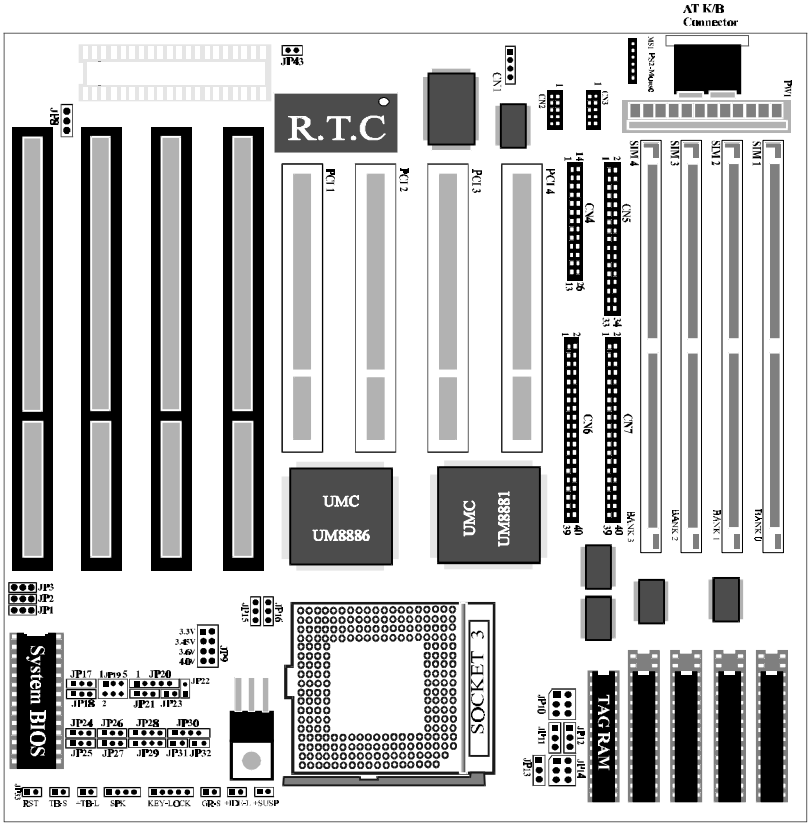
one 34-pin floppy disk drive flat cable

one 9-pin and 25-pin serial connector with cable

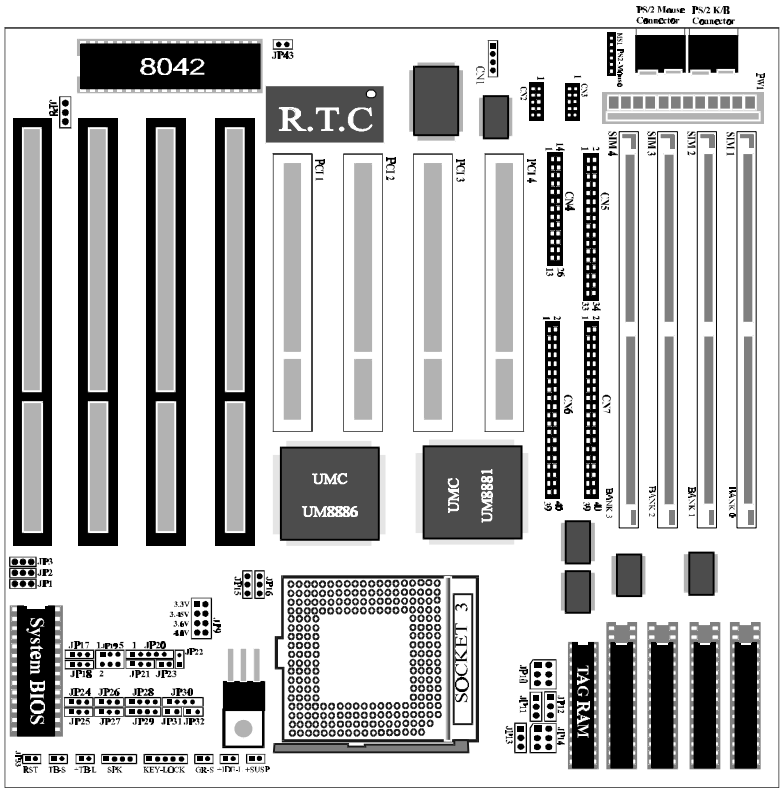
one 25-pin parallel port connector with cable

on-board enhanced IDE drivers on 3.5" floppy diskette

433 Mainboard Placement
(With AT Keyboard Connector)



433 Mainboard Placement
(With PS/2 Keyboard & Mouse Connectors)

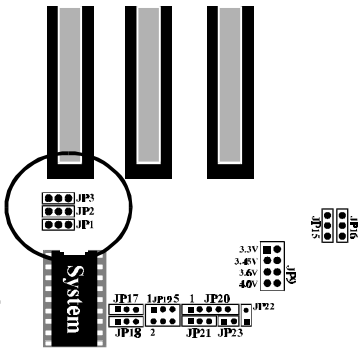


Chapter 2 Jumper Setting

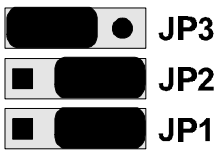
System Clock Selection

433 mainboard features a clock generator to provide adjustable system clock frequency. JP1, JP2, and JP3 are all 3-pin jumper which determine the clock frequency.

Proper jumper settings for generating 25MHz to 50MHz clock frequency for 486 system are shown bellow.



25MHz System Clock



33MHz System Clok

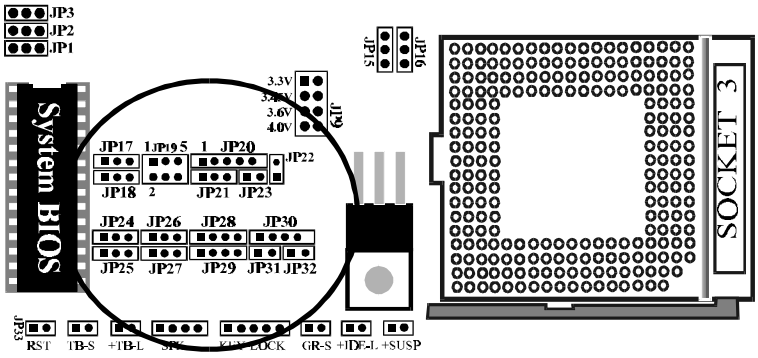
40MHz System Clok

50MHz System Clok

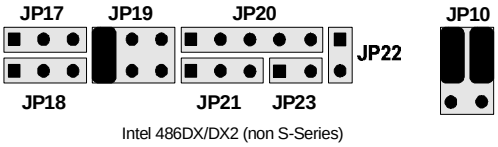
CPU Type Selection

433 mainboard accepts any member of the 486 series microprocessors. If you try to install or upgrade the CPU, you must set the CPU type jumpers correctly.

Note : It is highly recommended that a CPU cooling fan is attached to the CPU to ensure system stability.

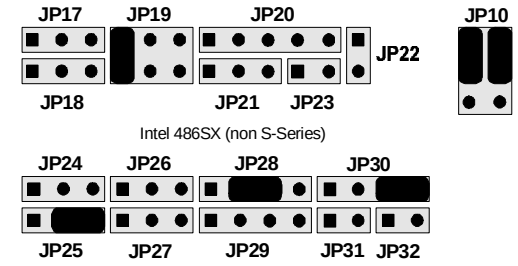


Intel 486DX/DX2



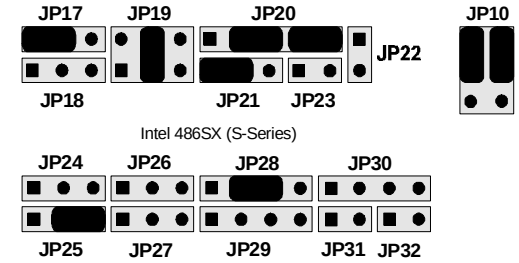
Intel 486DX/DX2 (non S-Series)

Intel 486SX



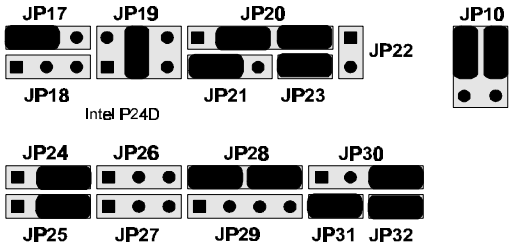
Intel 486SX (non S-Series)

Intel 486SX S-Series

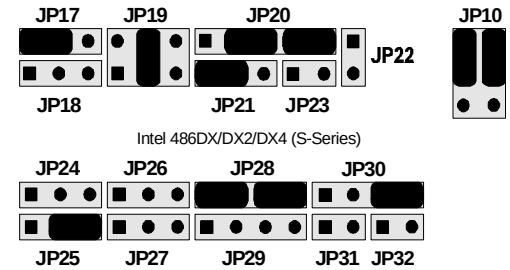


Intel 486SX (S-Series)

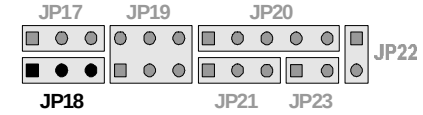
Intel P24D



Intel P24D

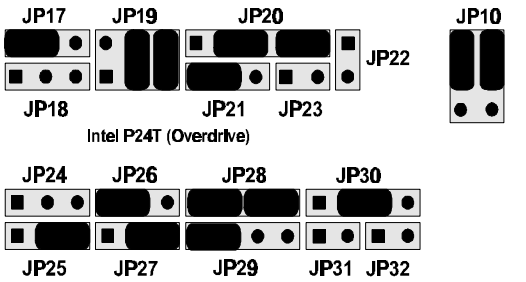


Intel 486DX4 (P24C) Clock Multiplier - JP18

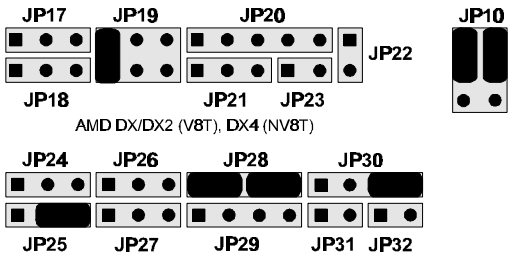


CPU Type	Core/Bus Clock Ratio	JP18	Internal Core Clock	External Bus Clock
DX4-100	3 : 1		100MHz	33MHz
DX4-100	2 : 1		100MHz	50MHz
DX4-75	3 : 1		75MHz	25MHz

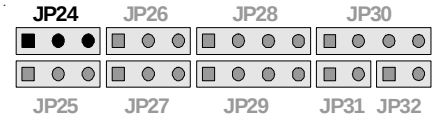
Intel P24T



AMD Am486DX/DX2(V8T)
AMD Am486DX4 (NV8T)

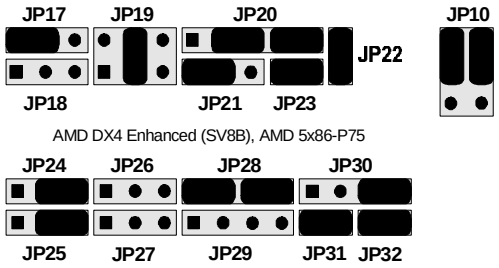


AMD Am486DX2/DX4 Clock Multiplier - JP24

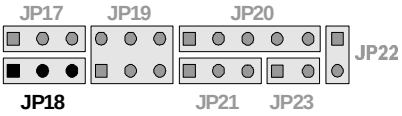


CPU Type	Core/Bus Clock Ratio	JP24	Internal Core Clock	External Bus Clock
DX4-100	3 : 1		100MHz	33MHz
DX4-100	2 : 1		100MHz	50MHz
DX2-80	2 : 1		80MHz	40MHz

AMD Am486DX4 Enhance (SV8B)
AMD Am5x86-P75

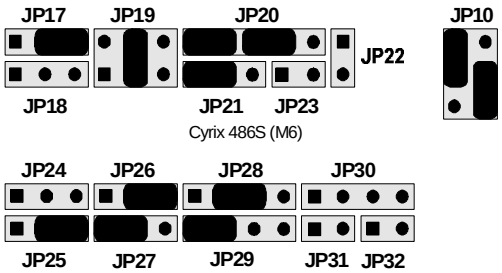


AMD Am486DX4 Enhance & Am5x86-P75 Clock Multiplier - JP18

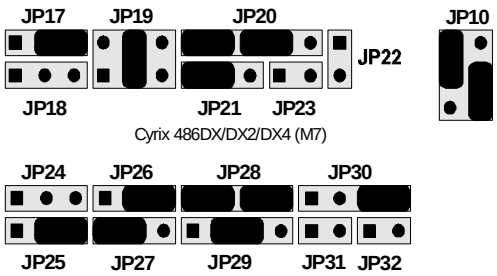


CPU Type	Core/Bus Clock Ratio	JP18	Internal Core Clock	External Bus Clock
AmDX4	3 : 1		100/120MHz	33/40MHz
AmDX4	2 : 1		100MHz	50MHz
Am5x86-P75	4 : 1		133/160MHz	33/40MHz

Cyrix Cx486S (M6)

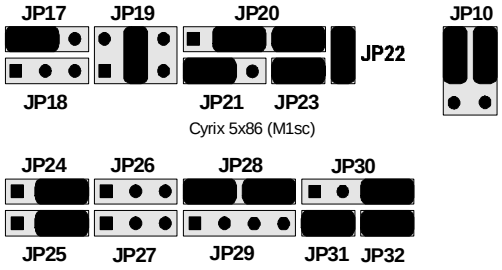


Cyrix Cx486DX/DX2/DX4 (M7)



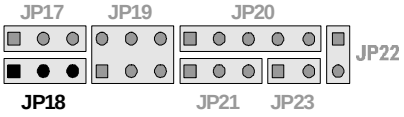
Cyrix 486DX/DX2/DX4 (M7)

Cyrix 5X86



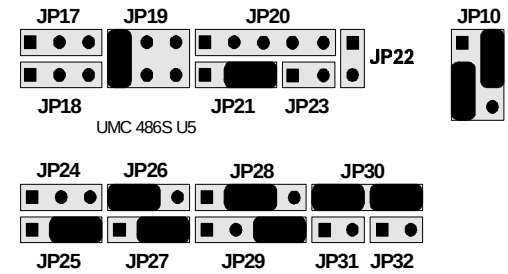
Cyrix 5x86 (M1sc)

Cyrix 5x86 Clock Multiplier - JP18



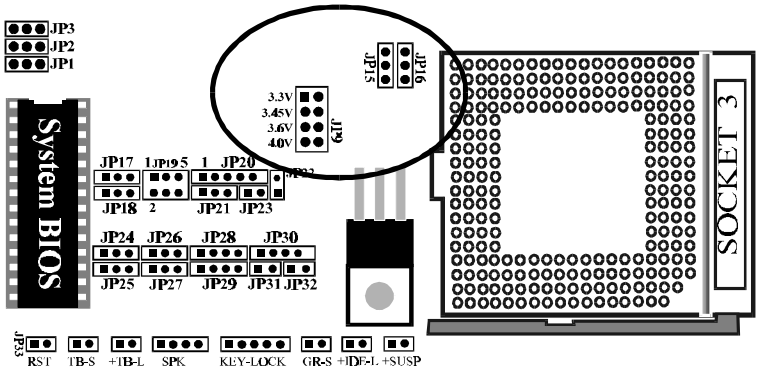
CPU Type	Core/Bus Clock Ratio	JP18	Internal Core Clock	External Bus Clock
Cyrix 5x86-100	3 : 1		100MHz	33MHz
Cyrix 5x86-100	2 : 1		100MHz	50MHz
Cyrix 5x86-120	3 : 1		120MHz	40MHz
Cyrix 5x86-133	4 : 1		133MHz	33MHz

UMC 486S U5


JP17
JP19
JP20
JP10
JP22
JP18
JP21
JP23
UMC 486S U5
JP24
JP26
JP28
JP30
JP25
JP27
JP29
JP31
JP32

CPU Voltage Selection

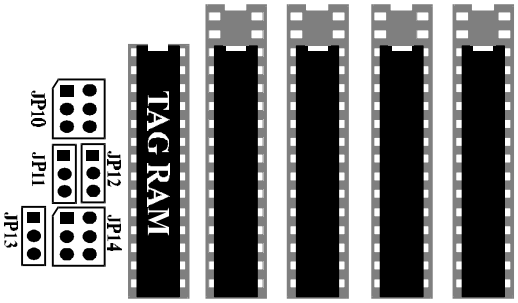
For Intel, AMD, and Cyrix 3V CPU, 433 mainboard features single voltage regulator to generate the voltage for CPU (Vcc) from 5V to 3.3/3.45/3.6/4.0V. JP15, JP16, and JP9 are provided for voltage setting between 5V and 3.3/3.45/3.6/4.0V.



CPU Voltage Selection		
CPU Voltage	**JP 15 / JP 16**	**JP 9**
5 Volt		**Don't care**
3,3 Volt		**Close 1-2**
3,45 Volt		**Close 3-4**
3,6 Volt		**Close 5-6**
4,0 Volt		**Close 7-8**

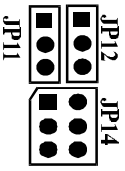
Cache Size Selection

433 mainboard supports secondary cache memory sizes of 128KB, 256KB, and 512KB. Cache memory is realized by four Data SRAM and one Tag SRAM. The Data SRAM used in 433 mainboard is 32Kx8, 64Kx8, or 128Kx8, Tag SRAM used in 433 mainboard is 8Kx8, 16Kx8 or 32Kx8.



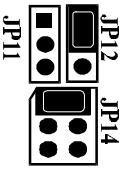
128 KB Cache Memory

Cache Size	Data RAM U15, 16, 17, 18	Tag RAM U26	Cacheable Range	
			Write-Through	Write-Back
128KB	32K x 8	8K x 8 /32K x 8	32MB	16MB

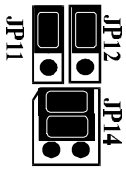


256 KB Cache Memory

Cache Size	Data RAM U15, 16, 17, 18	Tag RAM U26	Cacheable Range	
			Write-Through	Write-Back
256KB	64K x 8	16K x 8 /32K x 8	64 MB	32 MB



512 KB Cache Memory



Cache Size	Data RAM U15, 16, 17, 18	Tag RAM U26	Cacheable Range	
			Write-Through	Write-Back
512 KB	128K x 8	32K x 8	128 MB	64 MB

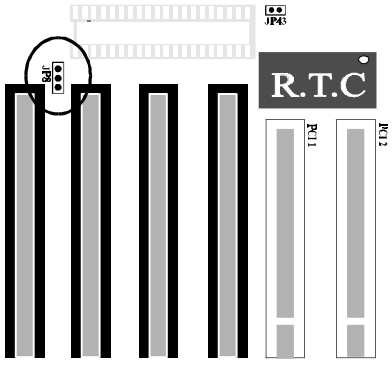
Flash EEPROM Vpp Selection

433 mainboard supports EPROM or 12V/5V programming voltage flash EEPROM for system BIOS. JP8 is provided to accommodate 12V and 5V flash EEPROM.

OPEN, or **Pin 2 - 3 Close** for 5V flash

Pin 1 - 2 Close for 12V flash.

Note: If an EPROM is in use on 433 system BIOS, the user may ignore the setting of JP8.



Clear CMOS

433 mainboard supports jumper **JP43** for discharge mainboard's CMOS memory. The CMOS memory retains the system configuration information in the component of R.T.C.

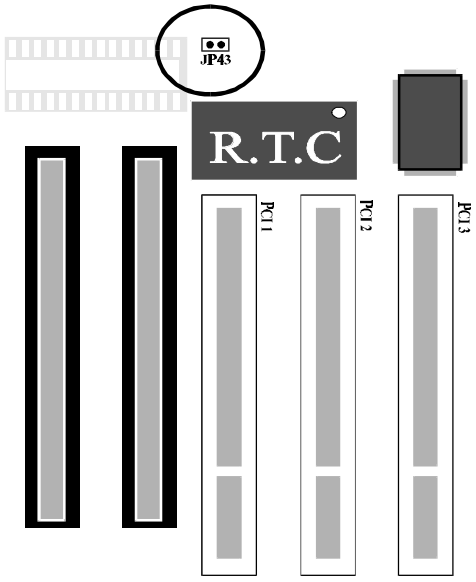
You should close this jumper for a moment when you wish to clear CMOS memory, and then make sure open this jumper for normal operation to retain your new CMOS data.

Note: Clear CMOS & R.T.C function available only when "DS12887A" or "DS12B887" are in use.

There are different ways to discharge CMOS memory between "DS12887A" and "DS12B887".

DS12887A - Turn off power, close jumper JP43 for 2 to 3 seconds then release and CMOS will be discharged.

DS12B887 - Keep power on, close jumper JP43 for 2 to 3 seconds then release and turn off power, CMOS will be discharged.



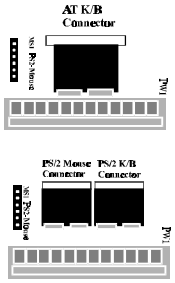
Connectors

Power Connector - PS1

PIN	Name	Function	Pin	Name	Function
1	PWRGD	Power Good	7	GND	Ground
2	+ 5 V	+ 5 volts Vcc	8	GND	Ground
3	+ 12 V	+ 12 volts	9	- 5 V	- 5 volts
4	- 12 V	- 12 volts	10	+ 5 V	+ 5 volts Vcc
5	GND	Ground	11	+ 5 V	+ 5 volts Vcc
6	GND	Ground	12	+ 5 V	+ 5 volts Vcc

Keyboard Connector - KB

433 mainboard provides access to AT-style keyboard connector integrated on the back panel, a PS/2 style keyboard and PS/2 style mouse connector are optional.



PS/2 Mouse Connector - MS1

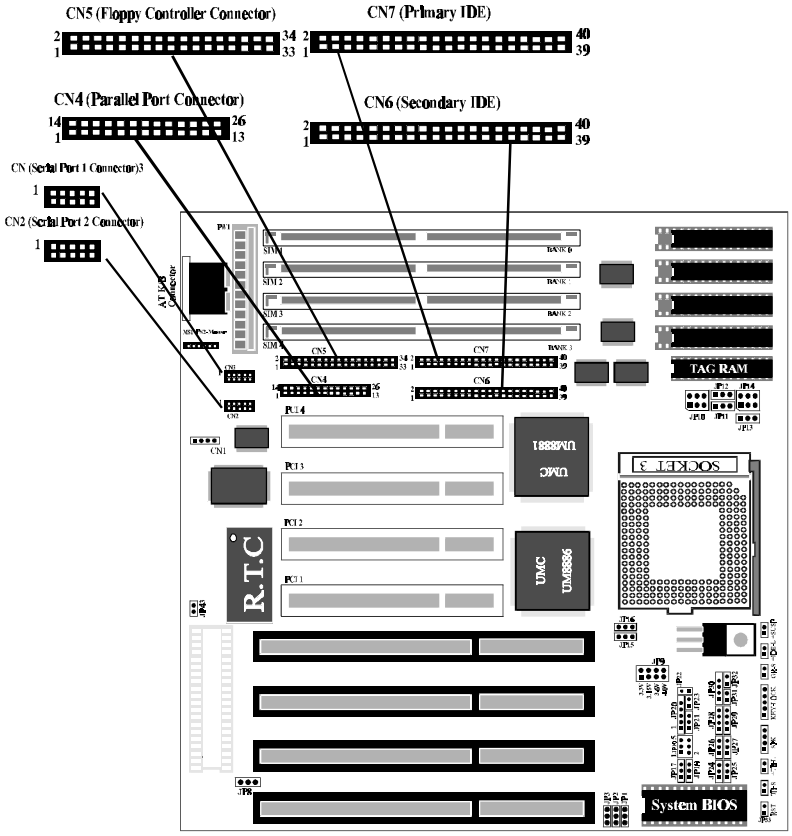
433 mainboard provides two type of PS/2 style mouse connectors, one for 6-pin header MS1 near by keyboard connector and one for optional mini DIN type connector.

6-pin header connector, the right table shows the pinout connection.

PIN	PINOUT
1	Data
2	Empty
3	Ground
4	VCC
5	Clock
6	Empty

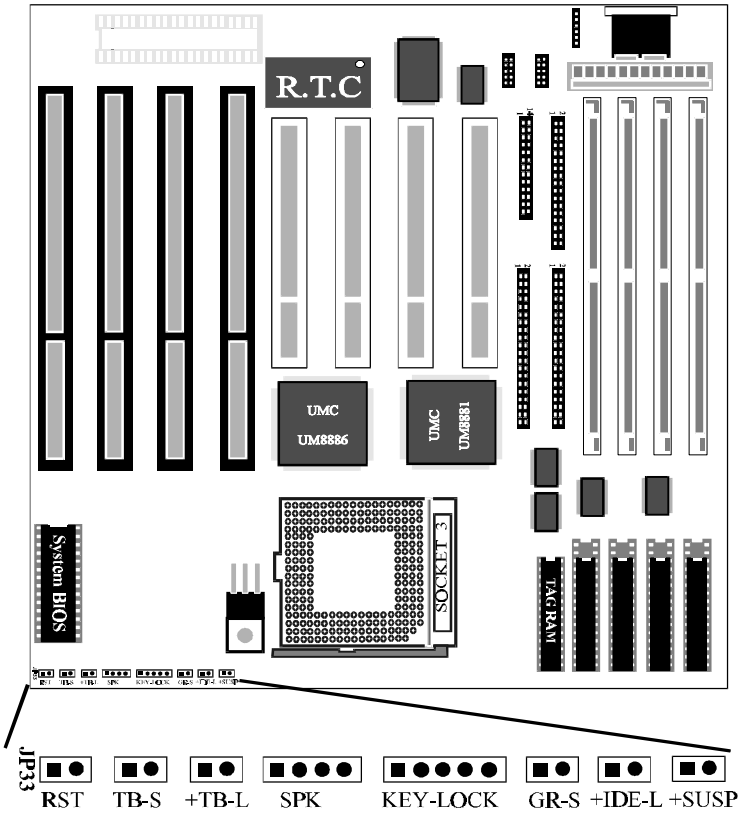
I/O Connectors

The mainboard contains pin header connections for cabling, to the serial, parallel, floppy, and IDE interfaces. List figure show the locations of these connectors and the orientation of pin 1 on each.



Front Panel Connectors

The mainboard contains pin header connections for cabling, to the Hardware Reset, Turbo LED, PC Speaker, Key Lock/Power LED, and Hard Drive IDE LED. List figure shows the location of these connectors.



Chapter 3 Memory Configuration

433 mainboard provides great flexibility to support a number of different on-board fast page mode and EDO DRAM up to 256MB.

On-board memory SIMM sockets are organized into four banks, with one SIMM socket assigned to each memory banks. 433 mainboard supports 1MB, 2MB, 4MB, 8MB, 16MB, 32MB, and 64MB 72-pin SIMM modules.

The following table shows the possible memory configuration of 433 mainboard.

433 Memory Configuration Reference Table				
BANK 0	BANK 1	BANK 2	BANK 3	TOTAL
1MB	NONE	NONE	NONE	1MB
1MB	1MB	NONE	NONE	2MB
1MB	1MB	1MB	NONE	3MB
1MB	1MB	1MB	1MB	4MB
2MB	NONE	NONE	NONE	2MB
2MB	2MB	NONE	NONE	4MB
2MB	2MB	2MB	NONE	6MB
2MB	2MB	2MB	2MB	8MB
4MB	NONE	NONE	NONE	4MB
4MB	4MB	NONE	NONE	8MB
4MB	4MB	4MB	NONE	12MB
4MB	4MB	4MB	4MB	16MB
8MB	NONE	NONE	NONE	8MB
8MB	8MB	NONE	NONE	16MB
8MB	8MB	8MB	NONE	24MB
8MB	8MB	8MB	8MB	32MB
16MB	NONE	NONE	NONE	16MB
16MB	16MB	NONE	NONE	32MB
16MB	16MB	16MB	NONE	48MB
16MB	16MB	16MB	16MB	64MB

433 Memory Configuration Reference Table (Cont'd)				
BANK 0	BANK 1	BANK 2	BANK 3	TOTAL
32MB	NONE	NONE	NONE	32MB
32MB	32MB	NONE	NONE	64MB
32MB	32MB	32MB	NONE	96MB
32MB	32MB	32MB	32MB	128MB
64MB	NONE	NONE	NONE	64MB
64MB	64MB	NONE	NONE	128MB
64MB	64MB	64MB	NONE	192MB
64MB	64MB	64MB	64MB	256MB
1MB	1MB	2MB	2MB	6MB
1MB	1MB	4MB	4MB	10MB
1MB	1MB	8MB	8MB	18MB
1MB	1MB	16MB	16MB	34MB
1MB	1MB	32MB	32MB	66MB
2MB	2MB	4MB	4MB	12MB
2MB	2MB	8MB	8MB	20MB
2MB	2MB	16MB	16MB	36MB
2MB	2MB	32MB	32MB	68MB
4MB	4MB	8MB	8MB	24MB
4MB	4MB	16MB	16MB	40MB
4MB	4MB	32MB	32MB	72MB
8MB	8MB	16MB	16MB	48MB
8MB	8MB	32MB	32MB	80MB
16MB	16MB	32MB	32MB	96MB
16MB	16MB	64MB	64MB	160MB
32MB	32MB	64MB	64MB	192MB

Notes:

*Please do nto use fast page mode SIMM and EDO SIMM on board simultaneously.

*When EDO DRAM are using, please select "EDO" type in category of "On board DRAM option" of chipset BIOS setup. (please refer to page 42)

*All SIMMs must be 70 ns or faster.

*All banks can use either single-sided or double-sided SIMMs.

Chapter 4 Power Management

433 mainboard provides four power management modes for reducing power consumption : On, Doze, Standby, and Suspend. Every single power management mode, 433 mainboard provides distinguishable flash speed indicating via turbo-LED.

433 mainboard also provide EPMI and power supply power down connector to enhanced power management.

Power Management Modes Description

ON mode. The ***ON*** mode is the normal operating mode of the PC system. In this mode, the doze timer (15 sec to 512 min) starts counting if no activity is taking place and the programmable time-out period has expired. The system will enter to doze mode. The types of activity monitored include Keyboard Controller, VGA, IDE, COM port, LPT port, Floppy, PCI master, ISA master, DMA, and one programmable memory region and one programmable I/O region.

DOZE mode. In this mode, CPU frequency is slowed to 1/2 of normal frequency and the ***STANDBY*** timer (2 min to 512 min) starts counting if no activity is taking place. The activities monitored are the same as in ***ON*** mode.

STANDBY mode. CPU and system future more reduce to a lower frequency. In this mode, the ***SUSPEND*** timer (2 min to 512 min) starts counting if no activity is taking place. The activities monitored are the same as in ***ON*** mode.

SUSPEND mode. In this mode, if S-Series CPU is present, 433 mainboard will stop the CPU clock (0MHz), slow down the system clock, power down the secondary cache. Auto-wake-up, including keyboard, mouse, EPMI (GR-S)button, and modem, and so forth, is programmable.

Power Management Modes Indicator

Normally the "**LED1**" (Turbo-LED) is a turbo LED. But when system gets into power management mode, the LED will flash to indicate the working status of different power management modes.

a. In **ON** (Normal) mode, turbo-LED active as a turbo/de-turbo indicator.

b. In **DOZE** mode, turbo-LED flash about per second.

c. In **STANDBY** mode, turbo-LED flash about per two seconds.

d. In **SUSPEND** mode, turbo-LED turned off.

EPMI Connector --- GR-S (JP35)

EPMI (External Power Management Interrupt) pin is provided for special purposes, such as standby(suspend)/resume button. When pushing this button will force system into power management mode, and the system will resume if the button is pushed again.

Power Supply Power Down Connector --- JP6

433 mainboard also provides a power supply power down connector to control the A.C. output of system power supply. If your power supply has signal to control the A.C. output, the signal can be connected to JP6; when system gets into power management mode, power supply A.C. output will be turned off. By this way, you can control other devices such as monitor ON/OFF.

Chapter 5 BIOS Setup

BIOS Setup configures system information that is stored in CMOS RAM. WINBIOS Setup has an easy-to-use graphical user interface that will be immediately recognizable to anyone who has ever used Microsoft Windows. WinBIOS Setup sets a new standard in BIOS user interfaces.

Starting WinBIOS Setup

As POST executes, the following message appears :

Hit <DEL> if you want to run SETUP

Press <Del> to run WinBIOS Setup.

Bus Mouse and Microsoft Mouse Support on BIOS Setup :

The following types of mouse devices are supported.

PS/2- type mouse.

Bus mouse that use IRQs 3, 4, or 5 (IRQ2 is not supported).

Microsoft-compatible mouse.

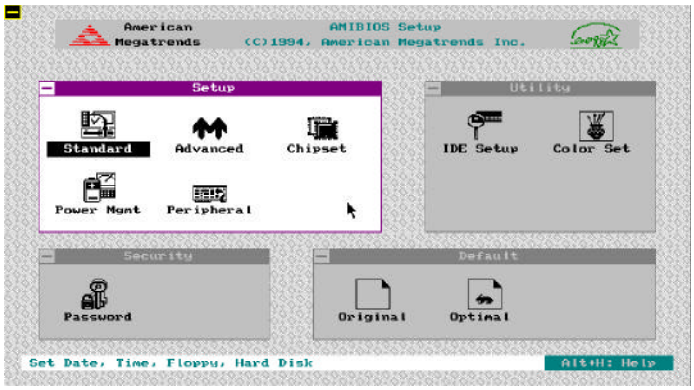
Logitech C-series-compatible mouses using the MM protocol.

WinBIOS Setup can be accessed via keyboard, mouse, or pen. The mouse click functions are :

single click to change or select both global and current field and double click to perform an operation in the selected field.

BIOS Setup Feature

The WinBIOS Setup main menu, shown below, is organized into four windows. Each window corresponds to a section in this chapter.



Each section contains several icons. Clicking on each icon activates a specific function. The WinBIOS Setup icons and functions are described in this chapter. The sections are :

Setup

This section has five icons that permit you to set system configuration options such as date, time hard disk type, floppy type, chipset parameter, power management, and peripheral I/O setup.

Utilities

This section has four icons that perform system functions.

Security

This section has one icon that control WinBIOS security features.

Default

This section has three icons that permit you to select a group of settings for all WinBIOS Setup options.

Each WinBIOS Setup option has two default settings. These settings can be applied to all WinBIOS Setup options when you select the Default section on the WinBIOS Setup main menu. The types of default are:

Original

These settings provide the restoring of old value.

Optimal

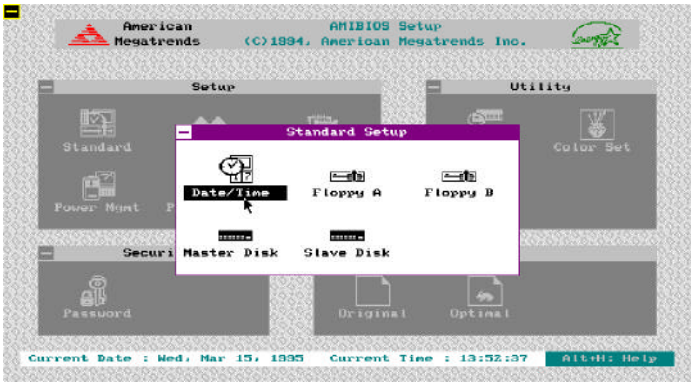
These settings provide that best performance characteristics.

Using the Keyboard with WinBIOS Setup

WinBIOS Setup has a built-in keyboard driver that uses simple keystroke combinations :

Keystroke	Function
<Tab>	Move to the next window or field.
⇨⇦⇧⇩	Move to the next field to the right, left, above, or below.
<Enter>	Select in the current field.
+	Increments a value.
-	Decrements a value.
<Esc>	Closes the current operation and return to previous level.
<PgUp>	Returns to the previous page.
<PgDn>	Advances to the next page.
<Home>	Returns to the beginning of the text
<End>	Advances to the end of the text.
<Alt><H>	Access a help window.
<Alt><Spacebar>	Exit WinBIOS Setup.
Alphabetic keys	A to Z are used in the Virtual Keyboard, and are not casesensitive.
Numeric Keys	0 to 9 are used in the Virtual Keyboard and Numeric Keypad.

Standard Setup



Date, Day and Time Configuration

Select the Standard option. Select the Date and Time icon. The current values for each category are displayed. Enter new values through the keyboard.

Hard Disk C: Type, Hard Disk D: Type

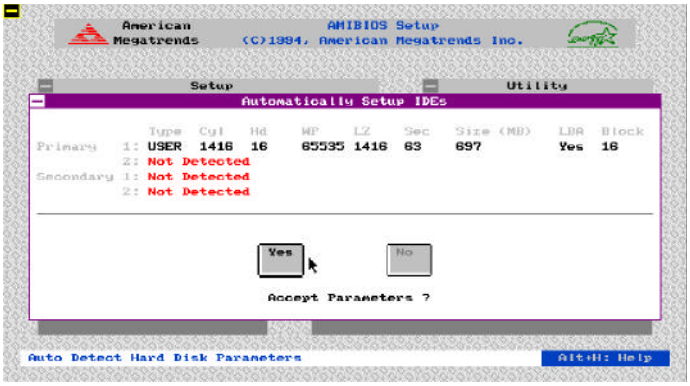
Select one of these hard disk drive icons to configure the drive named in the option. A scrollable screen that lists all valid disk drive types is displayed. Select the correct type and press <Enter>. If the hard disk drive is an IDE drive, select**IDE Setup** from the Utility section of the WinBIOS Setup main menu to allow WinBIOS to automatically detect the IDE drive parameters and report them on this screen.

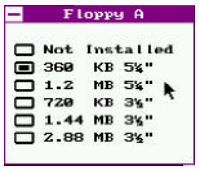
Using Auto Detect Hard Disk (Only for IDE

drivers)

If you select **IDE Setup** from the Utility section of the WinBIOS Setup main menu, WinBIOS automatically finds all IDE hard disk drive parameters. WinBIOS places the hard disk drive parameters that it finds in the Drive Type fields in Standard Setup.

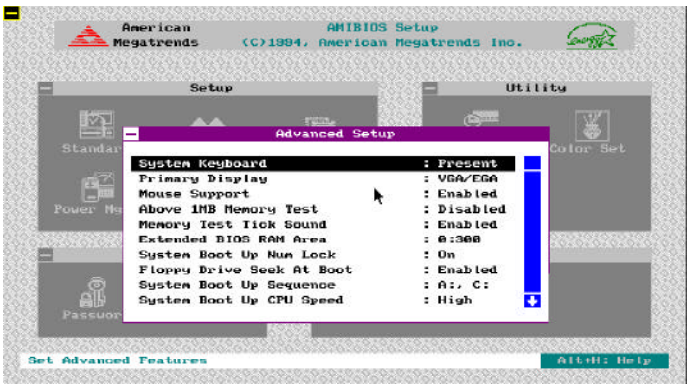
Floppy Drive A:, Floppy Drive B:





Move the cursor to these fields via and select the floppy type. The settings are *360KB 51/4 inch, 1.2MB 51/4 inch, 720KB 31/2 inch, 1.44MB inch, or 2.88MB 31/2 inch.*

Advanced Setup



System Keyboard

Select this option to configure whether checking for keyboard present or not.

Primary Display

Select this option to configure the type of monitor attached to the computer. The settings are ***Monochrome, Color 40 x 25, Color 80 x 25, VGA/PGA/EGA***, or ***Not Installed***.

Mouse Support

When this option is enabled, WinBIOS supports a PS/2-type mouse. The settings are ***Enabled*** or ***Disabled***.

Above 1 MB Memory Test

When this option is enabled, the WinBIOS memory test is performed on all system memory. When this option is disabled, the memory test is done only on the first 1 MB of system memory. The settings are ***Enabled*** or ***Disabled***.

Memory Test Tick Sound

This option enables or disables the ticking sound during the memory test. The settings are ***Enabled*** or ***Disabled***.

Extended BIOS RAM Area

Specify in this option if the top 1 KB of the system programming area beginning at 639K or 0:300 in the system BIOS area in low memory will be used to store hard disk information. The settings are **Top** ***DOS 1K*** or ***0:300***.

System Boot Up Num Lock

When *On*, this option turns off *Num Lock* when the system is powered on so the end user can use the arrow keys on both the numeric keypad and the keyboard. The settings are ***On*** or ***Off***.

Floppy Drive Seek At Boot

When this option enabled, WinBIOS performs a Seek command on floppy drive A: before booting the system. The settings are ***Enabled*** or ***Disabled***.

System Boot Up Sequence

This option sets the sequence of boot drive (either floppy drive A; or hard disk drive C:) that WinBIOS attempts to boot from after POST completes. The settings are ***C: , A:*** or ***A:, C:***.

System Boot Up CPU Speed

This option sets the speed of the CPU at system boot time. The settings are ***High*** or ***Low***.

Internal Cache

This option enabled or disabled the 8KB or 16KB internal cache memory in the 486 processor.

External Cache

This option enabled or disabled secondary cache (L2) memory.

Password Checking

This option enables the password check option every time the system boots or the end user runs Setup. If***Always*** is chosen a user password prompt appears every time the computer is tuned on. If ***Setup*** is chosen, the password prompt appears if WinBIOS is executed.

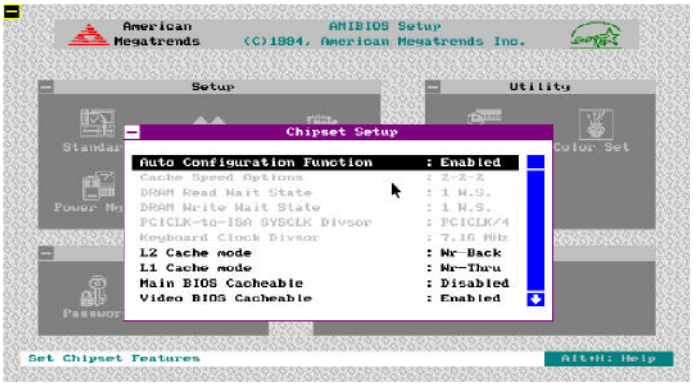
Video Shadow C000, 32K

When this option is set to Enabled, the video ROM area from C0000h ~ C7FFFh is copied (shadowed) to RAM for faster execution. The settings are***Absent, NoShadow***, or ***Shadow***.

Shadow xxxx, 16K,

These options enable shadowing of the contents of the ROM area named in the option title. The settings are***Absent, NoShadow***, or ***Shadow***. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

Chipset Setup



Auto Configuration Function

When this option is ***Enabled***, BIOS automatically configures listed features based on detection of the CPU clock frequency. when this option is ***Disabled***, BIOS leave these features manually adjust by the user.

Cache Speed Options

This feature allows the user to select cache burst read/write cycle : ***2-1-2, 2-2-2, 3-1-3***, and ***3-2-3***. The optimal setting depends on system clock speed.

DRAM Read Wait State

This feature allows the user to set the memory read wait state. The options are ***1, 2***, and ***3 W.S***. The optimal setting depends on system clock speed.

DRAM Write Wait State

This feature allows the user to set the memory write wait state. The options are ***0, 1, 2***, and ***3 W.S***. The optimal setting depends on system clock speed.

PCICLK-to-ISA SYSCLK Divisor

This feature allows the user to select the ISA clock that divide from PCI Clock. The options are***PCICLKI/2, PCICLKI/3***, and ***PCICLKI/4***.

Keyboard Clock Divisor

This feature allows the user to select the keyboard clock that divide from PCI Clock. The options are***PCICLKI/2, PCICLKI/3, CICLKI/4***, and ***7.16MHz***.

L1 Cache mode

This feature allows the user to select the internal cache scheme in processor. The options are***Write-Through*** and ***Write-Back***.

Note : *Intel P24D, P24T, AMD Am486 Enhanced, Am5x86-P75, Cyrix 5x86 support L1 write-back cache.*

L2 Cache mode

This feature allows the user to select the secondary cache scheme. The options are ***Write-Through*** and ***Write-Back***.

Video BIOS Cacheable

This feature allows the user to set whether the video BIOS in C000~C7FF area are cacheable or non-cacheable.

Host-to-PCI Post Write W/S

This feature allows the user to select the**Host to PCI post write** (CPU bus) wait state. The options are*0* and ***1 W.S***.

Host-to-PCI Burst Write

This feature allows the user to set the**Host to PCI Burst write** (CPU bus) enabled or disabled.

I/O Recovery Time Control

This feature allows the user to set the**I/O Recovery Time Control** to delay back-to-back 8 or 16-bit ISA I/O cyclesissued from the PCI master.

Post Write Buffer

This feature allows the user to set the **Post Memory Write Buffer** enabled or disabled. Enabled this feature will enhance system performance.

Bus Park

This feature allows the user to set the **Bus Park** enabled or disabled. Enabled this feature will enhance PCI performance.

1st (2nd, 3rd, 4th) Available IRQ

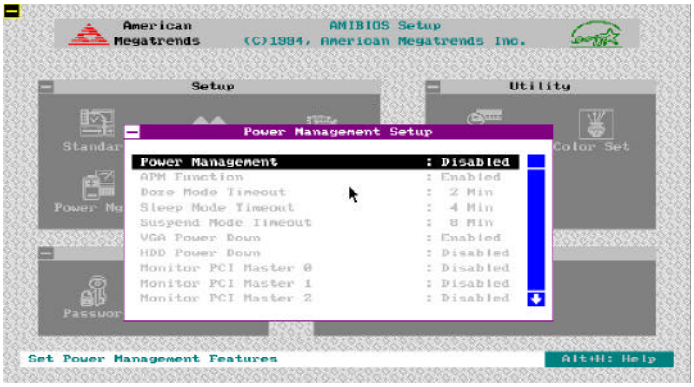
The system BIOS will assign these available IRQs to the first (second/thrid/fourth) found PCI device. The available options are ***5***, ***7***, ***9***, ***10***, ***11***, ***12***, ***14***, and ***15***.

On Board DRAM Option

This feature allows the user to select the on board SIMM DRAM type for 433 main board. The option are ***Normal*** for fast page mode DRAM and ***EDO*** for EDO mode DRAM.

Note : *When EDO DRAM are using, make sure select "EDO" type in this category.*

Power Management Setup



Power Management/APM

This feature allows the user to enable or disable 433 mainboard power management and APM function.

Doze Mode Timeout

This feature specifies the length of time-out of system entering ***DOZE*** mode. The timer options from ***15 sec*** to ***512 min***.

Standby Mode Timeout

This feature specifies the length of time-out of system entering ***STANDBY*** mode. The timer option are from ***2 min*** to ***512 min*** or ***disabled***.

Suspend Mode Timeout

This feature specifies the length of time-out of system entering ***SUSPEND*** mode. The timer option are from ***2 min*** to ***512 min*** or ***Disabled***.

VGA Power Down By

This feature specifies the display screen whether blanking or not when standby or suspend timer is expired.

The option are ***DPMS, Blank, H+V Sync, HV&Blank*** and ***Disalbed***.

HDD Power Down By

This option specifies the length of time of hard disk drive inactivity that must expire before the IDE hard disk drive is placed in IDE HDD Power Down. The settings are from 1 min to 14 min or disabled.

Monitor PCI Master x

Enabling this features, the doze timer start counting if no PCI Master activity is taking place. Disabling this feature, system will not to monitor PCI Master status.

Monitor ISA Master&DMA Activity

Enabling this features, the doze timer start counting if no**ISA Master** and **DMA** activity is taking place. Disabling this feature, system will not to monitor ISA Master and DMA status.

Monitor LPT Port Activity

Enabling this features, the doze timer start counting if no**LPT** port activity is taking place. Disabling this feature, system will not to monitor LPT port status.

Monitor COM Port Activity

Enabling this features, the doze timer start counting if no**COM** port activity is taking place. Disabling this feature, system will not to monitor COM port status.

Monitor IDE Activity

Enabling this features, the doze timer start counting if no**IDE** activity is taking place. Disabling this feature, system will not to monitor IDE status.

Monitor FLP Activity

Enabling this features, the doze timer start counting if no**FLP** (Floppy) activity is taking place. Disabling this feature, system will not to monitor Floppy status.

Monitor VGA Activity

Enabling this features, the doze timer start counting if no**VGA** activity is taking place. Disabling this feature, system will not to monitor VGA port status.

Monitor I/O Region Activity

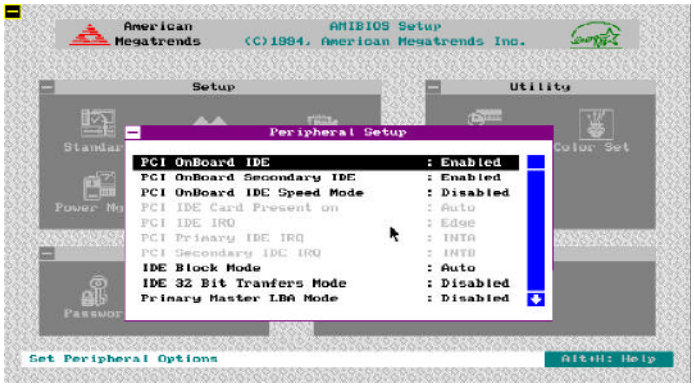
This feature specifies the programmable I/O port address will be monitored. The I/O address range from 100h to 3FFh.

Monitor IRQXX

This feature specifies whether the IRQxx (xx: 1, 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15) will be monitored or not. When system gets into power management mode, any IRQ activities will resume system to ***ON*** mode.

Note: All the monitoring functions work in conjuction with each others. All the specified options have to be met before the power management mode in activated. Then these monitoring function act as the walk-up activities. If activity found on any of the specified option, then the mainboard will exit the power management mode.

Peripheral Setup



Programming Mode

This option enables the BIOS auto detect and configure system peripheral including floppy disk controller, serial ports, and parallel port.

OnBoard FDC

This option enables the use and address of the floppy drive controller on mainboard. The options are***3F1H, 371H,*** and ***Disabled***.

Serial Port1

This option enables the use and address of the first serial port on mainboard. The options are***3F8H, 3E8H***, and ***Disabled***.

Serial Port2

This option enables the use and address of the secondary serial port on mainboard. The options are ***2F8H, 2E8H***, and ***Disabled***.

Parallel Port

This option enables the use and address of the parallel port on mainboard. The options are ***378H, 278H***, and ***Disabled***.

Parallel Port Mode

This feature specifies on-board parallel port mode. The options are ***SPP*** (Standard Parallel Port), ***EPP*** (Enhanced Parallel Port), and ***ECP*** (Extended Capabilities Port).

PCI OnBoard IDE

This feature specifies PCI on-board 2-channel IDE controller be enabled or disabled.

PCI OnBoard IDE Mode

This feature specifies PCI on-board IDE controller's PIO speed mode. The options are ***Mode 1, Mode 2, Mode 3***, ***Mode 4***, and ***Disabled***.

PCI IDE Card Present on

This feature specifies PCI IDE Add-on card are insert on which PCI slot. The options are ***Slot 1, Slot 2, Slot 3, Slot 4***, or leave BIOS ***Auto*** detected. (If this feature is assigned, please disabled ***PCI OnBoard IDE***)

PCI Primary IDE IRQ

This feature specifies PCI IDE Add-on card's primary IDE interrupt to **INTA, INTB, INTC** or **INTD**.

PCI Secondary IDE IRQ

This feature specifies PCI IDE Add-on card's secondary IDE interrupt to **INTA, INTB, INTC** or **INTD**.

PCI Secondary IDE

This feature specifies PCI on-board secondary IDE controller be enabled or disabled.

PCI IDE IRQ Trigger Mode

This feature specifies PCI IDE IRQ triggered mode, the options are ***Edge*** and ***Level***. (This feature only affect PCI IDE add-on card)

IDE Block Mode

If your IDE hard disk drive supports block transfer mode. This feature enable multiple sector reads and writes for IDE drives to enhance data transfer rate. The options are***2, 4, 8, 16, 32, 64, Auto,*** and ***Disabled***.

IDE 32 Bit Transfers Mode

IDE 32-bit transfers will enhance data transfer rate on IDE interface, but only 32-bit PCI IDE controller supports it on this mainboard.

Primary Master LBA Mode

If your primary master IDE hard disk over 528MB, please enables this LBA (Logical Block Addressing) mode feature.

Primary Slave LBA Mode

If your primary slave IDE hard disk over 528MB, please enables this LBA (Logical Block Addressing) mode feature.

Secondary Ctrl Drives Present

This feature specifies how many IDE hard disk drive connect to secondary channel port. The options are***1, 2,*** and ***Disabled***.

Secondary Master LBA Mode

If your secondary master IDE hard disk over 528MB, please enables this LBA (Logical Block Addressing) mode feature.

Secondary Slave LBA Mode

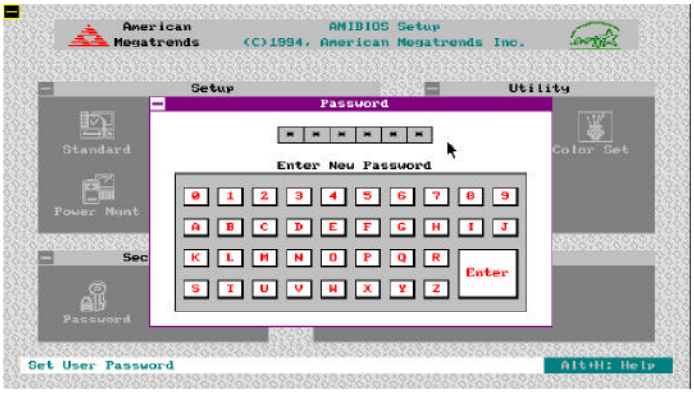
If your secondary slave IDE hard disk over 528MB, please enables this LBA (Logical Block Addressing) mode feature.

NCR SCSI at AD17 Present in

This feature allows the user to set PCI NCR 53C810 SCSI adapter present in which slot.

WinBIOS Password Support

WinBIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when WinBIOS Setup is executed. The following screen appears when you select the password icon.



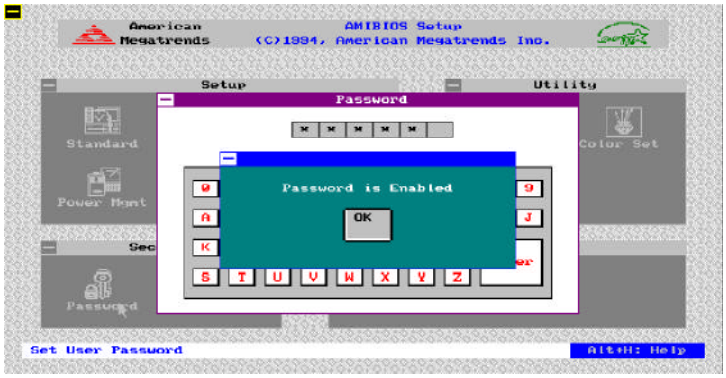
You can enter a password by:

- ❒ typing the password on the keyboard,
- ❒ selecting each letter via the mouse, or
- ❒ selecting each letter via the pen stylus.

Pen access must be customized for each specific hardware platform.

The password check option is enabled in **Advanced Setup** by choosing either *Always* or *Setup*. The password is stored in CMOS RAM.

The password can be from 1 to 6 alphanumeric word. Please make sure the password is noted down. If password is forgotten, the CMOS RAM must be drain and system must be reconfigure. WinBIOS will then display the following:



Selection the Password icon from the Security section of WinBIOS main menu. Enter the password and press <Enter>. The screen does not display the characters entered. After the new password is entered, you will be ask to retype the new password again for confirmation.

If the password confirmation is incorrect, an error message appears. Then please repeat the step above. If the new password is entered without error, press <Esc> to return to the WinBIOS Setup Main Menu. The password is now stored in CMOS RAM after WinBIOS Setup completes. The next time the system boots, you are prompted for the password then.

Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must drain CMOS RAM and reconfigure the system again in order to regain access to the system.

Warning : Retain a safe record of your password. If you've forgotten or loosed the password, the only way to access the system is to clear CMOS memory, please refer to "Clear CMOS" section on chapter 2.

Appendix A

Error Beeps and Message

Error can occur during POST (Power On Self Test), which is performed every time the system is powered on. Fatal errors are communicated through a series of audible beeps. All errors except Beep Code 8 are fatal errors. Fatal errors do not allow the system to continue the boot process. Most displayed errors allow the system to continue the boot process.

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry on the mainboard is faulty.
2	Parity Error	Parity error in the first 64KB of memory.
3	Base 64KB Memory Failure	Memory failure in first 64KB.
4		
5	Timer Not Operational	Memory failure in the first 64KB of memory, or Timer 1 on the mainboard is not functioning.
6	Processor error	The CPU on the mainboard generated an error.
7	8042 - Gate A20 Failure	The keyboard controller (8042) may be bad. The BIOS cannot switch to protected mode.
8	Processor Exception interrupt Error	The CPU generated an exception interrupt.
9	Display Memory Read/ Write Error	The system video adapter is either missing or its memory is fault error.
10	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS
11	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS RAM failed.
	Cache Error/External Cache Bad	The external cache is faulty.

AMIBIOS POST Checkpoint Codes

POST is performed by the BIOS when the system is reset or rebooted. POST performs diagnostics tests on system parts and initialized key system components. When a POST routine completes, a code is written to I/O port address 80h. Display this code by attaching diagnostic equipment to port 80h.

The following POST checkpoint codes are valid for 433 mainboard's WinBIOS.

Codes	Description
01h	Processor register test starting and NMI will be disabled.
02h	NMI is Disabled. Power on delay starting.
03h	Power on delay complete. Checking soft reset and power-on next.
05h	Soft reset and power determined. Enabling ROM next and disabling shadow RAM and cache memory, if any.
06h	ROM is enabled. Calculating ROM BIOS checksum.
07h	ROM BIOS checksum passed. CMOS shutdown register test to be done next.
08h	CMOS shutdown register test done. CMOS checksum calculation to be done next.
09h	The CMOS checksum calculation is done and the CMOS RAM Diagnostic byte has been written. CMOS RAM initialization is next if the *Initialized CMOS At Ever Boot* option is set.
0Ah	CMOS RAM is initialized. The CMOS RAM status register will be initialized for Date and Time next.
0Bh	The CMOS RAM status register has been initialized. Any initialization before the keyboard BAT test will be done next.
0Ch	The keyboard controller I/B is free. Issuing the BAT command to the keyboard controller next.
0Dh	The BAT command was issued to the keyboard controller. Verifying the BAT command next.
0Eh	The keyboard controller BAT result has been verified. Any initialization after the keyboard controller BAT command will be done next.

Codes	Description
0Fh	Initialization after the keyboard controller BAT command is done. The keyboard command byte will be written next.
10h	The keyboard controller command byte has been written. Issuing the keyboard controller pin 23 and 24 blocking the unblocking command next.
11h	Keyboard controller pins 23 and 24 have been blocked and unblocked.
12h	Checked if <Ins> key was pressed during power-on. Disabling the DMA and Interrupt controllers.
13h	DMA controllers 1 and 2 and interrupt controllers 1 and 2 have been disabled. The video display is disabled and port B is initialized. Initializing the chipset and doing automatic memory detection next.
14h	Chipset initialization and automatic memory detection has completed. Next, uncompressing the POST code if the BIOS has been compressed.
15h	The POST code has been umcompressed. The 8254 timer test is next.
19h	The 8254 timer test has completed. Starting the memory refresh test.
1Ah	The memory refresh line has been toggled. Checking the 15u second ON/OFF time next.
20h	The memory refresh period 30u second test has completed. Starting the base 64KB memory and address line test next.
21h	The address line test passed. Toggling parity next.
22h	Parity has been toggled. The sequential data Read/Write test on the base 64KB of system memory is next.
23h	The base 64KB sequential data Read/Write test passed. Next, setting the BIOS stack and doing any required configuration before the interrupt vector initialization.
24h	The configuration required before vector initialization has been completed. Interrupt vector initialization is next.
25h	Interrupt vector initialization is done. Reading the input port of the 8042 for turbo switch (if any) and clearing the password if the POST Diagnostic switch is on.
26h	The input port of the 8042 has been read. Initializing global data for the turbo switch.
27h	The global data initialization for the turbo switch is down . Any required initialization before setting the video more will be done next.
28h	Initialization before setting the video mode has completed. Setting the monochrome mode and color mode.

Codes	Description
2Ah	The monochrome and color modes have been set. Toggling parity before the optional video ROM test.
2Bh	Finished toggling parity. Passing control for required configuration before optional video ROM check.
2Ch	Processing before video ROM control is done. Searching for optional video ROM and passing control to this ROM, if present.
2Dh	Optional video ROM control is done. Passing control to do any processing after video ROM returns control to POST.
2Eh	Return from processing after the video ROM control. If EGA or VGA video is not found, will do the display memory Read/Write test.
2Fh	EGA/VGA not found. Next, displaying the memory Read/Write test.
30h	The memory Read/Write test passed. Searching for retrace checking next.
31h	Display memory R/W test or retrace checking failed. Performing the alternate display memory Read/Write test next.
32h	The alternate display memory Read/Write test passed. Searching for alternate display retrace checking next.
34h	Video display checking over. The display mode will be set next.
37h	Display mode set. Display the power on message.
39h	New cursor position read and saved. Displaying the *Hit <DEL>* message next.
3Bh	The *Hit <DEL>* message has been displayed. The virtual mode memory test is next.
40h	Preparing the descriptor tables next.
42h	The descriptor tables have been prepared. Entering virtual mode for the memory test next.
43h	Entered virtual mode. Enabling interrupts for diagnostics mode next.
44h	Interrupts enabled (if the diagnostics switch is no). Initializing data to check memory wrap at 0:0h.
45h	Data initialized. Checking for memory wraparound at 0:0h and finding the total system memory size.
46h	Memory wraparound test done. Memory size calculation over. Writing patterns in memory to test memory next.
47h	Pattern to be tested written in extended memory. Write patterns in base 640KB memory.

Codes	Description
48h	Pattern written in base memory. Determining the amount of memory below 1MB memory.
49h	
4Bh	Amount of memory below 1MB found and verified. Determining the amound of memory above 1MB next.
4Ch	Amount of memory above 1MB found and verified. Checking for soft reset and clearing the memory below 1MB for a soft reset. (If at power on, go to checkpoint 4Eh).
4Dh	
4Eh	Memory below 1MB cleared. Next, doing a soft reset to clear memory above 1MB.
4Fh	Memory above 1MB cleared via a soft reset. Saved the memory size. Going to checkpoint 52h next.
50h	Memory test started. A soft reset was not done. Displaying the first 64KB memory size next.
51h	The memory size display has started and will be updated during the memory test. The sequential and random memory tests will be performed next.
52h	Memory testing the initialization for the memory below 1MB is complete. Adjust the displayed memory size for memory relocation and shadowing next.
53h	The memory size display was adjusted because of memory relocation and shadowing. The test of the memory above 1MB will be done next.
54h	The testing and initialization of the memory above 1MB has complete. Next, saving the memory size information.
57h	The memory size information has been saved. The CPU registers have been saved. Entering real mode next.
58h	The shutdown was successful and the CPU is in real mode. Disabling the Gate A20 line next.
59h	The Gate A20 address line is disabled. Adjusting the memory size depending on the memory relocation and/or shadowing parameters.
60h	The memory size has been adjusted for memory relocation and/or shadowing. Clearing the *Hit <DEL>* message next.
62h	The *Hit <DEL>* message has been cleared. The *Wait...* message is being displayed. Starting the DMA and interrupt controller tests next.
	DMA page register test passed. The DMA controller 1 base register test is next.
	The DMA controller 1 base register test passed. Starting the DMA controller 2 base register test next.

Codes	Description
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66h	
67h	DMA controllers 1 and 2 have been programmed. Initializing the 8259 interrupt controllers next.
80h	8259 initialization has completed. Starting the keyboard test next.
81h	The keyboard test has started. Clearing the output buffer and checking for stuck keys. The keyboard reset command will be issued next.
82h	
83h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
84h	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
85h	
86h	The keyboard command byte was written and global data initialization has completed. Checking for a locked keyboard next.
87h	
88h	Keyboard locked key checking has completed. Checking for a memory size mismatch with the data in CMOS RAM.
89h	The memory size check has completed. Displaying soft errors, checking for a password, or bypassing WINBIOS and AMIBIOS Setup next.
8Bh	The password as been checked. Doing programming before WINBIOS and AMIBIOS Setup runs next.
8Ch	Programming before WINBIOS and AMIBIOS Setup has completed. Uncompressing the WINBIOS and AMIBIOS Setup code and executing WINBIOS and AMIBIOS Setup next.
8Dh	
8Eh	Returned from WINBIOS and AMIBIOS Setup and screen is cleared. Doing programming after WINBIOS and AMIBIOS Setup next.
	Programming after WINBIOS and AMIBIOS Setup has completed. Display the power-on screen message next.
	First power-on screen message displayed. The Wait ... message is also displayed. Shadowing of the system BIOS and Video BIOS will be done next.
	The system and Video BIOS have been shadowed successfully. Programming system configuration options after WINBIOS and AMIBIOS Setup about to start.
	The WINBIOS and AMIBIOS Setup options have been programmed. The mouse check and initialization will be done next.
	The mouse check and initialization have completed. Resetting the hard disk controller next.

Codes	Description
8Fh	The hard disk controller has been reset. The floppy drive will be configured next.
91h	Floppy configuration is complete. Hard disk configuration will be done next.
94h	Hard disk configuration has complete. Setting the base and extended memory sizes next.
96h	The memory size was adjusted because of PS/2 mouse support and hard disk type 47. Next performing any initialization required before passing control to the adaptor ROM at C8000h.
97h	Initialization before C8000h adaptor ROM control has completed. Checking the C8000h adaptor ROM, then passing control to it next.
98h	C8000h adaptor ROM has passed control back to WINBIOS and AMIBIOS POST. Doing any required processing after C8000h adaptor ROM returns control next.
99h	The initialization required after the adaptor ROM test has completed. Configuring the timer data area and printer base address.
9Ah	The timer and printer base addresses have been configured. Configuring the RS-232 base I/O port address next.
9Bh	The RS-232 base I/O port address has been configured. Performing any initialization required before the coprocessor test next.
9Ch	The required initialization before the coprocessor test has completed. Initializing the coprocessor next.
9Dh	The coprocessor has been initialized. Doing any required initialization after the coprocessor test next.
9Eh	The required initialization after the coprocessor test has completed. Checking the extended keyboard, keyboard ID, and Num Lock key next.
9Fh	The extended keyboard check is done and the keyboard ID flag is set. The Num Lock key has been turned On or Off as specified in WINBIOS and AMIBIOS Setup. The keyboard ID command will be issued next.
A0h	The keyboard ID command was issued. The keyboard ID flag will be reset next.
A1h	The keyboard ID flag has been reset. The cache memory test will be done next.
A2h	The cache memory test has completed. Displaying any soft errors next.
A3h	The soft errors have been displayed. Setting the keyboard typematic rate next.

Codes	Description
A4h	The keyboard typematic rate has been set. Programming the memory wait states next.
A5h	
A7h	The memory wait states have been programmed. Clearing the screen and enabling parity and the NMI next.
A8h	The NMI and parity have been enabled. Performing any required initialization before passing control to the adaptor ROM at E0000h next.
A9h	
AAh	Any required initialization before the E0000h adaptor ROM gains control has been completed. The E0000h adaptor ROM gets control next.
B0h	Control returned to WINBIOS and AMIBIOS POST from the E0000h adaptor ROM. Performing any required initialization after E0000h adaptor ROM control next.
B1h	Any required initialization after the E0000h adaptor ROM had control has completed. Displaying the WINBIOS and AMIBIOS system configuration screen next.
00h	The WINBIOS and AMIBIOS system configuration is displayed. Uncompressing the WINBIOS and AMIBIOS Setup code for hotkey setup next, if required.
	The WINBIOS and AMIBIOS Setup code for hotkey setup has been uncompressed. Copying any required code to a specific area.
	The code has been copied to a specific area done. Passing control to the INT 19h boot loader.

FCC Notice:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used properly. In strict accordance with the manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures :

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/television technician

for help and for additional suggestions.

The user may find the following booklet prepared by the Federal Communications Commission helpful "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office. Washington, DC 20402, Stock o. 004-000-00345-4

FCC Warning

The user is cautioned that changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

Note : In order for an installation of this product to maintain compliance with the limits for a Class B device, shielded cables and power cord must be used.