1.1 General

Toshiba T3100 is a portable personal computer which is compatible with IBM PC and is situated at higher rank of portable computer than Toshiba T2100. It provides many powerful functions in spite of its compact size. Hardware of the T3100, most of IC chips are C-MOS type so that the power consumption is very little (15 W) and Gate Array IC chips are applied so that it is very compact and light weight (6.6 kilogrems).

The T3100 System has following two types.
1. F/F type - Two Floppy Disk Drive.
2. F/H type - One Floppy Disk Drive and one Hard Disk Drive.

The T3100 is composed of System PCB, Keyboard, Plasma Display , 3.5" FDD (Floppy Disk Drive),3.5" HDD (Hard Disk Drive) for only F/H type , Power Supply Unit and case. Plasma Display can display 640 X 400 pixels in graphic mode and 2000 characters in character mode. The 3.5" FDD have capacity of 720KB. The 3.5" HDD have capacity of 10 MB.
The standerd memory size of the T3100 is 640 KB and it is able to extend up to 2 MB with optional Memory Card.
Option unit to the T3100 system which are one Memory Card (2 MB), MODEM Card and Interface Card are capable to be installed in the T3100 System Unit. The optional external unit attached to the system unit is I/O Expansion Box, 5.25" external FDD (Storage capacity of 360 KB 2D) is prepared.
The T3100 has connectors of Color CRT Display port and RS232C port and printer/FDD on the rear panel of the T3100.

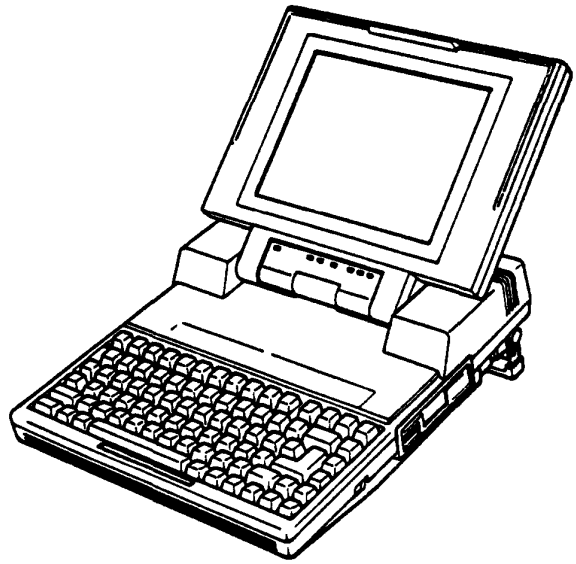
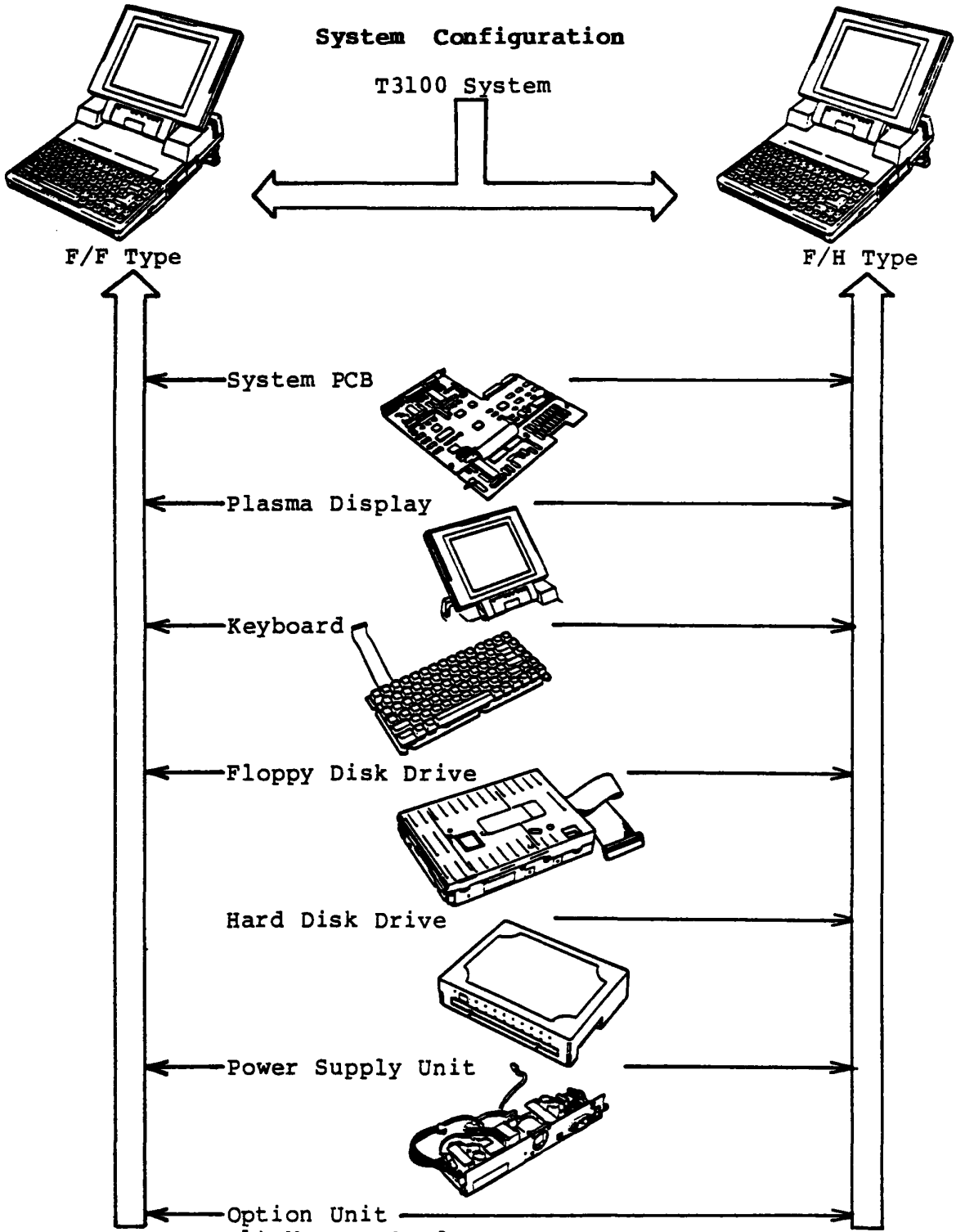


Figure 1-1 T3100 system

System Configuration



1) Memory Card
2) Modem Card
3) I/O Expansion Box and Interface Card
4) External Floppy Disk Drive (2D 5.25")

Configuration Matrix

Modules/Units *Subsystem	Standard	Options
System Unit		
* System Board	1	
CPU		
640KB RAM		
Color/Graphics Controller & Interface		
Floppy Drive Controller & Interface		
Parallel Printer Port		
Keyboard Interface		
* Plasma Display (640 x 400 pixels)	1	
* Keyboard (81 keys)	1	
* Floppy Disk Drive (FDD)		
F/F type ... Two FDD (3.5")	2	
F/H type ... One HDD (3.5") and one FDD (3.5")	1	1
* Hard Disk Drive (HDD)		
F/F type ... Two FDD (3.5")		1
F/H type ... One FDD (3.5") and one HDD (3.5")	1	
* Hard Disk Drive Controller & Interface (Only F/H Type)		
F/F type ... Two FDD (3.5")		1
F/H type ... One FDD (3.5") and one HDD (3.5")	1	
* Power Supply Unit	1	
* Covers	1	
Memory Expansion Board (2 MB)		1
Modem Expansion Board		1
I/O Expansion Box		1
External Floppy Disk Drive (5.25") 2D		1

1.2 System Unit

The T3100 System Unit is composed of subunits. All subunits of T3100 system are built in one compact System Unit case. They are System PCB (Printed Circuit Board), 3.5" FDD (Floppy Disk Drive), 3.5" HDD (Hard Disk Drive) for Only F/H type, Plasma Display , Keyboard, Power Supply Unit and harnesses.
In a maintenance service, the faulty subunit will be replaced with good spare subunits easily.
Followings are showing locations of subunits and connectors for external cables of the T3100 System Unit.

(1) Locations of subunits

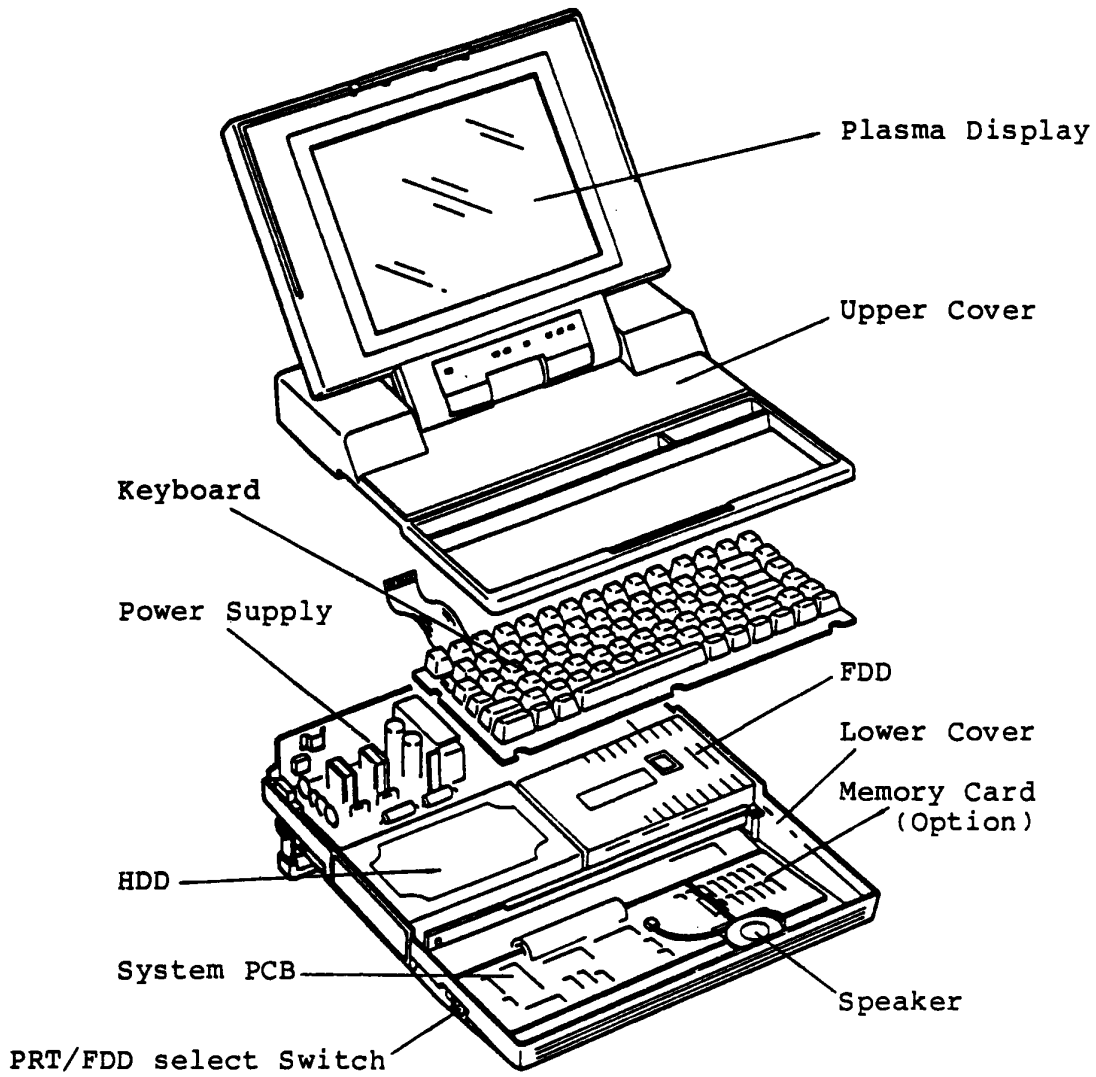


Figure 1-2 System Unit(F/H Type)

continued

The System Unit is to contain the following subunits

System PCB
3.5" FDD (Floppy Disk Drive)
3.5" HDD (Hard Disk Drive) for F/H type
HDC (Hard Disk Controller) for F/H type
Plasma Display
Keyboard
Power Supply Unit
Harnesses
Covers

AC Input power
Voltage : 115V (104-127V) For U.S.A. version
230V (207-253V) For Europe version
Frequency : 50/60 Cycles (49-61 cycles)

(2) Locations of connectors and switches

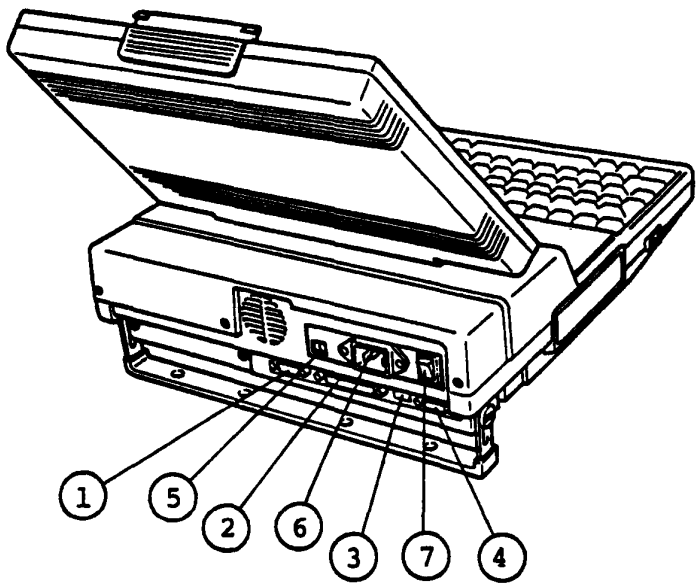


Figure 1-3 Rear view of the T3100

① : RS-232C Connector
② : External FDD and Printer Connector
③ : DIP Switch
④ : Color CRT Display port (RGB)
⑤ : Switch for selection of 115V/230V AC
⑥ : AC jack
⑦ : Power Switch

1.2.1 System PCB

System PCB is composed of processor (i80286), RAM Memory (640KB for Main Memory, 64KB for Video RAM), ROM Memory (64KB for BIOS, 64KB for Character Generater of CRTC), FDD Controller, Keyboard Controller, Display and Printer controller and Printer Adaptor. As the advanced technology, this PCB introduces four "Gate Array" packages .

The System PCB houses;

- Central Processor Unit (CPU; i80286 compatible 16-bit Processor.)
  Clock speed is 4.77 MHz (compatible mode) or 7.16 MHz (turbo mode).
  Switching the clock speeds can be done by depressing some keys of keyboard.
  When the system power turns on, the processor runs at 7.16 MHz.

- Main Memory 640KB dynamic RAM (as standard configuration)

- PCB connector for additional Main Memory (from 640KB to 2640 KB)
  Internal 2 MB memory expansion cards.(Option)

- BIOS ROM (64K-Bytes EPROM) including Initial Reliability Test and Initial Program Loader.

- Programmable Interrupt Controller (PIC; i82C59A compatible)
  Providing eight-level Interrupt Register/Priority Logic, Interrupt Mask and Vector Address

- Programmable Interval Timer (PIT; i82C54 compatible)

- Direct Memory Access Controller (DMAC; i82C37 compatible) for Floppy Disk Controller, Hard Disk controller and serial Input/Output operation.

- Floppy Disk Controller (FDC : TC 8565 compatible)

Continued

- DIP switch (Configuration information for Software)
- BUS Controller (82288 compatible)
  (Bus control, Keyboard control, etc.)
- Clock genarater DMA timing Controller
- BUS driver Gate Array
- Display Controller Gate Array
  (Plasma, RGB-CRT, Composit signal control)
- DMA Controller Gate Array
- Memory Mapper Gate Array
- I/O Controller Gate Array

Continued

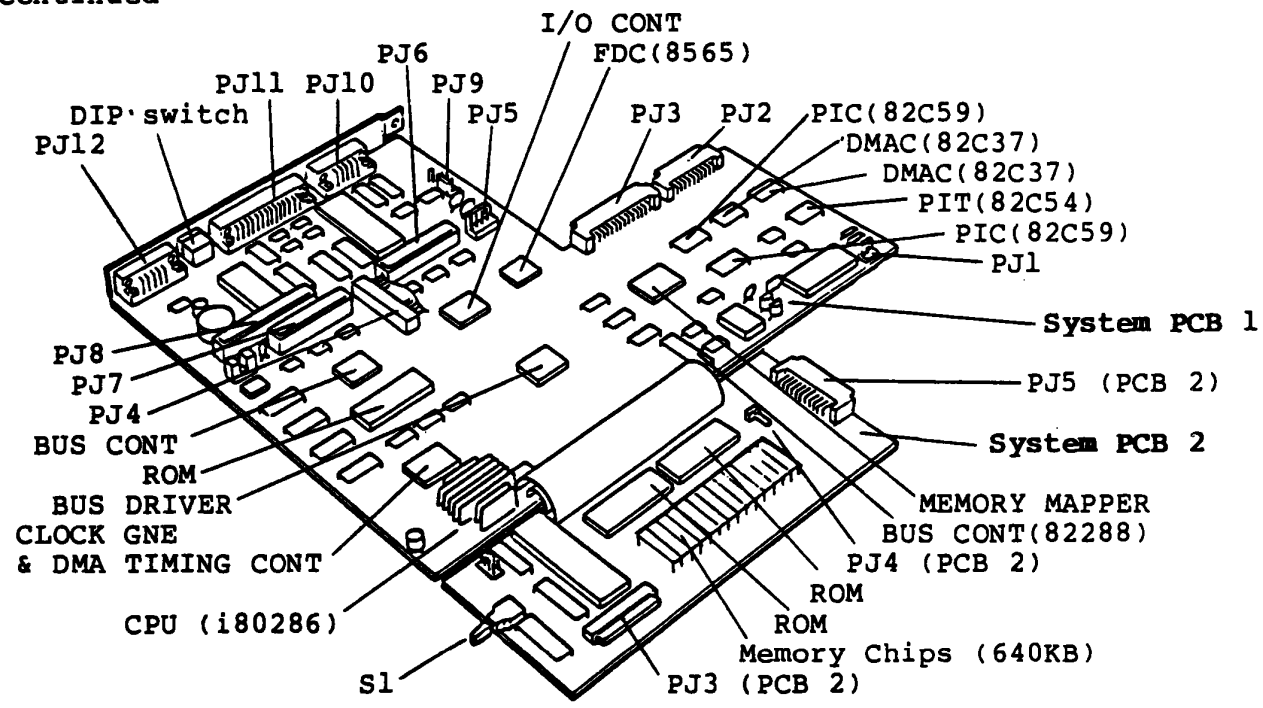


Figure 1-4 System PCB

Connectors

System PCB 1

PJ1 - Battery Connector
PJ2 - Expansion Modem Card or Interface Card Connector
PJ3 - Expansion Modem Card or Interface Card Connector
PJ4 - Plasma Display Connector
PJ5 - Power Supply Controller
PJ6 - FDD 1 Connector
PJ7 - FDD 2 Connector
PJ8 - HDC Connector
PJ9 - Power Supply Connector
PJ10 - RS232C Connector
PJ11 - External FDD and Printer Connector
PJ12 - Color CRT Display Connector

System PCB 2

PJ3 - Keyboard Connector
PJ4 - Speaker Connector
PJ5 - Memory Card Connector

Continued

Configuration switches

The T3100 System Unit Configuration Swicth is 6 pin Dual-In Line Package (DIP) switches.

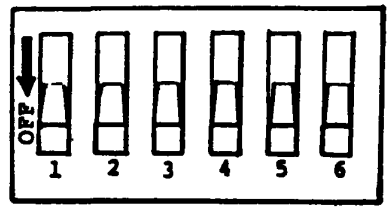


Figure 1-5 DIP switch

The meanings of all Configuration DIP Switch's settings are described in the following tables.

SW	DESCRIPTION
1	Switch over the North European Font ON ..... North European Font OFF ..... Normal
2	Changing the size of DRAM ON ..... 512 KB OFF ..... 640 KB
3	Switching over the external CRTC ON ..... Disable internal CRTC OFF ..... Enable internal CRTC
4	Changing the printer port ON ..... For the port of input or output OFF ..... For the printer port
7	Changing the font of Plasma Display ON ..... For double dots OFF ..... For single dot
6	Changing the port address of internal communication channel ON ..... '2FA' OFF ..... '3FA'

1.2.2 3.5" Floppy Disk Drive (FDD)

The 3.5" FDD is a high performance, high reliable, slim sized Floppy Disk Drive (FDD) for 3.5" floppy disks.
The drive is able to read and write single or double density 3.5" floppy disk with 1M-bytes of recording capacity (unformatted) in double side, double density and 135 TPI.

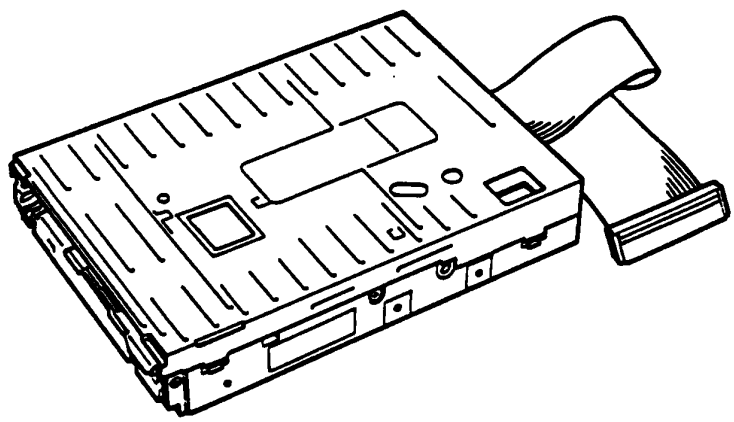


Figure 1-6 3.5"FDD

Performance Specification

Storage Capacity (K-bytes)	
Unformatted	1,000
Formatted	720
Number of Heads/Drive	2
Track/Surface (tracks)	80
Data Transfer Rate (K-bits/Second)	250
Access Time (ms)	
Per Track	6
Average (Including Settling Time)	100
Settling Time	15
Head Load Time	0 *(1)
Average Latency Time (ms)	100
Recording Density (Max.)	
Bit Density (BPI)	8,717
Track Density (TPI)	135
Motor Start Time (ms)	500
Rotational Speed (RPM)	300
Recording Method	MFM
Recording disk	3.5" ANSI Standard disk
Weight (g)	460
Size (mm)	101.6(W) X 149.5(D) X 25.4(H)

Note *(1) : Heads have been always loaded in operation mode.

1.2.3 3.5" Hard Disk Drive (HDD)

The JD-3812M of 3.5-inch hard disk drive use simple, compact construction with quartz-locked spindle motor and embedded servo control; high tracking accuracy and excellent stability are assured through state-of-the-art technology. By reducing power consumption and by making the drives extremely resistant to shocks and vibrations while maintaining their ability to exclude contamination, these drives have characteristics that make them ideal for use in a variety of computer applications including portables, wordprocessors and microminiaturized configurations.

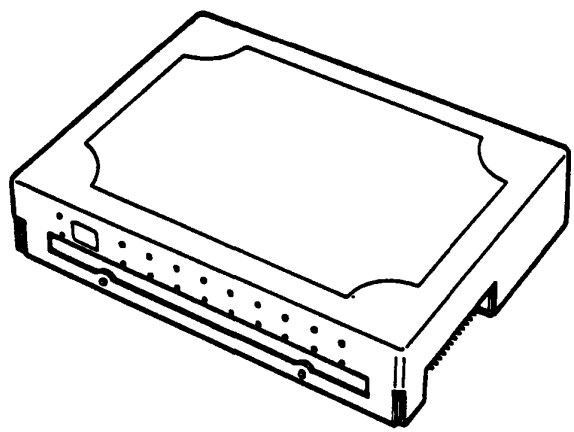


Figure 1-7 3.5" HDD

Performasce Specification of JD-3812M

Storange Capacity		
Unformated		
Per Drive	(M Bytes)	12.65
Per Disk	(M Bytes)	12.65
Per Surface	(M Bytes)	6.33
Formatted		
Sectors per track		17
Per Sector	(Bytes)	512
Per track	(Bytes)	8704
Per Surface	(M Bytes)	5.3
Per Disk	(M Bytes)	10.7
Per Drive	(M Bytes)	10.7
Data Transfer Rate (M bit/second)		3.2
Access Time		
Minimum	(m sec.)	8
Average	(m sec.)	100
Maximum	(m sec.)	230
Rotation Speed	(RPM)	2322
Recording Method		MFM
Recording Density	(BPI)	12808
Track Density	(TPI)	849
Number of Disks		1
Number of Cylinders		612 + 4
Number of Tracks		1224 + 8
Weight	(grms/lbs)	660/1.47

1.2.4 3.5" Hard Disk Controller (HDC)

The WD1002A/S-WX2 Winchester Controller is an IBM XT compatible Winchester Controller board designed to interface. The drive interface is based upon the Seagate Technology ST506. The drives need not be of the same capacity or configuration. All necessary receivers and drivers are included on the board to allow direct connection to the drive(s).

The WD1002A/S-WX2 interfaces directly with the T3100 I/O bus via several interface busses. Data transfer to or from the Controller can be either programmed I/O or DMA.

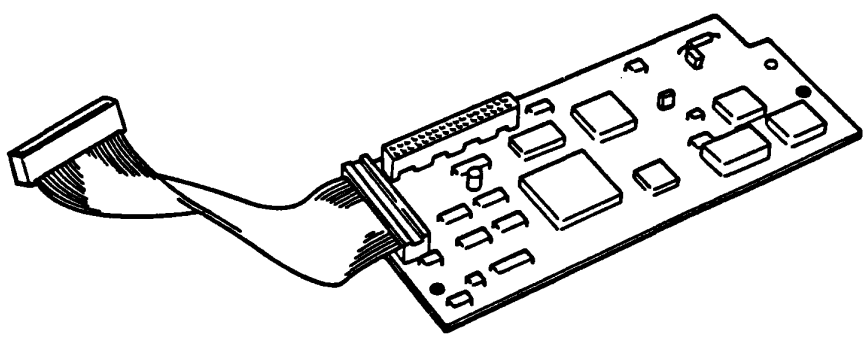


Figure 1-8 3.5" HDC

Specification of WD1002A/S-WX2

Drive interface	
Encoding Method	MFM
Cylinders per disk	Up to 1024
Number of head	Up to 8
Sector per track	Up to 17
Step Rate	70,200 or 3000 us
Data transfer rate	5 Mbits/Sec
Host interface	
Type	IBM XT
Power	+5V $\pm$ 5%, 2.0A max

1.2.5 Keyboard

The keyboard consists of keytops & Keyswitches (81) and matrix circuit, and it is connected to the System PCB through signal cable.
The keyboard controller (80C49AF6) is built in on the System PCB.
It is applied by changing the keytops with option keytops for character differences due to the Nations where the T3100 is used

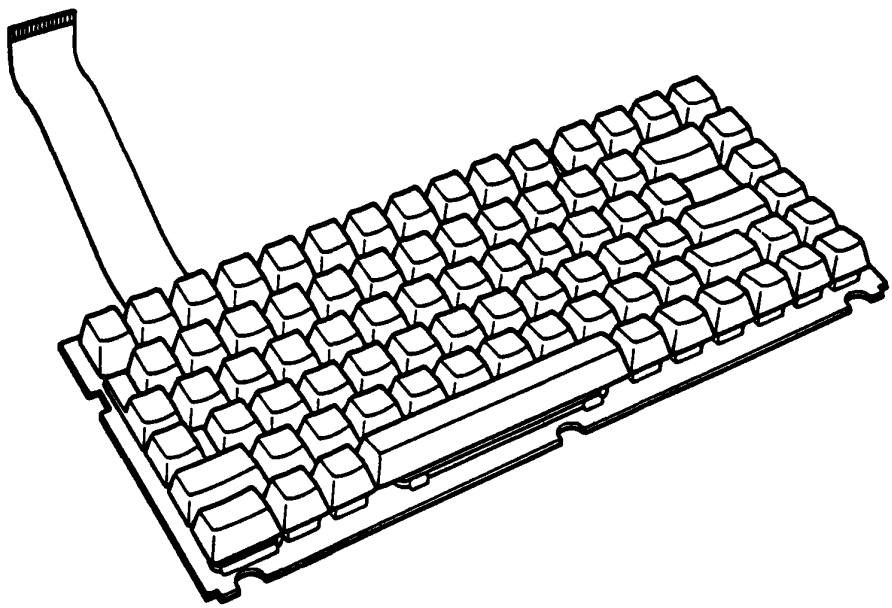


Figure 1-9 Keyboard

1.2.6 Plasma Display

The display is luminescence type flat panel 640X400 pixel Plasma Display.
This Plasma Display can display three type of character sets. (8X8 and 8X16 dots character)
You can see character in the dark for being luminesconce type flat panel, and this picture quality is clearness.

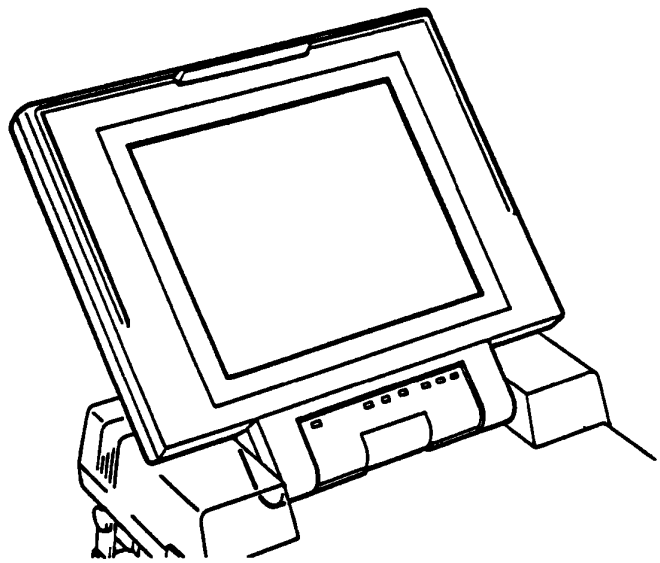


Figure 1-10 Plasma Display

Refresh Cycle (Hz)	60.4
Supply Voltage (volts)	E1 +5V DC ±0.5V E2 -205V DC ±5V *E3 +5V DC ±0.5V
Number of Dot (pixel)	640 (Horizontal) 400 (Vertical)
Dot Size (mm)	0.18 W X 0.22 H
Dot Pitch (mm)	0.30 (Horizontal) 0.36 (Vertical)
Power Consumption (W)	34 Max

Note* : Reference of voltage E3 is E2.

1.2.7 Power Supply Unit

This Power Supply Unit is Housed in System Unit and is designed to support the following:

1) System PCB
2) 3.5" FDD
3) 3.5" HDD (Only F/H type)
4) HDD Controller PCB (Only F/H type)
5) Plasma Display
6) Expansion PCB's

The Power Supply Unit includes the input line filter, line fuse, cooling fan, power conversion circuitry and connectors as following:

System PCB (4 Pin X2)
Plasma Display (3 pin)

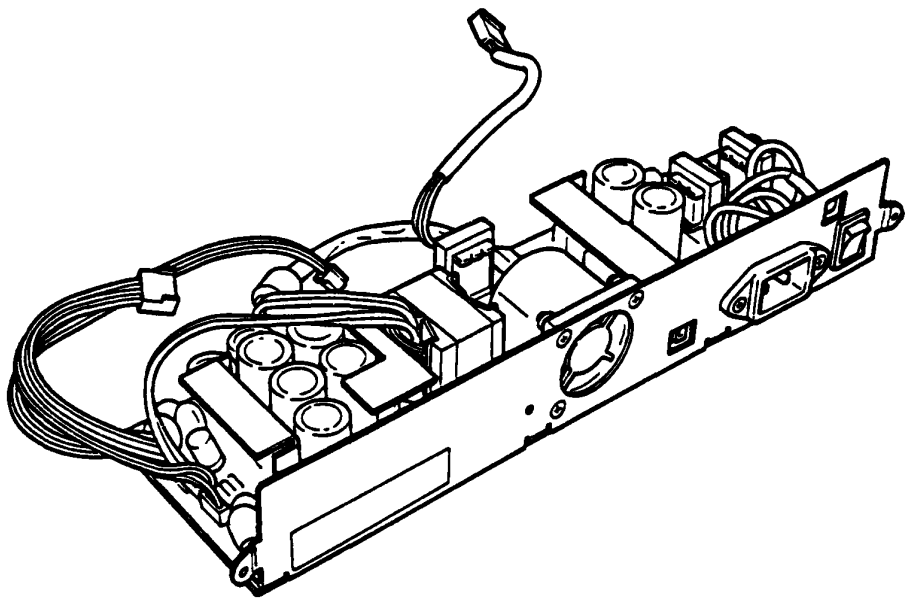


Figure 1-11 Power Supply Unit

Input (AC)	115V (104-127) - For U.S.A. version 230V (207-253) - For Europe version Frequency (50/60 Hz)
Output (DC)	-205V (± 5V) 80mA @ 30 to 150mA +5V (±10%) 60mA @ 20 to 60mA (for Plasma) +5V (± 5%) 3.8A @ 0.5 to 5.6A (for System PCB) +12V (±5%)150mA @ 0 to 250mA -9V (-7.2 -13.2V) 30mA @ 0 to 30mA

1.3 Option Units

The T3100 has a variation of option units to be attached to the System. Following Units are possible to attached to the T3100 System.

1) Memory Expansion Card (2 MB)

2) Modem Expansion Card

3) I/O Expansion Box

4) External Floppy Disk Drive (5.25") 2D

1.3.1 Expansion Memory Unit

The Expansion Memory Unit is an option memory board to be installed on the System PCB. It is installed to the T3100 System Unit just by plugging in the connector on the System PCB and expands the memory size of the T3100 system till 2640KB with the basic 640KB memory.
When the Expansion Memory Unit is installed, the configuration DIP switch must be changed properly. (refer to page 1-10)

WARNING

The Memory chip is very weak in a static electricity shock. When you handle the Expansion Memory board itself, it is recomended to protect the Expansion Memory Unit with anti static electricity materials.

1.3.2 Modem Expansion Card

The Expansion Modem Card is an option card which communicates with an external asynchronous communications device through an appropriate cable having modulatar jacks on both end. One end of the cable is connected to the External Modem Card and other end is to a wall jack of the telephone line.

It supports CCITT V.22 asynchronous mode and BELL 212A. The specifications of this card are as follows.

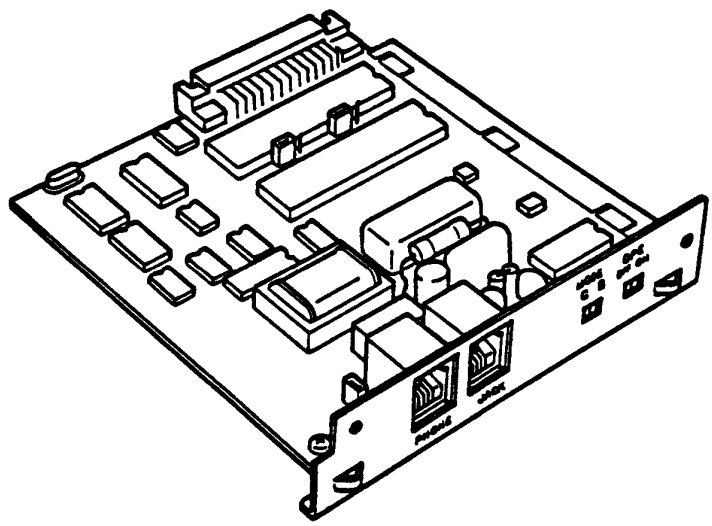


Figure 1-12 Modem Expansion Card

Performasce Specification of Modem Card

Data Format Low Speed(0-300 BPS)	7 or bits, 1 or 2 stop bits odd, even or noparity.
High Speed(1200 BPS)	7 bits, no parity, 2 stop bits 7 bits, e/o parity, 1 stop bits 8 bits, no parity, 1 stop bits
Dialing Capability	Tone Dial / Pulse Dial
Audio Monitor	Speaker
Receive Sensitivity	- 45 dBm

1.3.3 I/O Expansion Box

Expansion Box is an option unit to provide the I/O channel to the T3100 System. This unit is composed of the Expansion I/O Cable, Interface Card, Expansion Box and Ac Power Cord. The Expansion Card, Backpannel Card and Power Supply are in the Expansion Box. Adding an Expansion Box provides five expansion slots.

An option adaptor in the Expansion Box and the System Unit communicates through the Interface and Expansion Cards. The Interface Card is plugged into the EXP sockets at the rear of System Unit. This card is connected to the Expansion Card in the Expansion Box via a cable having 62-pin D-shell connectors at the both ends. The Expansion Card is mounted one of six Expansion Slots in the Expansion Box.

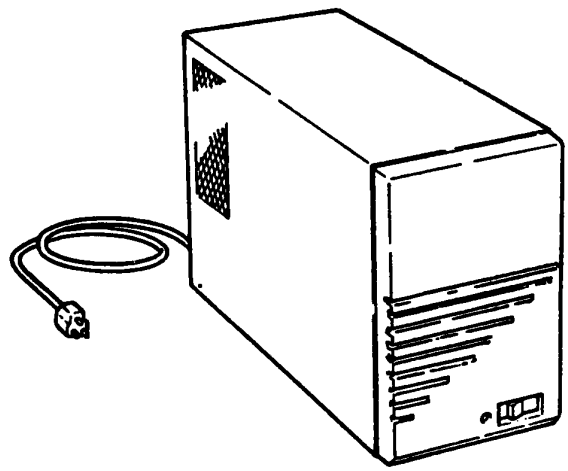


Figure 1-13 Expansion Box

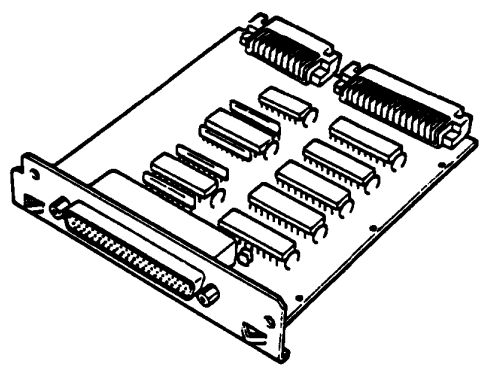


Figure 1-14 Interface Card

1.3.4 5.25" External FDD (SD-521)

The SD-521 is a high performance, high reliable, slim sized Floppy Disk Drive (FDD) for 5.25" floppy disks.
The drive is able to read and write single or double density 5.25" floppy disk with 500KB of recording capacity (unformatted) in double side, double density and 48 TPI.
T3100 system uses the SD-521 as external 5.25" FDD unit (option).

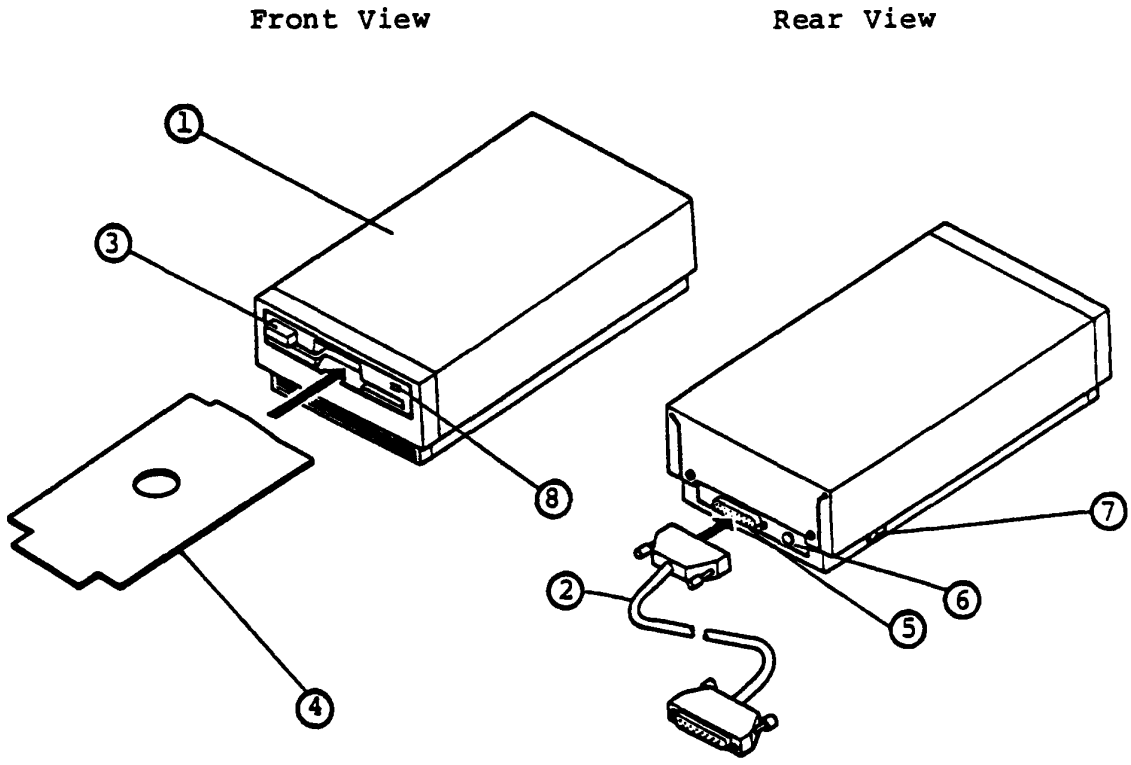


Figure 1-15 5.25" External FDD (SD-521)

Explanations on components

① 5.25" External FDD
5.25" External FDD (Floppy Disk Drive) is composed of Disk Drive and Control PCB.

② Connector Cable
This cable is a signal cable between the FDD and the T3100 System Unit.

③ Disk Eject Button
This button is used to set a disk to the FDD, and to remove a disk from the FDD. Push the button after inserting a disk while disk setting to the FDD, and push the button to eject a disk from the FDD.

④ Cardboard Protector
This cardboard is used for head protection against a shock during a transportation of the FDD.

⑤ DSub-Connector
The DS-Connector is a 25-pin connector for the Connector Cable.

⑥ DC Jack
The DC Jack is for the AC Adaptor.
The required specification of AC Adaptor is
Input : 220-240V ac
Output : 18V dc, 600mA

⑦ Power Switch
Push the rear portion of the switch to Power ON.
Push the front portion of the switch to Power OFF.

⑧ Drive Unit Select Indicator
It is lit while the FDD is selected to use by The T3100 system. Do not eject a disk while it is lit.

Performance Specification of SD-521

Storage Capacity (K-bytes)	
Unformatted	500
Formatted (9 Sectors/Track)	360
Number of Heads/Drive	2
Track/Surface (tracks)	40
Data Transfer Rate (K-bits/Second)	250
Access Time (ms)	
Per Track	6
Average	97
Settling Time	15
Head Load Time	0
Recording Density (Max.)	
Bit Density (BPI)	5,876
Track Density (TPI)	48
Motor Start Time (s)	0.5
Rotational Speed (RPM)	300
Recording Method	MFM

1.4 CRT Display Interface Connector

The T3100 system has CRT Display Interface connector on the back of T3100 System Unit.
You can connect the following types of CRT Display to the T3100 System Unit.

1) Medium Resolution Color Display Unit

320 x 200 pixel's Color CRT Display.
It can display 80 column x 25 line or 40 column x 25 line characters in character mode on one frame.
It can be connected to the T3100 System through D-sub 9-pin connector.

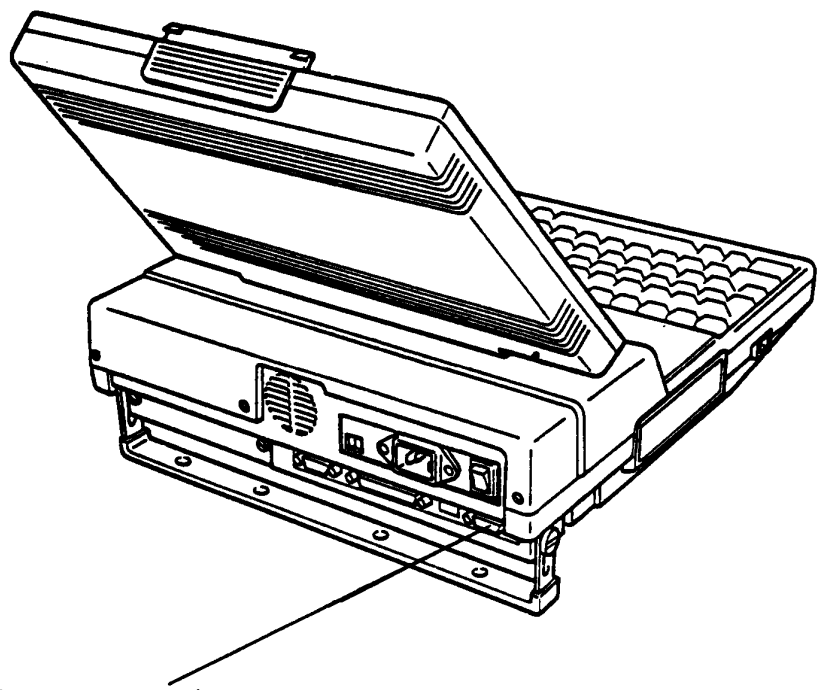


Figure 1-16 CRT Display Interface Connector

Specification

Unit type	
Signal	Description
1.Medium Resolution Color Display Unit	
Connector	9-pin D-sub
Video signal	14.3 MHz (Max) Red video : Positive level TTL compatible Green video: Positive level TTL compatibel Blue video : Positive level TTL compatible
Vertical drive	60 Hz refresh rate 200 scan lines displayed (non-interlace) Positive level, TTL compatibel
Horizontal drive	15.75 KHz scan rate 320/640 pixels displayed Positive level, TTL compatible

PART 2 REQUIRED TOOLS

The following tools and materials are required for the maintenance and repair.

2.1 Standard tools

1) Phillips screw driver
2) Blade screw driver
3) Work Disk
4) MS-DOS System Disk
5) Tweezers
6) Adhesive tape
7) AVO meter

2.2 Special tools

1) Printer Wraparound Connector
2) RS232C Wraparound Connector
3) Printer Port LED
4) AVO meter
5) Alignment Disk
6) FDD Exerciser
7) Cleaning Disk Kit
8) Oscilloscope

PART 3 PREVENTIVE MAINTENANCE

Apply head cleaning to FDDs during every service activity.

You need prepare the Cleaning Disk Kit.

You load the **CE Diagnostic Test Program** , then select the **DISK CLEANING** of **DIAGNOSTIC MENU** .(Refer to PART 8: Test and Diagnostic)

PART 4 TROUBLE ISOLATION PROCEDURE

CONTENTS

This PART is a Trouble Isolation Procedures (TIP's) for the T3100 system .
It is based on the FRU (Field Replaceable Unit) which is defined in **PART 7.** The target of this Trouble Isolation Procedures is to isolate the faulty unit from the system and replace it in the field.

The required tools for this trouble-shooting are as follows.

1). MS-DOS System Disk (including T&D program)

2). Work Disk (for FDD test)

3). AVO meter

4). Cleaning Disk

5). Screwdrivers (Blade screwdriver and Phillips screwdriver)

6). Printer port LED

7). Printer Wraparound Connector

8). RS-232C Wraparound Connector

For the trouble-shooting, you are required to read the T&D operation procedure of **PART 8** of this manual.

You will follow the Trouble Isolation Procedures (TIP's) to isolate the failing Field Replaceable Unit (FRU) in case you met a failure on the FRU of the TOSHIBA Personal Computer T3100. The TIP's are composed of the following groups, and the TIP's in these groups will lead you to failing FRU.

The [ENTRY] is the isolation procedure of which TIP should be taken for the trouble.
Another TIP's are of the units which will be given by [ENTRY], or the suspected units.
Start from next page, for any trouble shooting.

Fault Component (FRU) is identified already ?

1. If fault component (FRU) is identified already, or obvious problem such as unusual noise or damaged part on a component, go to the appropriate TIP (Trouble Isolation Procedure).

TIP	Page
Power On Diagnostic	4-14
Power Supply Unit	4-21
System PCB	4-34
FDD (3.5" Int. FDD)	4-42
HDD (For the option)	4-65
Keyboard	4-75
Display	4-83
External FDD	4-101

2. If fault component (FRU) is not identified, go to next page.

Before the Trouble Isolation Procedure

Set up the system to standard for checking.

1. Turn OFF the power switch of the System Unit.

2. Check that the AC select switch at the rear panel of the System Unit properly reflects the AC commerical power voltage.
   115 V ..... For United States of America version
   230 V ..... For Europe version
   If AC select switch is set different, the Power Supply Unit is broken. Go to Power.

3. Discnnect the all connectors from rear panel, but AC cord.

4. Check that the PRT/FDD select switch at the left side of the System Unit is set to PRT side.

5. Push the Latch of the Plasma Display, then open the Plasma Display.
   And go to **Enter-1.**

LED check

1. Turn ON the power switch of System Unit.
2. Check that the LED(Power/Speed) of indicator lighting.

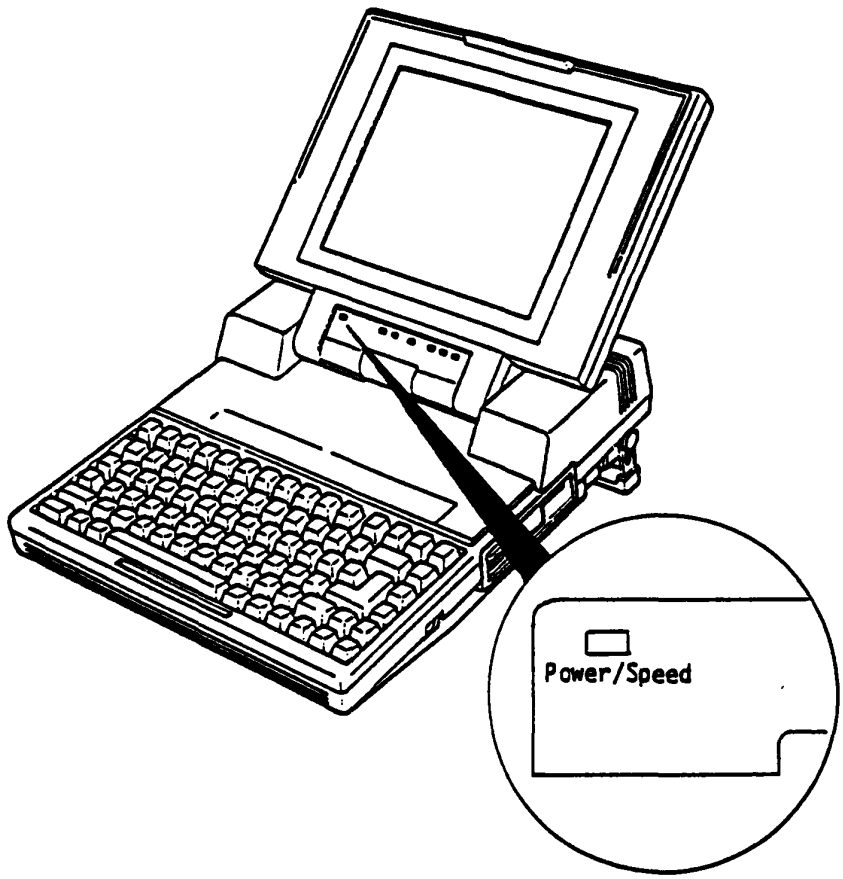


Figure 4-1 LED Check

Is the LED lighting ?

Yes: Go to **ENTRY-2.**

No: Go to **POWER.**
If you have disassembled the System Unit before, confirm that the Indicator cable is connected correctly to the Indicator board.

Cooling Fan chcek

1. Check the fan for not working, strang smell, and noise.

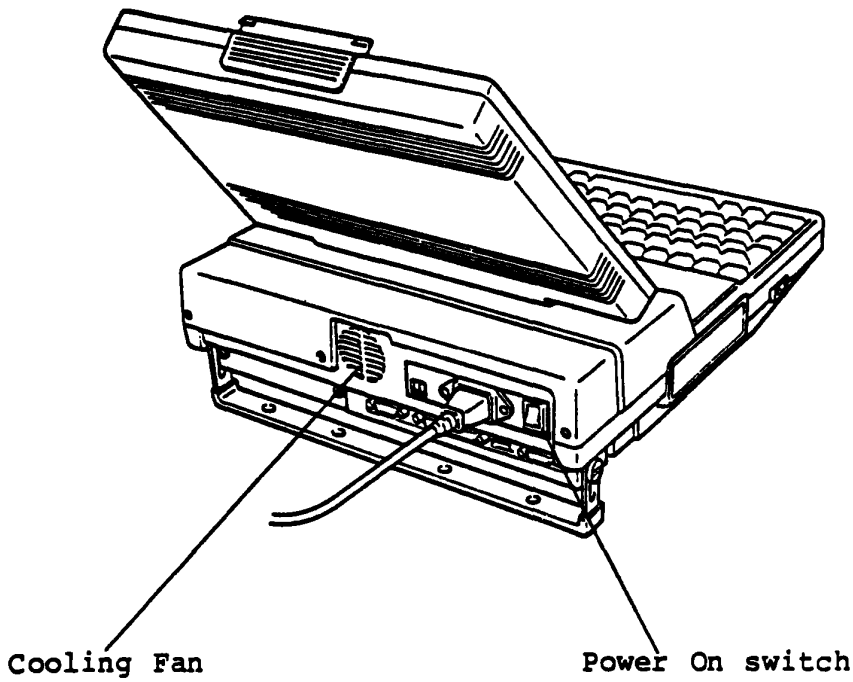


Figure 4-2 Cooling Fan

Is the fan working normally ?

Yes: Go to **ENTRY-4.**

No: Turn OFF the power switch of the System Unit.
Remove the Upper Cover and Power Supply Unit Cover.
(Refer to PART 5)
Confirm that the Cooling Fan connector is connected on the Power Supply PCB.
If the Cooling Fan connector is disconnected, connect them, then repeat the operation to verify it.
If the failuer remains, go to **ENTRY-3** .

Colling Fan voltage check

1. Set the dummy load resister (4.7K ohm, 20W) to Power Supply connector (PJ4).(From pin 1 to pin 3 or from pin 2 to pin 4)
2. Turn ON the power switch of the System Unit.
3. Check the output voltage of 5V (PJ 2) with AVO meter.

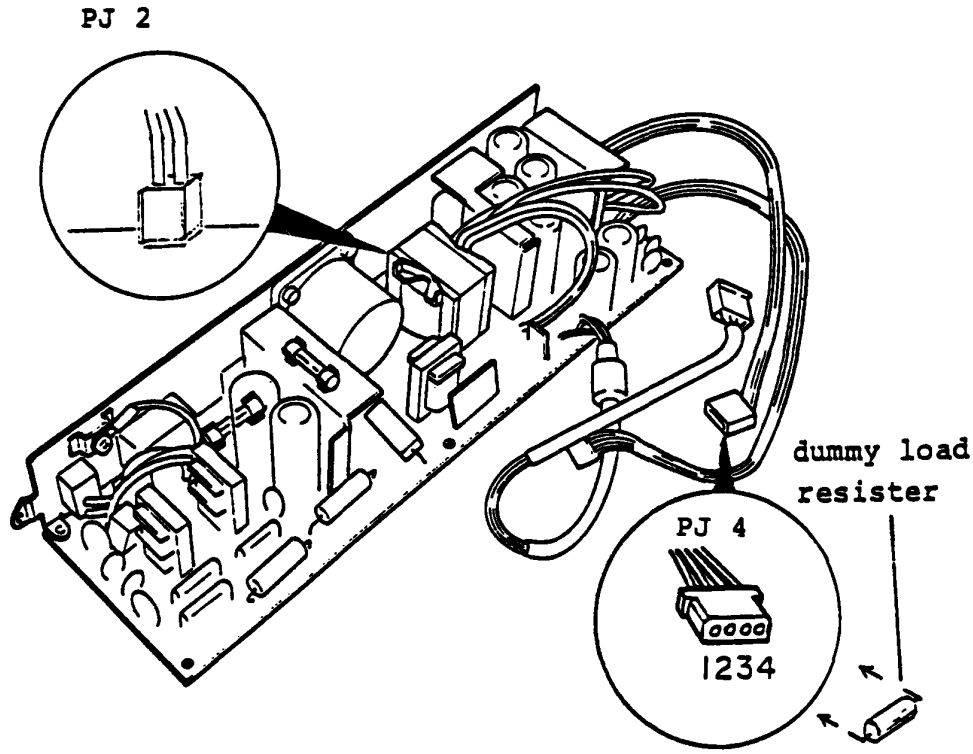


Figure 4-3 Cooling Fan voltage check

Is the output voltage in tolerance ?

Yes: The Cooling Fan may be faulty.
Replace the Cooling Fan (Refer to PART 5), then repeat the operation to verify it.
If the failure remains, the Power Supply Unit may be faulty.
Go to **POWER.**

No: The Power Supply Unit may be faulty.
Go to **POWER.**

Plasma Display check

1. Check that the display indicats all dots for a second momentarily after turning the power ON.

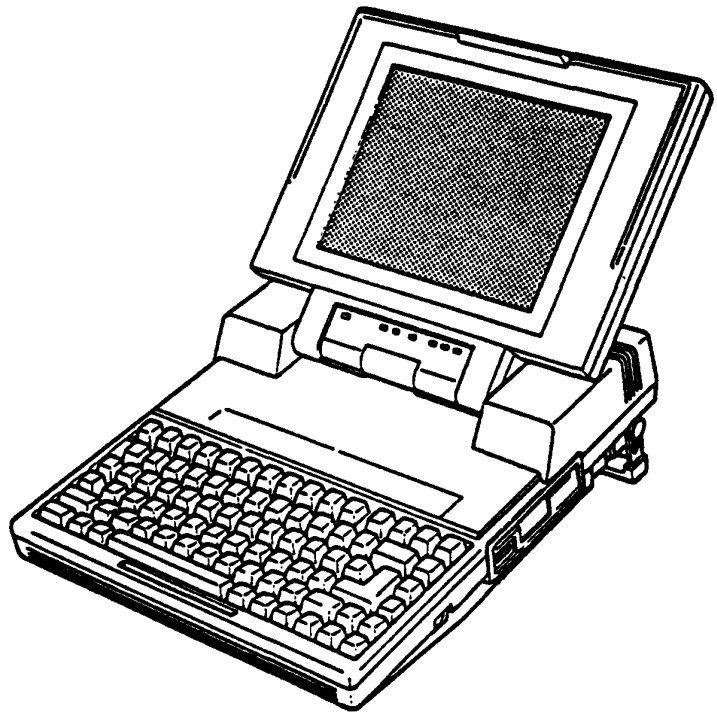


Figure 4-4 Display indicats all dots

Are the above all dots displayed ?

Yes: Go to **ENTRY-5.**

No: The Plasma display may be Faulty.
Go to **PLASMA DISPLAY.**

Screen check at the start up time

1. Confirm that the following message appears on the display screen.

MEMORY TEST XXX KB

Does the above message appear ?

Yes: Go to **ENTRY-6.**

No: The System PCB may be faulty.
Go to **SYSTEM PCB.**

Speaker check

1. After **MEMORY TEST XXX KB** message appears on the display screen, check that Beep sound from speaker.

Figure 4-5 Check the beep sound

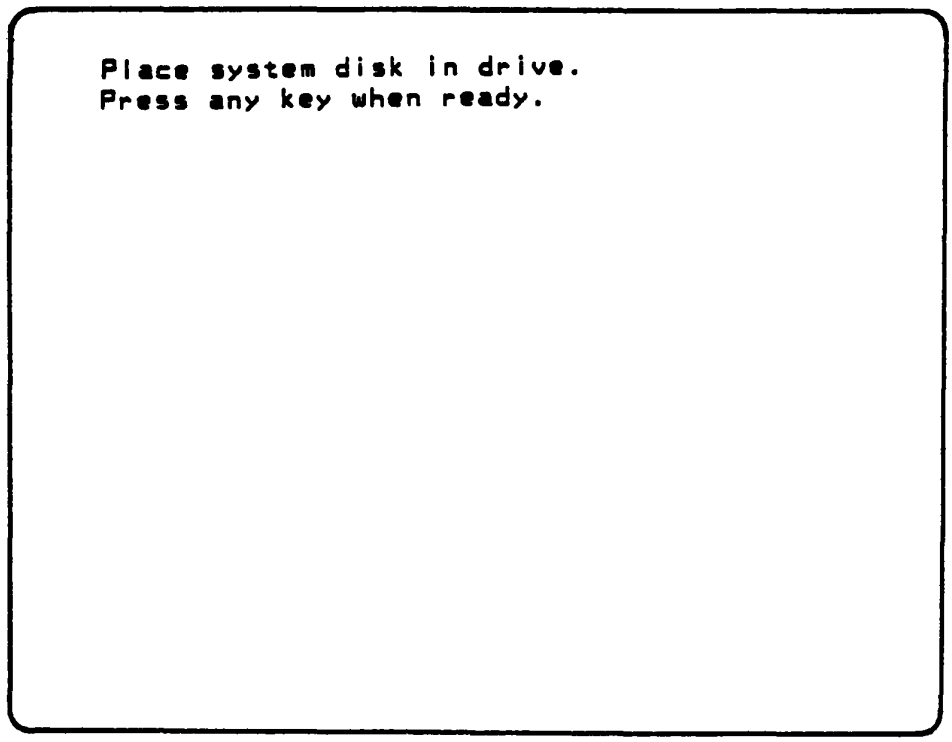
Is the speaker Beep sound ?

Yes: Go to **ENTRY-7.**

No: Turn OFF the power switch of the System Unit.
Disassenble the System Unit cabinet. (Refer to PART 5)
Confirm that the Speaker cable is connected.
Repeat to turn ON the power switch of the System Unit.
If the Speaker cable is connected to System PCB, replace the Speaker Unit with a good spare Speaker Unit.(Refer to PART 5)
If the failure remains, the System PCB may be faulty.
Go to **SYSTEM PCB.**

Message check

1. Confirm that the following message appears on the display screen, about 15 seconds after the Beep sound from the speaker.



Does the above message appear ?

Yes: Go to **ENTRY-8.**

No: You may use a different MS-DOS System Disk.
Replace the good MS-DOS System Disk, then repeat the operation to verify it.
If failure remains, the FDD may be faulty.
Go to **FDD.**
Note: If the MS-DOS system disk has been inserted in the System before the power on , the above massage is bypassed. (Go to **ENTRY-8**)

MS-DOS loading cheak

1. Insert the MS-DOS system Disk into the internal disk drive and press the any key.
2. After the MS-DOS loading, press the "ENTER" twice.
3. Confirm that the following message appears on the display screen.

```
Toshiba  Personal Computer   (RXXXXUS)      Preliminary version

Copyright 1984,86 Toshiba Corporation

MS-DOS   Ver 2.11
Copyright 1983,84 Microsoft Corp.

Command  Ver 2.11V
Current date is  Wed  1-01-1986
Enter new date :
Current time is   0:36:46.00
Enter new time :

A>
```

Does the above message appear ?

Yes: Go to **ENTRY-9.**

No: You may use a damaged MS-DOS System Disk.
Replace the good MS-DOS System Disk, then repeat the operation to verify it.
If failure remains, the Floppy Disk Drive may be faulty.
Go to **FDD.**

Input check

1. Input the file name of **CE DIAGNOSTIC** as **testce** to load the diagnostic program.
   The underlined position on the follow screen are to input **testce** message.

2. Confirm that the **testce** message is inputed on the screen.

```
Toshiba  Personal Computer   (RXXXXUS)      Preliminary version

Copyright 1984,86 Toshiba Corporation

MS-DOS   Ver 2.11
Copyright 1983,84 Microsoft Corp.

Command  Ver 2.11V
Current date is  Wed  1-01-1986
Enter new date :
Current time is   0:36:46.00
Enter new time :

A>testce
```

Is the message inputed ?

Yes: Press the "ENTER" key.
Execute the T&D operation. (Refer to PART 8)

No: Go to **KEYBOARD.**

This section describes how to execute the **POWER-ON DIAGNOSTIC TEST.**

You need to prepare the Printer Port LED (maintenance tool).

POWER ON DIAGNOSTIC TEST is for executing System PCB test.

Go to **POWER-ON DIAGNOSTIC-1.**

Set the Printer Port LED

1. Turn OFF the power switch of the System Unit.
2. Disconnect the all cable except AC cord from the System Unit of rear panel.
3. Connect the Printer Port LED (Maintenance tool) to PRT/FDD connector of the System Unit (rear panel) as shown below.
4. Confirm that PRT/FDD select switch is set to PRT side.

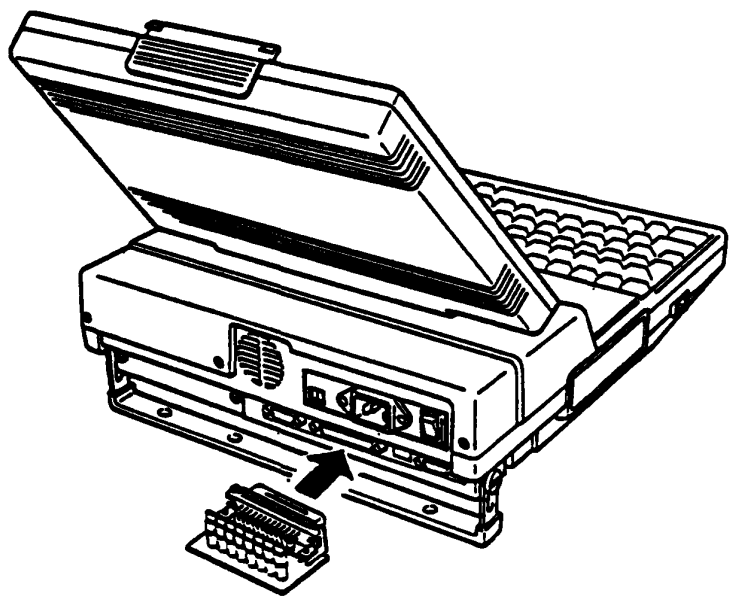


Figure 4-6 Printer Port LED setting

Run the Power-On Diagnostic

1. Turn on the Power switch of the System Unit to run the Power-On Diagnostics.
2. Confirm that the LED of Printer Port LED is lighted.

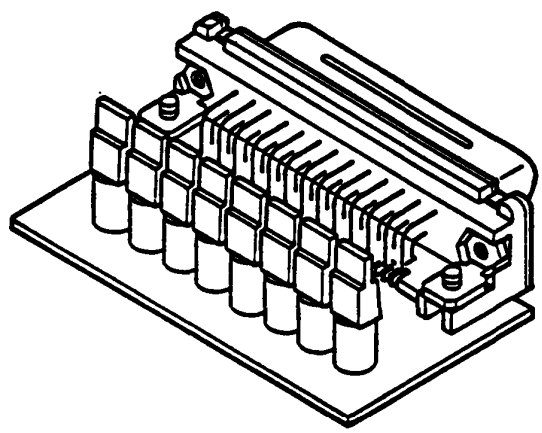


Figure 4-7 Printer Port LED

Is the Printer Port LED lighted ?

Yes: Go to **POWER-ON DIAGNOSTIC-3.**

No: Go to **POWER.**

Read error status and isolate the failre component.

You may have an error condition in the Power-On Diagnostics, and the status has been indicated on the Printer Port LED.
(NOTE) The status **D5(H)** means no error.

1. Read the error status on the Printer Port LED.

2. Isolate the failure component in accordance with the following chart of Power-On Diagnostics.

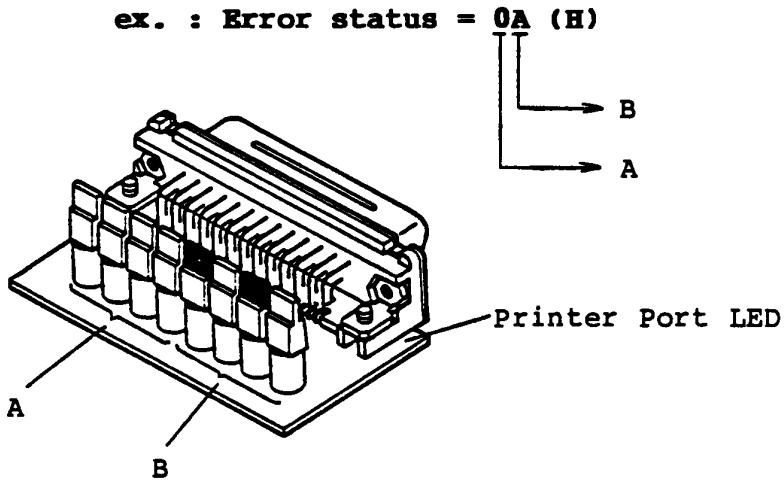


Figure 4-8 Indicat on the Printer Port LED

(order number :

3. In the following flow chart of the Power-On Diagnostics, sequence of the subtest executions is shown by arrow marks. In each subtest, all possible error status and information corresponding the error are described as below.

To be continued.

Read error status and isolate the failure component (Continued)

Status of Printer Port LED

Items	Status
Initial setup of LSI start	01(H)
Initial setup of RTC end	02(H)
Initial setup of PIT end	03(H)
Initial setup of DMAC(#1) end	04(H)
Initial setup of DMAC(#2) end	05(H)
Initial setup of PIC(#1) end	06(H)
Initial setup of PIC(#2) end	07(H)
Initial setup of DMA page resister end	08(H)
Initial setup of KB controller end	09(H)
Initial setup of memory (0 - 64KB) end	0A(H)
Initial setup of memory (64 - 640KB) end	0B(H)
Initial setup of memory (more than 1MB) Protect mode end	0C(H)
Initial setup of memory (more than 1MB) Real mode end	0D(H)
Check a checksum of CMOS end	0E(H)
Check classfication of CRT end	0F(H)
Check item of CMOS end	10(H)
Initial setup of CRT end	11(H)
Initial setup of Keyboard end	12(H)
Initial setup of Timer end	13(H)
Initial setup of FDD end	14(H)
Initial setup of HDD end	15(H)
Initial setup of option ROM end	16(H)
Initial setup of printer end	17(H)
Initial setup of RS232C end	18(H)
Prepare the boot end	19(H)

To be continued.

Read error status and isolate the failure component (Continued)

Status of Printer Port LED

Items	Status
Memory size error	81(H)
Move to protect mode error (memory size)	82(H)
Disable od address 20 error (memory size)	83(H)
KB controller self test error	84(H)
IBF empty error (KB controller)	85(H)
OBF empty error (KB controller)	86(H)
IBF empty error (memory size)	87(H)
IBF empty error (memory size)	88(H)
IBF empty error (morochrome and color)	89(H)
IBF empty error (keyboard)	8A(H)
IBF empty error (printer)	8B(H)
OBF empty error (printer)	8C(H)
Start MSW error (PE=1)	91(H)
Memory size MSW error (PE=0)	92(H)
Memory test MSW error (PE=0)	93(H)
ROM checksum error	94(H)
RTC data buss error	A1(H)
RTC interrupt error	A2(H)
RTC clock function error	A3(H)
PIT data buss error	A4(H)
PIT channel 2 output error (for buzzer)	A5(H)
PIT clock error	A6(H)
PIT channel 1 output error (refresh)	A7(H)
PIT channel 0 output error (timer interript)	A8(H)
DMAC #1 data buss error	A9(H)
DMAC #2 data buss error	AA(H)
PIC #1 data buss error	AB(H)
PIC #1 data buss error	AC(H)
PIC #2 data buss error	AD(H)
PIC #2 data buss error	AE(H)
DMA page resister data buss error	AF(H)
DMA page resister address error	B1(H)
16 bit - 8 bit change error	B2(H)
Memory test error	B3(H)
Move a protect mode error (memory test)	B4(H)
IBF empty error (memory test)	B5(H)
Disable of address 20 error (memory test)	B6(H)
IBF empty error (memory test)	B7(H)
OBF empty error (FDD test)	B8(H)

To be continued.

Read error status and isolate the failure component (Continued)

Status of Printer Port LED

Items	Status
Memory error (until 64KB) data buss	C1(H)
Memory error (until 64KB) 8 bit - 16 bit	C2(H)
Memory error (until 64KB) a fixed data	C3(H)
Memory error (until 64KB) address	C4(H)
Parity error (until 64KB)	C8(H)
Parity error (until 64KB)	C9(H)
Parity error (until 64KB)	CA(H)
Parity error (until 64KB)	CB(H)
Parity error (until 64KB)	CC(H)
Memory test OK (since 64KB)	D0(H)
Memory error (since 64KB) data buss	D1(H)
Memory error (since 64KB) 8 bit - 16 bit	D2(H)
Memory error (since 64KB) a fixed data	D3(H)
Memory error (since 64KB) address	D4(H)
Memory address error	D5(H)
Parity error (since 64KB)	D8(H)
Parity error (since 64KB)	D9(H)
Parity error (since 64KB)	DA(H)
Parity error (since 64KB)	DB(H)
Parity error (since 64KB)	DC(H)
VRAM error (monochrome)	E1(H)
VRAM error (color/plasma)	E2(H)
VRAM error (plasma)	E3(H)
CRTC error (monochrome)	E4(H)
CRTC error (color/plasma)	E5(H)
FDC error	E6(H)

POWER
(Power Supply Unit)

You have reached this TIP since the Power Supply Unit is suspected of the cause of failure.

You need the good Power Supply Parts and Power Supply Unit for maintenance.
Power Supply Parts name is following:

Diode	1S1853 *4
	3DH61
Resister	2.2 ohm 5 W
Transistor	2SC3261
	2SC3346
	2SC366
IC	TA78005
	TL431C
Dummy load	2 ohm 20 W and 4.7K ohm 20 W
Controller	UA1

The symptom may be one of follows.

1) No character is on the Plasma Display.

2) No LED is on the Printer Port LED.

3) Power/Speed indicator could not be off.

4) Error status is disappeared on the Printer port LED.

Go to **POWER-1** for the symptom 1, 2, 3 or 4 of the above.

AC Power cord check

1. Turn OFF the power switch of the System Unit.
2. Confirm that the AC power cord is connected correctly & securely.
3. Unplug the AC Power cord from the System Unit and wall outlet.
4. Check each line of the AC Power cord for conductibility.

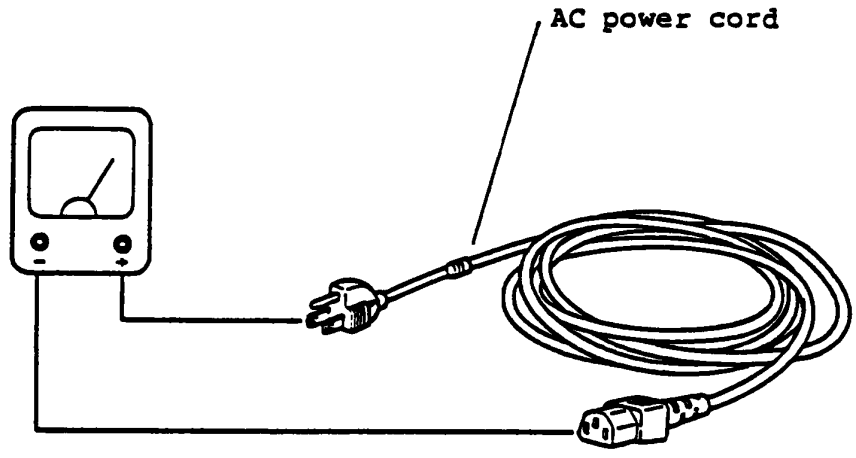


Figure 4-9 AC power cord

Is the AC Power cord free of damage ?

Yes: Go to **POWER-2.**

No: Prepare good AC Power cord. Repeat turn ON the power switch of the System Unit.
If the failure remains, go to **POWER-2.**

Fuse check

1. Remove the Power Supply Unit from the System Unit.
   (Refer to PART 5)

2. Check the fuse of Power Supply Unit with AVO meter.
   Note: Fuse F1 ... AC 125V 3.15A for USA version
   Fuse F2 ... AC 250V 2A for Europe version

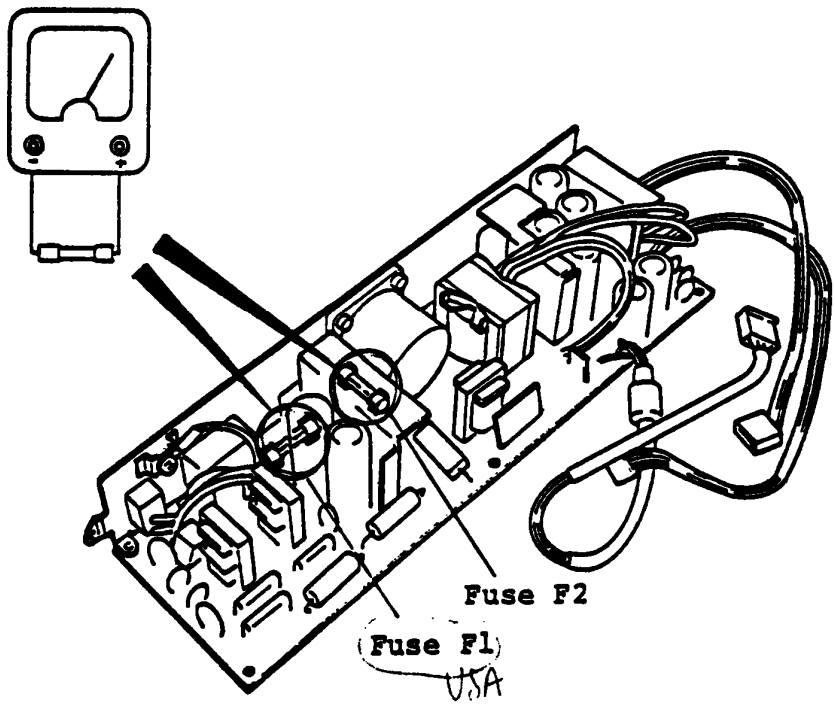


Figure 4-10 Fuse check

Is the fuse good ?

Yes: Go to **POWER-3.**

No: Replace the fuse.
Install the Power Supply Unit, then turn ON the power switch of the System Unit.
If the failure remains, go to **POWER-3.**

Output voltage check

1. Connect the AC cord to Power Supply Unit.
2. Set the dummy load resister (A) (2 ohm 20 W) to the PJ4 of the System PCB power connector. (from pin-1 to 3 or from pin-2 to 4)
3. Set the dummy load resister (B) (4.7K ohm 20 W) to the PJ3 of the System PCB power connector. (from pin-1 to 3)
4. Turn ON the power switch of the Power Supply Unit.
5. Check all output voltage of +205V, +5V, +5V, +12V and -9V DC with AVO meter. (Refer to next page)

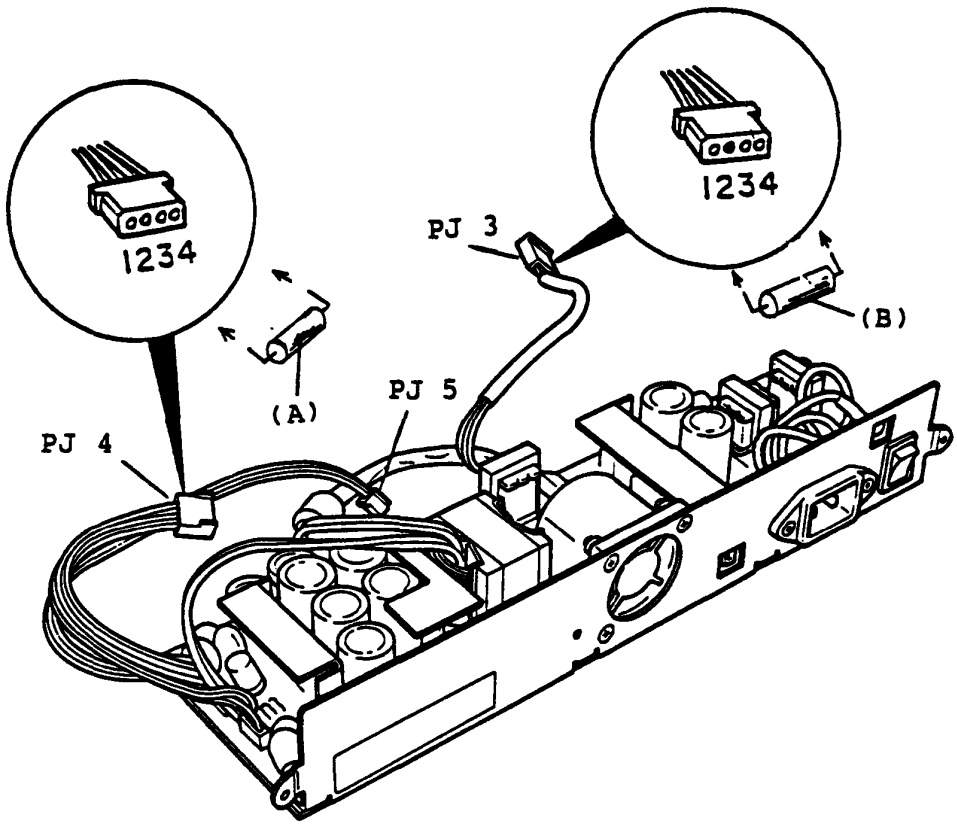


Figure 4-11 Power Supply Unit

To be continued.

Output voltage check (Continued)

System PCB connectors

Connector	Pin		Voltage		
	+lead	-lead	Normal Vdc	Min Vdc	Max Vdc
PJ 4	1	3,4	+ 5	+ 4.75	+ 5.25
	2	3,4	+ 5	+ 4.75	+ 5.25
PJ 5	1	2,4	+ 12	+ 11.4	+ 12.6
	3	2,4	- 9	- 7.2	- 10.8

Plasma Display Panel connector

Connector	Pin		Voltage		
	+lead	-lead	Nomal Vdc	Min Vdc	Max Vdc
PJ 3	3	2	+ 205		
	1	2	+ 5		

Are all output voltages in tolerance ?

Yes: Power Supply Unit is good.

No: In the case of the all voltages are not appeared to AVO meter, go to **POWER-4.**
In the case of the specific voltages are not appeared to AVO meter, obey the following.

+ 205V (PJ3) ⟶ **POWER-7**
+ 5V (PJ3) ⟶ **POWER-8**
+ 12V (PJ5) ⟶ **POWER-9**
- 9V (PJ5) ⟶ **POWER-10**

1. Turn OFF the power switch of the Power Supply Unit.
2. Unplug the AC power cord from the Power Supply Unit and wall outlet.
3. Check the Resister (R1) or transistor (Q1) on the Power Supply Unit PCB with AVO meter.

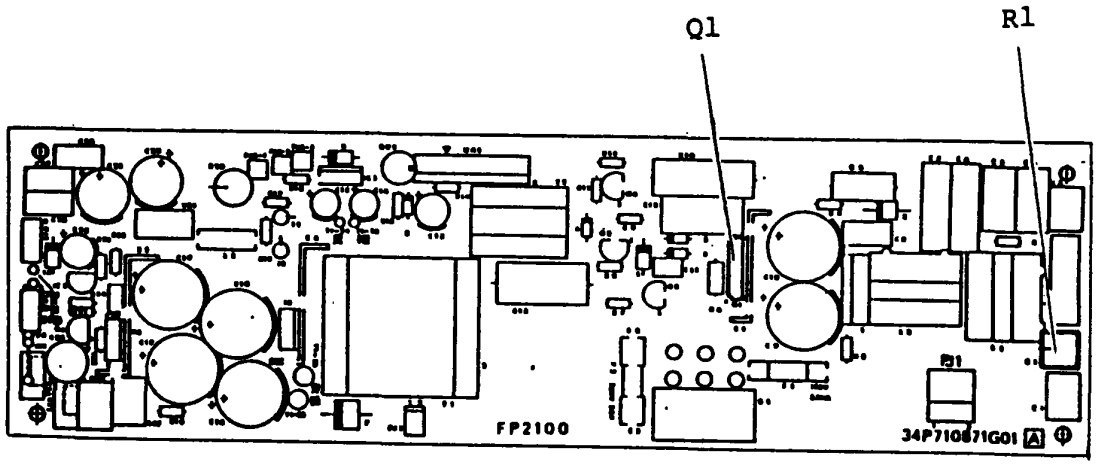


Figure 4-12 Power Supply PCB

Are the load and transistor normal ?

Yes: Go to **POWER-5.**

No: Replace the good spare resister (2.2 ohm 5 W) or transistor (2SC3261), then repeat the voltage check. If the failure remains, go to **POWER-5.**

Power Supply Unit Adjustment

1. Voltage of + 5V is adjustable.
   If it is out of tolerance, adjust it with AVO meter.
   (Refer to PART 5)

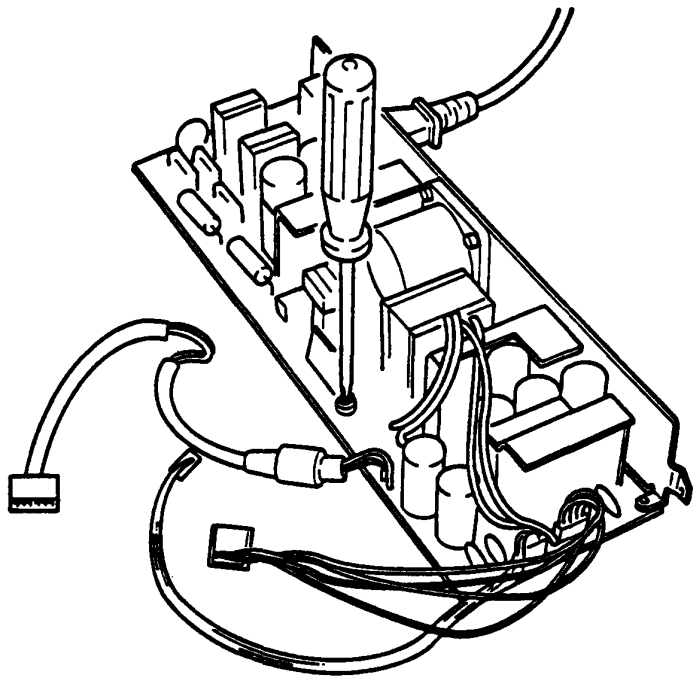


Figure 4-13 Power Supply Adjustment

Are the voltages in tolerance ?

Yes: Repeat the operation to verify. If the failure remain, go to **POWER-11.**

No: Replace the Controller (UA1) on the Power Supply PCB, then repeat the voltage check.
If the voltages (+ 5V) in tolerance, repeat the all voltage check for switing regulator.
If the failure remain, go to **POWER-6.**

In the case of + 5V (PJ4)

1. Turn OFF the power switch of the Power Supply Unit.
2. Unplug the AC power cord from the Power Supply Unit and wall outlet.
3. Check the two transistors (Q5, Q6) and IC (IC2) on the Power Supply PCB with AVO meter.

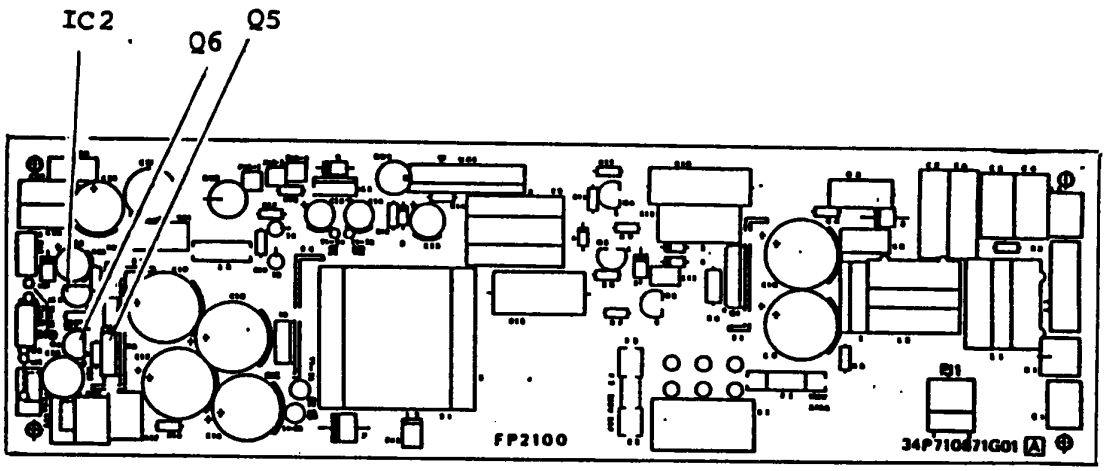


Figure 4-14 Power Supply PCB

Are the transistors and IC normal ?

Yes: Go to **POWER-11.**

No: Replace the transistor (Q5 2SC3346, Q6 2SC336) or IC (TL431C), repeat the voltage check.
If the voltages (+ 5V) in tolerance, repeat the all voltage check for switching regulator.
If falure remains, go to **POWER-11.**

In the case of +205V

1. Turn OFF the power switch of the Power Supply Unit.
2. Unplug the AC power cord from the Power Supply Unit and wall outlet.
3. Check the two diode (CR11,CR12) on the Power Supply PCB with AVO meter.

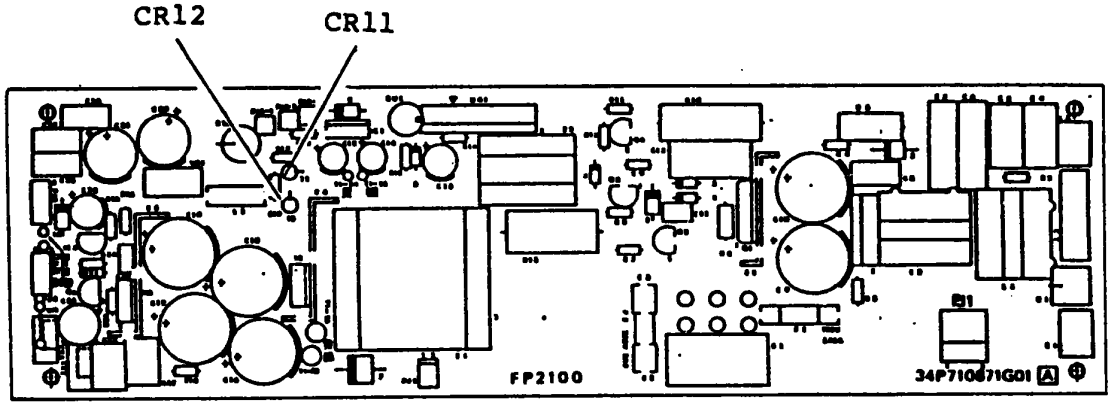


Figure 4-15 Power Supply PCB

Are the diodes nomal ?

Yes: Go to **POWER-11.**

No: Replace the good spare diodes (1S1835), repeat the voltage check.
If the failure remains, go to **POWER-11.**

In the case of +5V (PJ3)

1. Turn OFF the power switch of the Power Supply Unit.
2. Unplug the AC power cord from the Power Supply Unit and wall outlet.
3. Check the diode (CR9) and IC (IC1) on the Power Supply PCB with AVO meter.

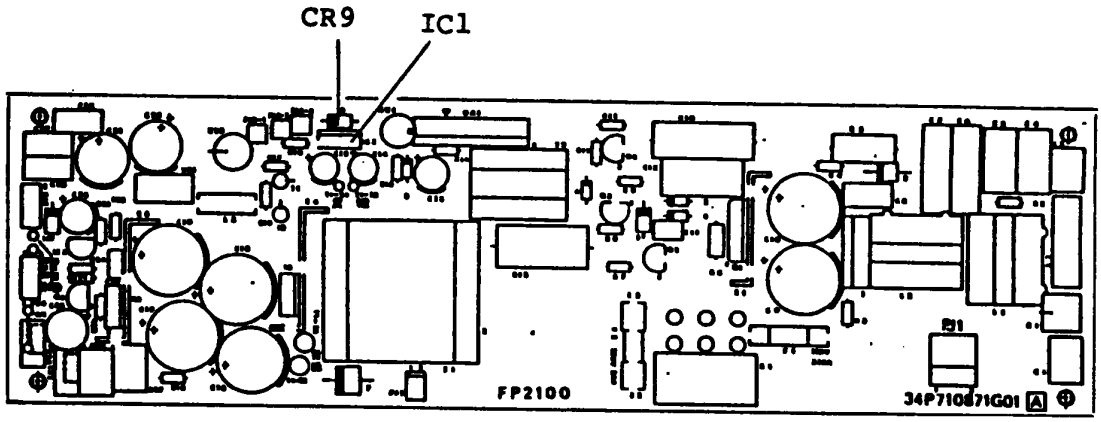


Figure 4-16 Power Supply PCB

Are the diode and IC nomarl ?

Yes: Go to **POWER-11.**

No: Replace the good spare diode (1S1835) or IC (TA78005AP) , then repeat the voltage check.
If failure remain, go to **POWER-11.**

In the case of +12V

1. Turn OFF the power switch of the Power Supply Unit.
2. Unplug the AC power cord from the Power Supply Unit and wall outlet.
3. Check the diode (CR7) on the Power Supply PCB with AVO meter.

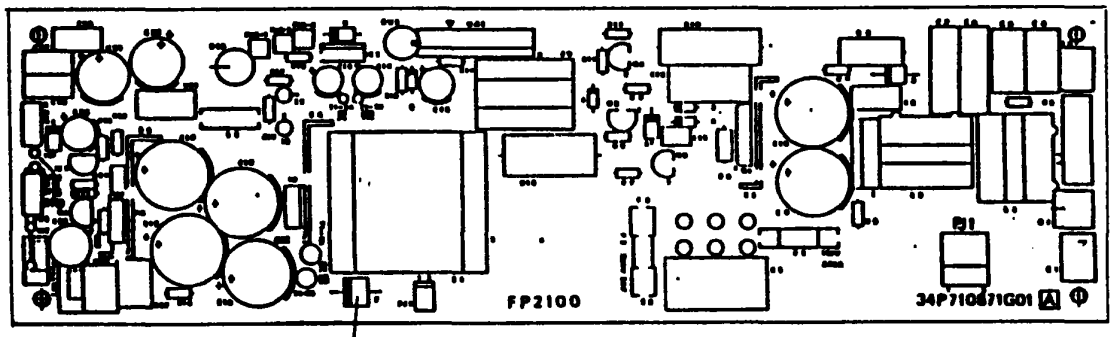


Figure 4-17 Power Supply PCB

Are the diode nomal ?

Yes: Go to **POWER-11.**

No: Replace the good spare diode (3DH61) , then repeat the voltage check.
If the failur remain, go to **POWER-11.**

In the case of -9V

1. Turn OFF the power switch of the Power Supply Unit.
2. Unplug the AC power cord from the Power Supply Unit and wall outlet.
3. Check the diode (CR13) on the Power Supply PCB with AVO meter.

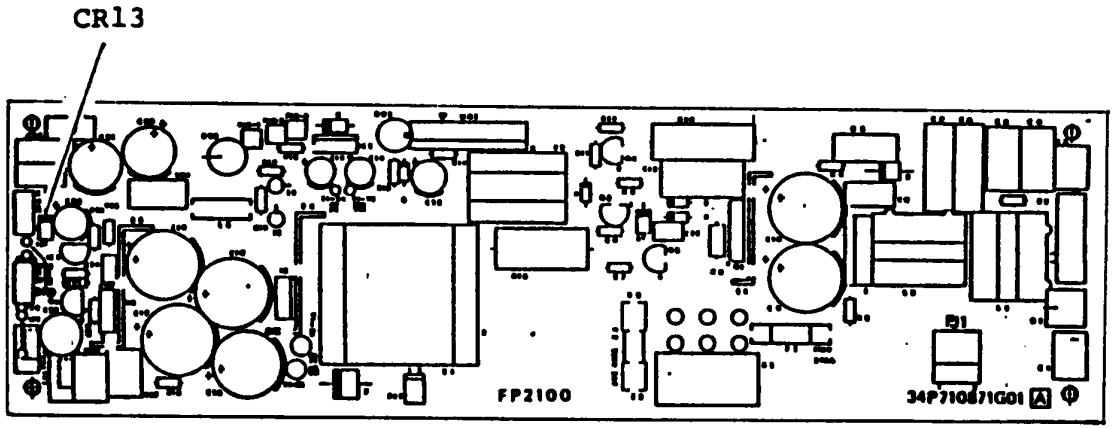


Figure 4-18 Power Supply PCB

Are the diode nomal ?

Yes: Go to **POWER-11.**

No: Replace the good spare diode (1S1853), repeat the voltage check.
If the failure remains, go to **POWER-11.**

Replacement Power Supply Unit

1. Turn OFF the power switch of the Power Supply Unit.
2. Replace the suspected Power Supply Unit with a good spare Power Supply Unit.
3. Turn ON the power switch of the System Unit.
4. Repeat the operation to verify it.

Does the failure remain ?

Yes: The Power Supply Unit is good. Another Unit may be Suspected.

No: The Power Supply Unit is faulty.

You have reached this TIP since the System PCB is suspected of the cause of failure.
You need the Printer Port LED.

The symptom may be one of follows.

1) The Power-On Diagnostics could not run at all.
   No error status is indicated on the Printer Port LED.

2) An error status has been indicated on the Printer Port LED during the Power-On Diagnostics.

Go to **SYSTEM-1** for the trouble shooting of above symptoms.

Set the Printer Port LED

1. Turn OFF the power switch of the system Unit.
2. Disconnect the all connectors from rear panel, but AC cord.
3. Connect the Printer Port LED to the PRT/FDD connector of the System Unit.
4. Confirm that PRT/FDD select switch is set to PRT side.
5. Turn ON the power switch of the System Unit.
6. Check whether the symptom disappears or not.
   (Refer to **POWER-ON DIAGNOSTIC**)

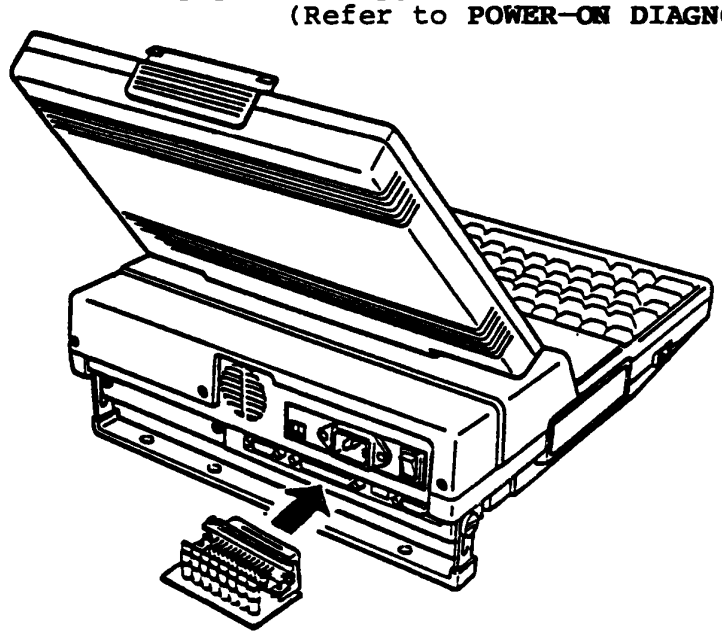


Figure 4-19 Set the Printer Port LED

Does the symptom disappear?

Yes: Failure is the one of separated units.
Connect each separated unit one by one to the System Unit and run Power-On Diagnostics for the failure unit isolation.
Turn OFF the power switch of the all units before making disconnection.

No: Go to **SYSTEM PCB-2.**

Connector check

1. Turn OFF the power switch of the System Unit.
2. Remove the Plasma Display Unit, Upper Cover and Power Supply Unit. (Refer to PART 5)
3. Check the connectors and cables between Power Supply Unit and System PCB are connected correctly & securely.

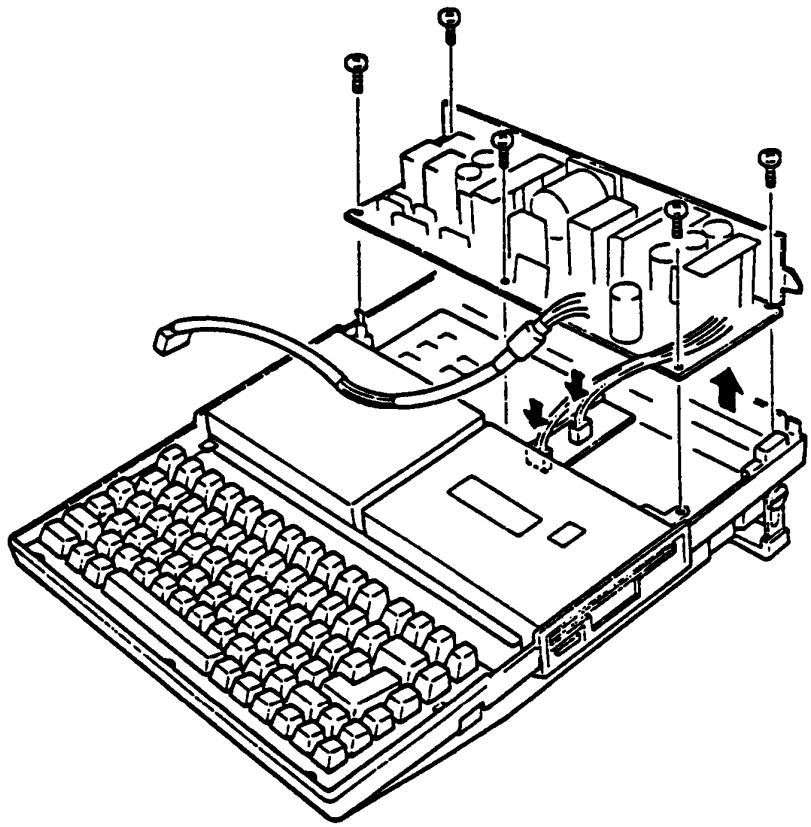


Figure 4-20 Connector Check

Are the connectors and cables connected correctly & securely ?

Yes: Go to **SYSTEM PCB-3.**

No: Correct them, then repeat the opration to verify it.

Remove all option PCB(s)

1. Turn OFF the power switch of the System Unit.
2. Remove all option PCB(s) (Expansion Memory Card and Modem Card or I/O expansion card.)
3. Turn ON the power switch of the System Unit then check the error status on the Printer Port LED.
   (Refer to **POWER-ON DIAGNOSTIC-3**)

Figure 4-21 Option PCB removal

Does the symptom disappear?

Yes: Failure is the one of option PCB(s).
Reinstall each option PCB one by one to the System Unit and run Power-On Diagnostics for the failure PCB isolation.
Turn OFF the power switch of the System Unit before making removal and reinstallation of each option PCB.

No: Go to **SYSTEM PCB-4.**

Disconnect all signal cables

1. Turn OFF the power switch of the System Unit.
2. Disconnect all signal cable connectors of Int. FDD, Plasma Display and Keyboard.
3. Turn ON the power switch of the System Unit, then check the error status on the Printer Port LED.

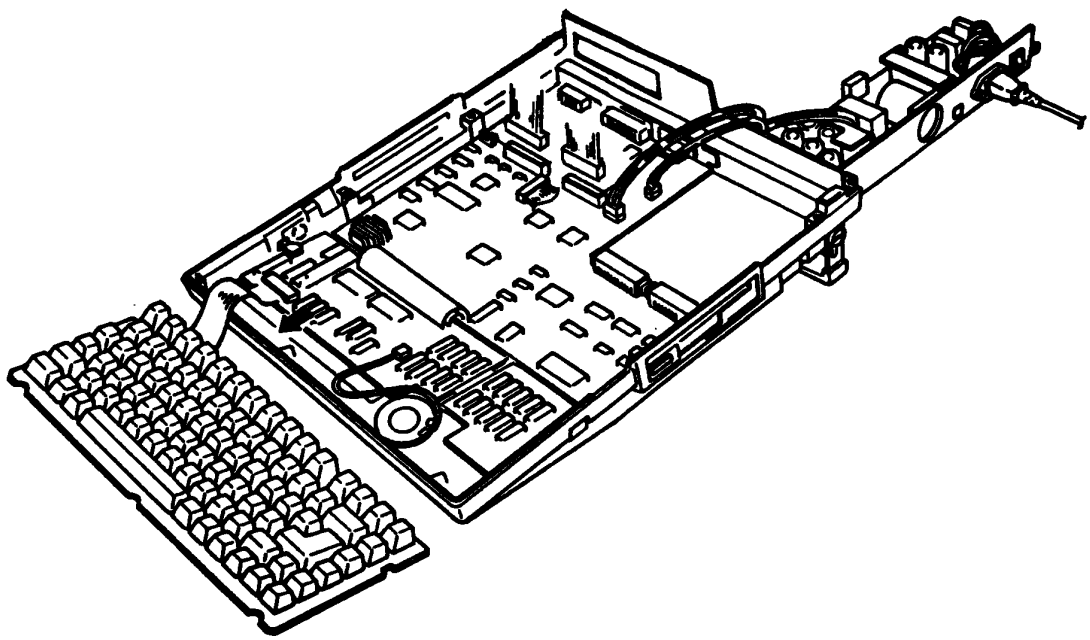


Figure 4-22 Disconnect signal cable

Does the symptom disappear?

Yes: Falure is one of Int. FDD, Plasma Display or Keyboard.
Connect each unit of them one by one to the System Unit and run Power-On Diagnostics for failure unit.
Turn OFF the power switch of the System Unit before each disconnection and connection of unit.

No: Go to **SYSTEM PCB-5.**

Voltage check

1. Turn ON the power switch of the System Unit.

2. Check the voltages at connector pin (PJ 6, PJ 7, PJ 8) with AVO meter. (Refer to next page.)
   Note: Ground point is screw (A).

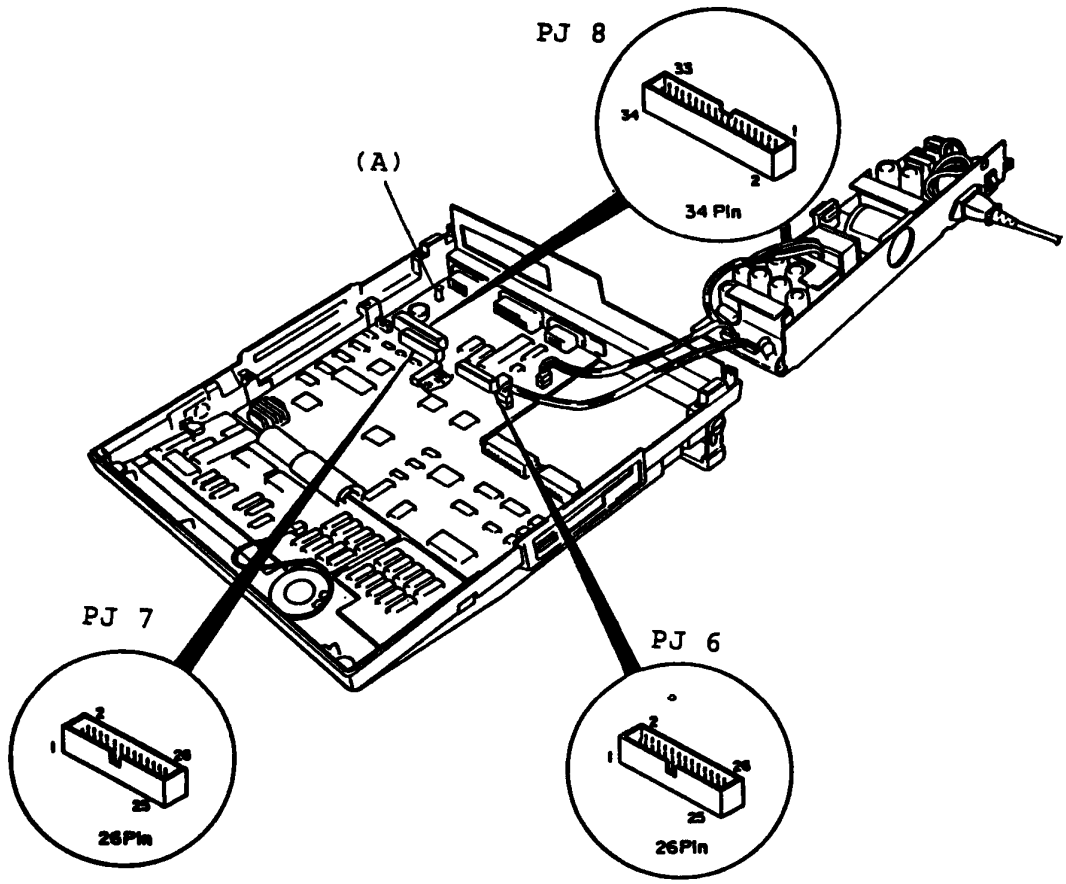


Figure 4-23 Voltage Check

To be continued.

Voltage check (Continued)

Voltage Tolerance

Connector	Pin		Voltage		
	+Lead	-Lead	Normal Vdc	Min Vdc	Max Vdc
PJ 6	1,3,5 7,9	GND	+ 5	+ 4.75	+ 5.25
PJ 7	1,3,5, 7,9	GND	+ 5	+ 4.75	+ 5.25
PJ 8	1,2	GND	+ 5	+ 4.75	+ 5.25
	33,34	GND	+ 5	+ 4.75	+ 5.25
	16	GND	+ 12	+ 11.4	+ 12.6

Is the voltage in tolerance?

Yes: Go to **SYSTEM PCB-6.**

No: Go to **POWER-1.**

System PCB replacement

1. Replace the suspected System PCB with a good spare System PCB.
   Note: Set the Configuration DIP switch. (Refer to page 1-10)
2. Turn ON the Power switch of the System Unit.
3. Repeat the operation to verify it.

Does the failure remain ?

Yes: The System PCB is good. Another Unit may be suspected.

No: The System PCB is faulty.

FDD
(3.5" Intarnal Floppy Disk Drive)

You have reached this TIP since FDD is suspected of the cause of the failure.
For the trouble shooting, you will need one good spare 3.5" Int. FDD for the replacement.
You will need one work disk for Test program and Cleaning disk for head cleaning. Work disk must be formated. (Refer to PART 8)

Before the trouble-shooting, confirm that PRT/FDD select switch of the System Unit is set to PRT position.

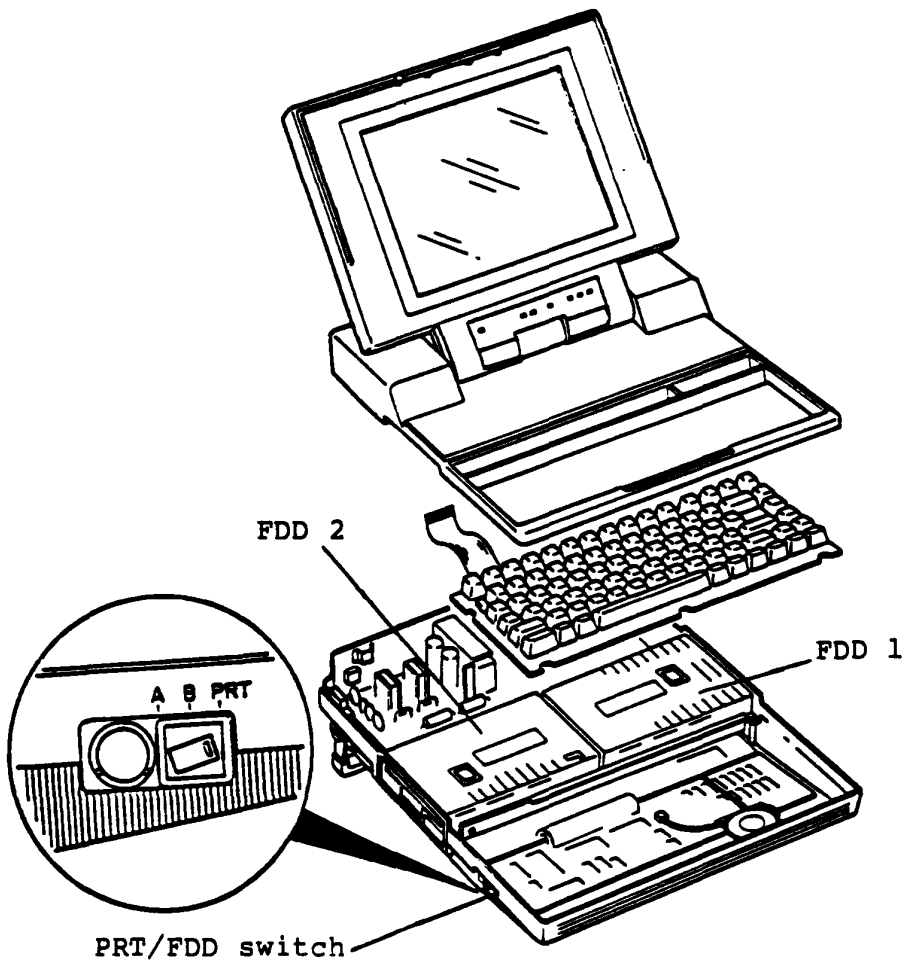
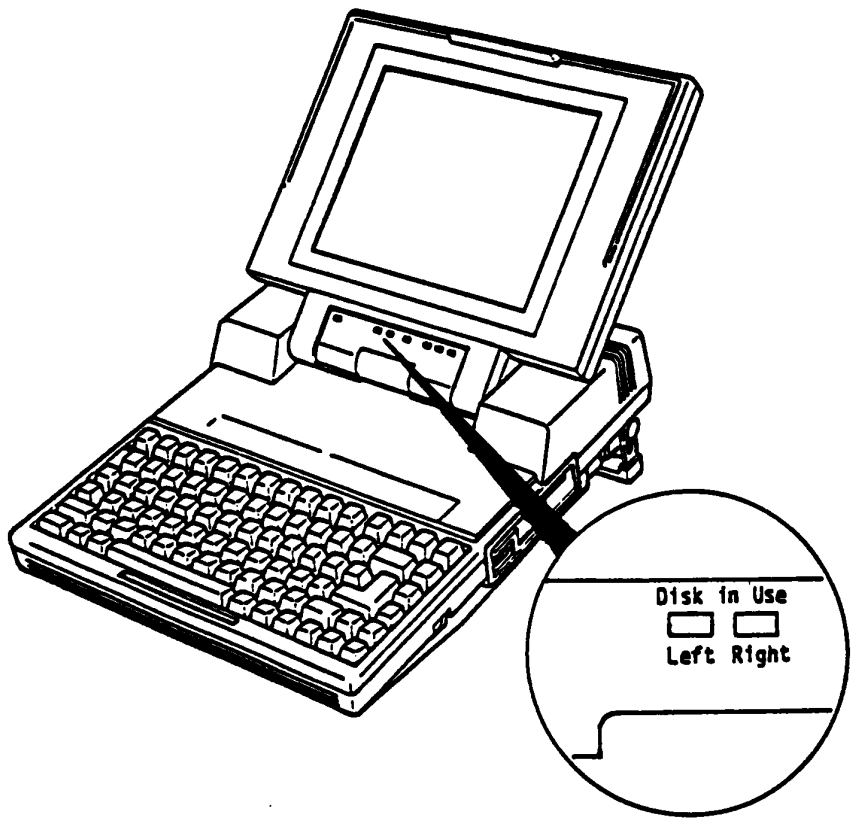


Figure 4-24 T3100 System Unit (F/F type)

LED of FDD Check

1. Turn ON the power switch of the System Unit.
2. Confirm that the Floppy Disk is inserted into the FDD. If the Floppy Disk is inserted into the FDD, remove the Floppy Disk from the FDD.
3. Confirme that both **Disk in Use** (Left/Right) indicators light sequentialy, right indicator light at first, then left indicator light.



Figuren 4-25 LED Check

Is the LED lighting ?

Yes: Go to **FDD-2.**

No: System PCB is suspected. Go to **SYSTEM-PCB** .

The MS-DOS loarding

1. Turn OFF the power switch of the System Unit.
2. Insert the MS-DOS system disk to the internal disk drive, then turn on the power of the System Unit.
3. The MS-DOS is loaded after Power On Diagnostic execution.
4. After the MS-DOS loading, confirm that the following message appears on the display screen.
5. Press the "ENTER" key twice, then input file name of **CE Diagnostic** as **testce** to load the diagnostic program.

```
Toshiba  Personal Computer   (RXXXXUS)      Preliminary version

Copyright 1984,86 Toshiba Corporation

MS-DOS   Ver 2.11
Copyright 1983,84 Microsoft Corp.

Command  Ver 2.11V
Current date is  Wed  1-01-1986
Enter new date :
Current time is   0:36:46.00
Enter new time :

A>testce
```

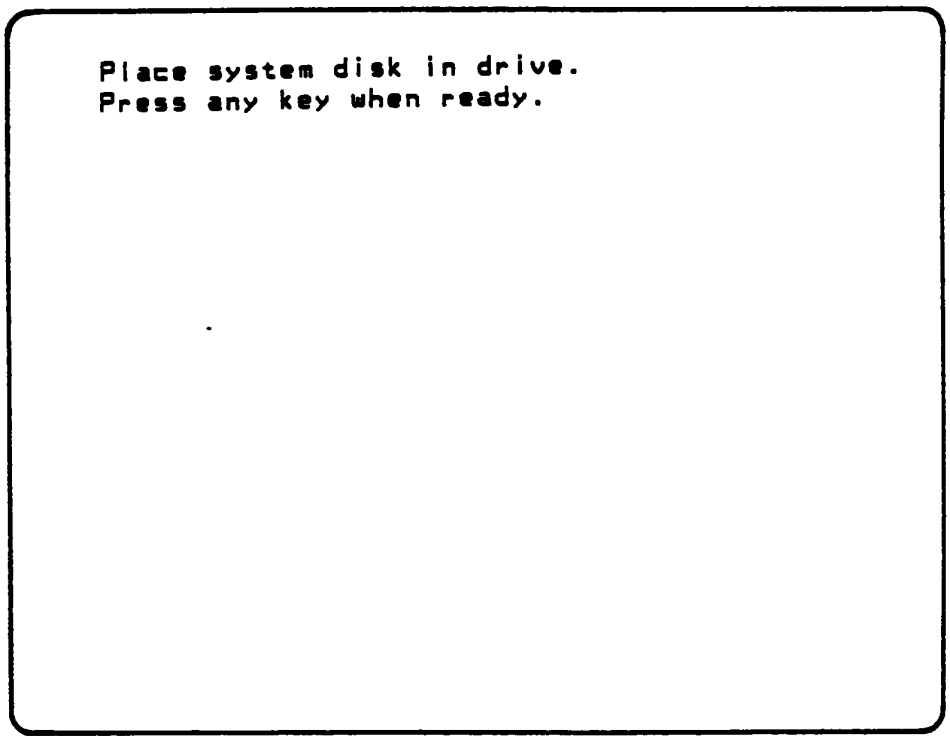
Is the above message displayed?

Yes: The underlined portion on the above screen are for the input **testce** message. And press the "ENTER" key. Go to **FDD-5.**

No: Go to the next page.

The MS-DOS loarding (Continued)

6. Confirm that the following message on the display screen.



Does the above message.appear ?

Yes: You may use a damaged system disk. Prepare the other good MS-DOS system disk, then repeat the turn ON the power switch of the System Unit to verify.
Head of FDD may be dirty. Clean the head of FDD (Refer to **PART 8**).
If the failure remains, go to **FDD-10** (F/H type) or **FDD-4** (F/F type).

No: Go to **FDD-3.**

Prepare the good MS-DOS system disk

1. Turn OFF the power switch of the System Unit.
2. You may use a different system disk.
   Prepare the good MS-DOS system disk.
3. Turn ON the power switch of the System Unit.
4. Confirm that the MS-DOS is loarded. (Refer to **FDD-2**)

Is the MS-DOS loarded ?

Yes: Go to **FDD-5** .

No: Head of FDD may be dirty.
Clean the head of FDD (Refer to PART 8).
Repeat the opration to verify, then if the MS-DOS is loaded, go to **FDD-10** (F/H Type) or go to **FDD-4** (F/F Type).

Use the FDD 2

1. Turn OFF the power switch of the System Unit.
2. Insert the MS-DOS system disk to other FDD (FDD 2).
3. Turn ON the power switch of the System Unit.
4. Confirm that the MS-DOS is loarded. (Refer to **FDD-2**)

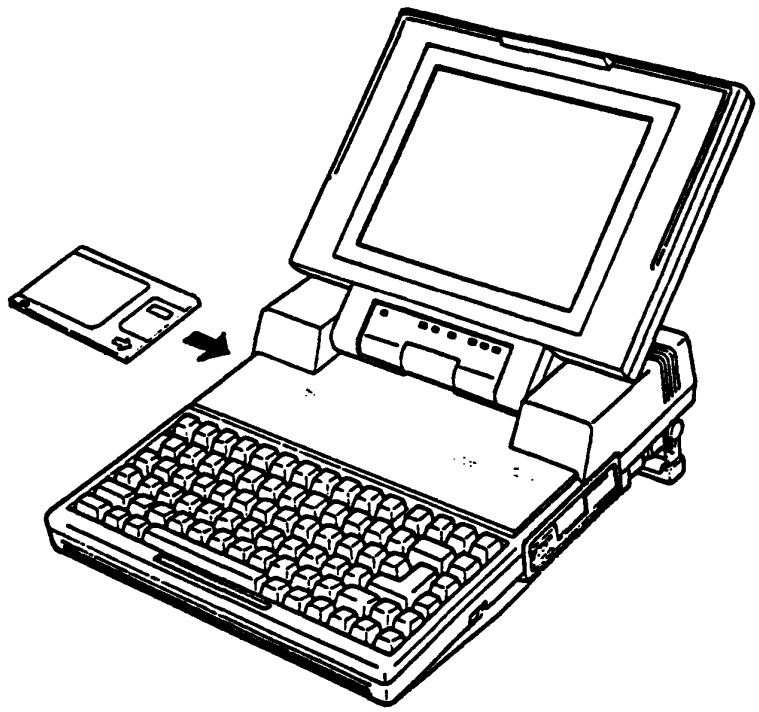


Figure **4-26** Use the FDD 2

Is the MS-DOS loaded ?

Yes: FDD 1 is faulty. Go to **FDD-10.**

No: Though FDD 2 is on ready, it may be interfered by FDD FDD 1. Remove the Upper Cover (Refer to PART 5), disconnect the FDD 1 cable from System PCB.
Repeat the operation to verify, then the MS-DOS is loaded, go to **FDD-5.**
If the failure remains, go to **FDD-10.**

Diagnostic Menu Check

1. After the T&D program loading, confirm that the following Diagnostic Menu appears on the display screen.

```
TOSHIBA personal computer T3100 DIAGNOSTICS
version X.XX (c) copyright TOSHIBA Corp 1986

DIAGNOSTICS MENU :

  1 - DIAGNOSTIC TEST
  2 - HARD DISK FORMAT
  3 - SEEK TO LANDING ZONE (HDD)
  4 - HEAD CLEANING
  5 - LOG UTILITIES
  6 - RUNNING  TEST
  7 - FDD UTILITIES
  8 - SYSTEM CONFIGURATION
  9 - EXIT TO MS-DOS
  0 - SETUP




PRESS [0]-[9] KEY
```

Is the above message displayed?

Yes: Go to **FDD-6.**

No: You may use a damaged disk. Prepare the other MS-DOS system disk, then repeat the operation to verify. (press "Ctrl"+"Alt"+"Del" keys)
If the failure remains, go to **FDD-10.**

Diagnostic Test Menu Check

1. Press "1" then "Enter" keys to display the Diagnostic Test Menu .

2. Confirm that the following Diagnostic Test Menu appears on the display screen.

```
TOSHIBA personal computer T3100 DIAGNOSTICS
version X.XX (c) copyright TOSHIBA Corp 1986

DIAGNOSTIC TEST MENU :

   1 - SYSTEM TEST
   2 - MEMORY TEST
   3 - KEYBOARD TEST
   4 - DISPLAY TEST
   5 - FLOPPY DISK TEST
   6 - PRINTER TEST
   7 - ASYNC TEST
   8 - HARD DISK TEST
   9 - REAL TIMER TEST
  88 - FDD & HDD ERROR RETRY COUNT SET
  99 - EXIT TO DIAGNOSTICS MENU




 PRESS [1]-[9] KEY
```

Does the above message displayed?

Yes: Go to **FDD-7.**

No: You may use a damaged disk. Prepare the other MS-DOS system disk, then repeat the operation to verify. (press "Ctrl"+"Alt"+"Del" keys)
If the failure remains, go to **FDD-10.**

Test Number Select

1. Press "5" then "Enter" keys to select the Floppy Disk Test.

2. Confirm that the following message appears under the Diagnostic Test Menu.

```
TOSHIBA personal computer T3100 DIAGNOSTICS
version X.XX (c) copyright TOSHIBA Corp 1986

DIAGNOSTIC TEST MENU :

   1 - SYSTEM TEST
   2 - MEMORY TEST
   3 - KEYBOARD TEST
   4 - DISPLAY TEST
   5 - FLOPPY DISK TEST
   6 - PRINTER TEST
   7 - ASYNC TEST
   8 - HARD DISK TEST
   9 - REAL TIMER TEST
  88 - FDD & HDD ERROR RETRY COUNT SET
  99 - EXIT TO DIAGNOSTICS MENU


Test drive number select (1:FDD1,2:FDD2,0:FDD1&2) ?


PRESS [0]-[9] KEY 5
```

Does the above message appear ?

Yes: Select the test drive number.
For FDD 1 test, press "1" then "Enter" keys.
For FDD 2 test, press "2" then "Enter" keys.
For FDD 1 and FDD 2 test, press "0" then "Enter" keys.
Go to **FDD-8.**

No: You may use a damaged disk. Prepare other MS-DOS system disk, then repeat the operation to verity.
(press "Ctrl"+"Alt"+"Del" keys)
If the failure remains, go to **FDD-10.**

Floppy Disk Test Menu

1. Confirm that the floppy Disk Test Menu is displayed as shown below.

```
FLOPPY DISK                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA  : XX
ADDRESS    : XXXXXX    STATUS      : XXX

SUB-TEST MENU :

01 - Sequential read
02 - Sequential read/write
03 - Random address/data
04 - Write specified address
05 - Read specified address
99 - Exit to DIAGNOSTIC TEST MENU




SELECT.SUB-TEST NUMBER  ?
```

2. Execute each sub-test in accordance with T&D operation procedures in. PART 8.
   Note: You need the good Work Disk for test execution.

Is any error message display ?

Yes: Go to **FDD-9.**

No: FDD is good. Anoter Unit may be suspected.

Connector Check

1. Turn OFF the power switch of the System Unit.
2. Remove the Upper Cover. (Refer to PART 5)
3. Check the FDD cable and connector for disconnection.

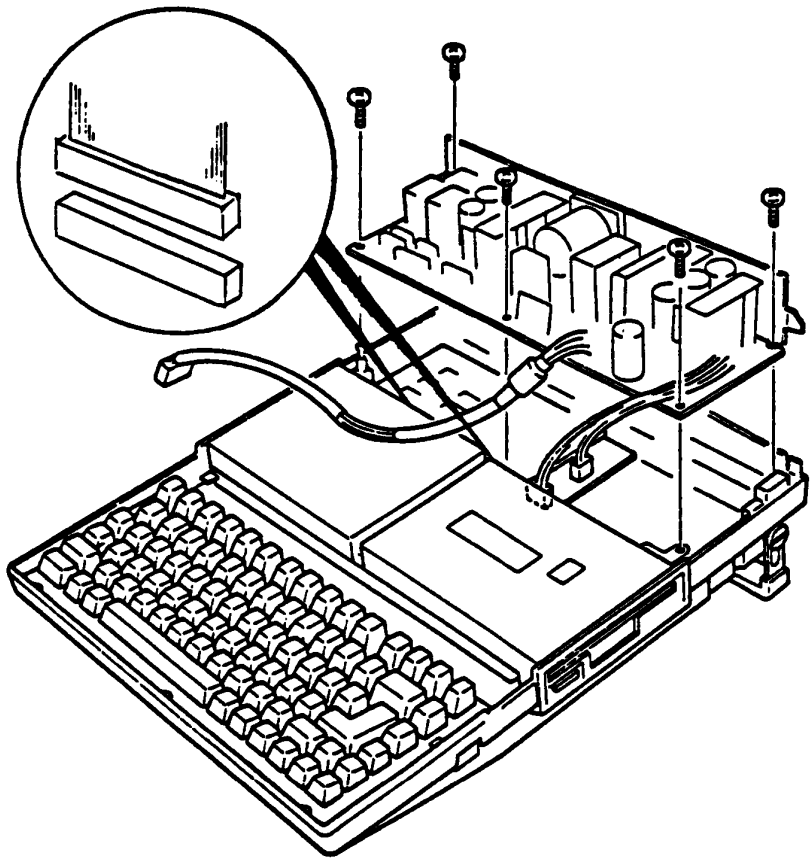


Figure 4-27 Connector Check

Is the FDD cable connection with the connector & correctly?

Yes: Go to **FDD-10.**

No: Conneect them, then repeat the T&D operation to verify. If the failre remains, go to **FDD-10.**

FDD connector check

1. Turn OFF the power switch of the System Unit.
2. Remove the FDD Unit. (Refer to PART 5)
3. Spread the four nailes(A) with the blade screwdriver to remove as shown below.

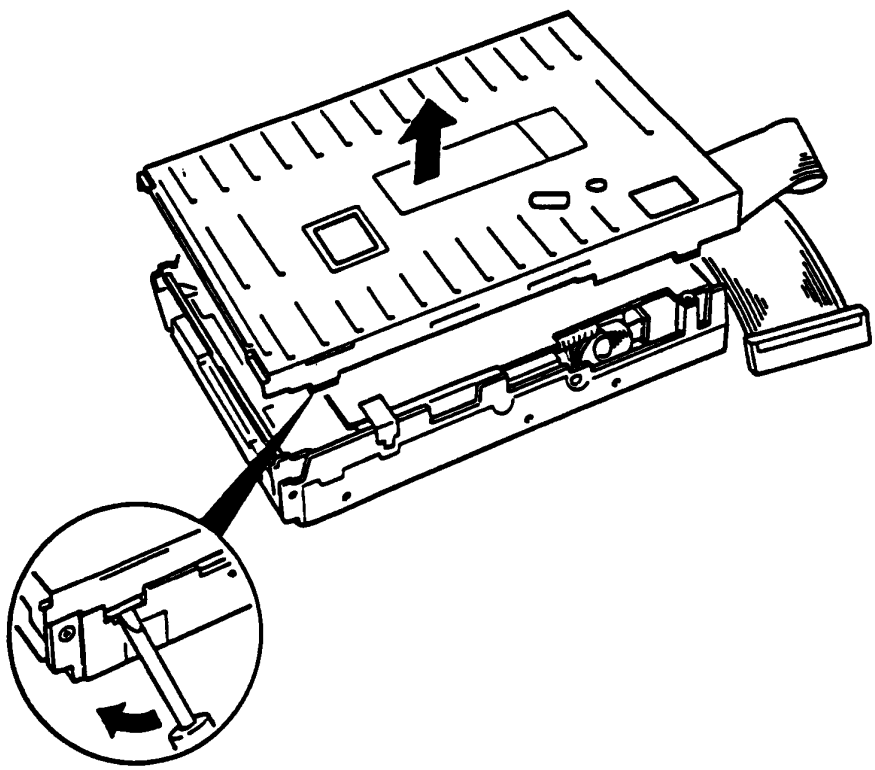


Figure 4-28 FDD Cover Removal

To be continued.

FDD conectors check (Continued)

4. Confirm that the five (J3, J4, J5, J6, J7) cables are connected to FDD PCB.

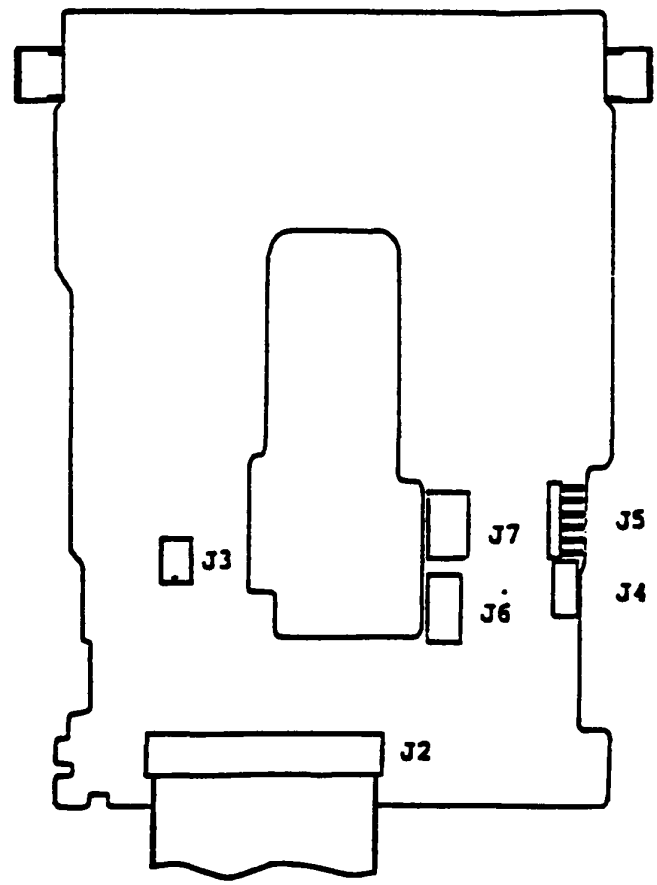


Figure 4-29 FDD PCB

Are the all cables connected ?

Yes: Go to **FDD-10.**

No: Connect them, then repeat the operation to verify it.

FDD PCB Replacement

1. Remove the two mounting screws (A), then spread two nailes (B) with the blade screwdriver and disconnect the soket (C).

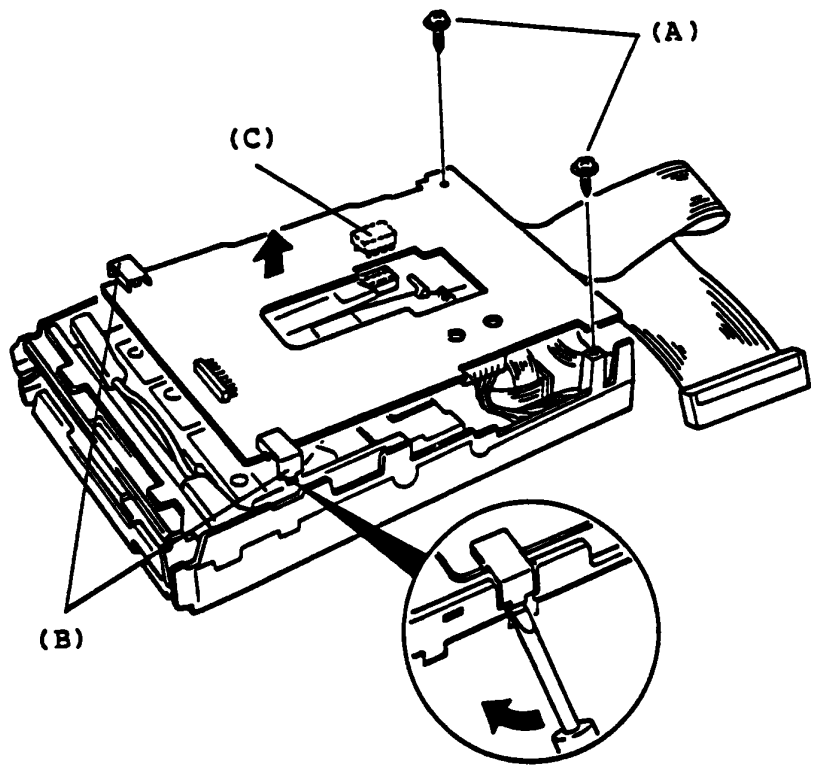


Figure 4-30 FDD PCB Removal

To be continued.

FDD PCB Replacement (Continued)

2. Disconnect two cables (D) from FDD PCB with a pair of tweezers hooking in the hole as shown below.
3. Disconnect the two connector (E) from the FDD PCB to remove.
4. Replace the suspected FDD PCB with a good spare FDD PCB.
5. Turn ON the power switch of the System Unit.
6. Repeat the T&D operation to verify.

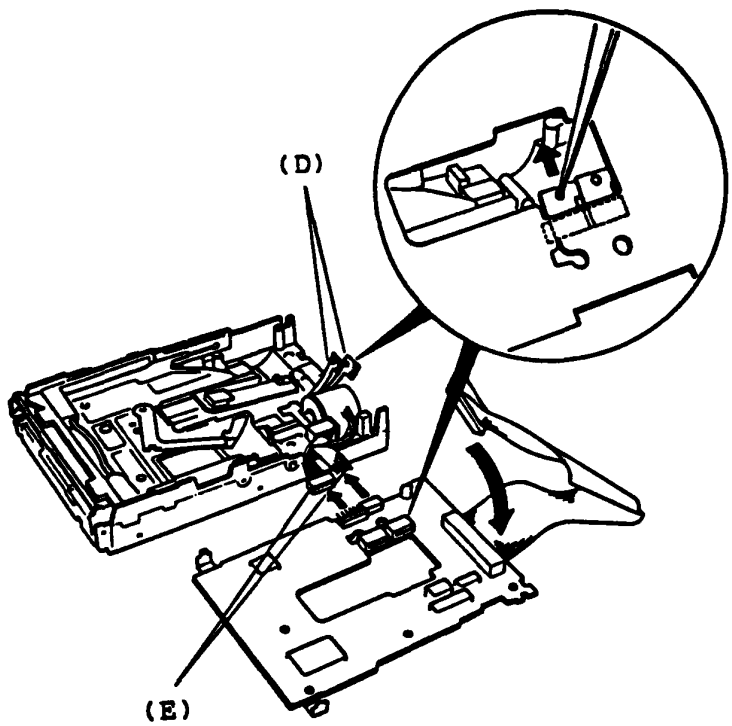


Figure 4-31 FDD PCB Removal

Does the failure remain ?

Yes: FDD PCB is good. Go to **FDD-12.**

No: FDD PCB is faulty.

FDD mechanical parts replacement

1. Replace the suspected FDD mechanical parts with a good spare FDD Device.
2. Install the FDD Unit, then turn ON the power switch of the System Unit.
3. Repeat the T&D operation to verify.

Does the Failure remain ?

Yes: The FDD mechanical parts is good. Go to **FDD-13.**

No: The FDD mechanical parts faulty.

FDD Replacement

1. Replace the suspected FDD with a good spare FDD.
2. Install the FDD Unit, then turn ON the power switch of the System Unit.
3. Repeat the T&D opration to verify.

Does the failure remain ?

Yes: The FDD is good. Another FDD Unit may be suspected.

No: The FDD is faulty.

FDD Adjustment

NOTE ...Following items are not applied to field maintenance.

This section provides adjustment procedure of FDD Unit and it includes the following.

1. Disk rotation period adjustment
2. Offtrack adjustment
3. Track 00 sensor position adjustment
4. Index timing adjustment

Note: Adjustment should be performed in the above order because the adjustments have an effect on the driver chracteristics.

Adjustment Tools

Adjustment Items / Required Tools	Disk rotation period adjustment	Offtrack adjustment position	Track 00 sensor adjustment	Index timing adjustment
Exerciser	○	○	○	○
Oscilloscope		○	○	○
CE Disk (Epson TC-301)		○	○	○
Normal Disk	○		○	
#1 Phillips screwdriver		○	○	○
#1 Flat screwdriver		○	○	○
Precision flat screwdriver	○			○
Torque screwdriver		○	○	○
Adhesive agent (LOCTITE #601)		○		

Positions and Functions of Test Points

Eight test points are provided on the SMD-280 main board unit for measuring the signal waveforms required for adjustment and inspection.

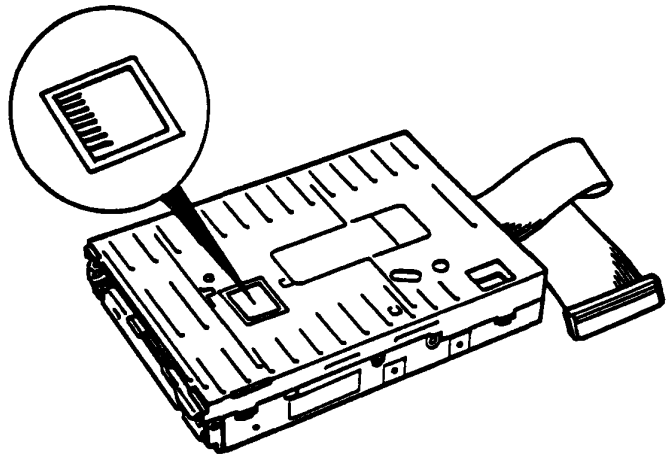


Figure 4-32 Position of Test Points

The contents of Test Pin as Follows.

TP-1(TKO) .... Test point for measuring the track 00 sensor position, the output level is Low and at track 1 or High at track 2.

TP-2(IDX) .... Test point for measuring the index signal.

TP-3(GND) .... An 0V (GND) analog signal line.
A reference point for measuring signal waveforms of TP-1, TP-2, TP-4, TP-5, TP-7, and TP-8.

TP-4(AMP) .... Test point for measuring read amplifiertput
TP-5(AMP) output. Differential waveforms which are 180 out of phase appear at TP-4 and TP-5.

TP-6(GND) .... 0V (GND) analog signal line.
A reference point for measuring the signal waveforms of TP-1, TP-2, TP-4, TP-5, TP-7, and TP-8.

TP-7(DIF) .... Test point for measuring differential
TP-8(DIF) amplfier output. Differential waveforms whic are 180 out of phase appear at TP-7 and TP-8.

Adjustment Procedures

1. Disk rotation Period Adjustment

   Adjustment Procedure

   a) Turn off the power.
   b) Connect the cable of an exerciser to the connecter PJ
   c) Turn on the power of spindle moter.
   d) Set the normal disk.
   e) Seek the head to track 40.
   f) Adjust VR1 on the spindle motor unit and set the pulse interval of the index output as follows:
      200 ± 0.6sec

2. Offtrack Adjustment

Adjustment Procedure

a) Turn off the power.
b) Connect the SMD-280 to the Exerciser and connect TP-1 to CH 1 of the oscilloscope, TP-2 to CH2, and the Exerciser index output terminal to the external trigger.
c) Set the measuring conditions of the oscilloscope as follows:

Channel	CH1,CH2
AC-GND-DC	AC
VERT MODE	ADD
INVERT	ON
VOLTS/DIV	50 mV
TIME/DIV	20 msec

d) Turn on the spindle motor and set the CE disk.
e) Return the head to track 00. Next, move the head to track 40 using the STEP switch on the Exerciser.
f) Observe the offtrack signal waveforms on the oscilloscope. If the ratio between the right and left burst signal levels (small/large) is 0.8 or less, insert the Phillipes screwdriver into the screwdriver insertion holes on the main board unit and loosen the two stepping clamper mounting screws. Next, insert the stepping motor unit back and forth while turning the screwdriver. after adjusting the burst signal level ratio to 0.8 or more, tighten the stepping clamper mounting screws.
g) Apply the adhesive agent (LOCTITE #601) to the stepping clamper mounting screws.

3. Index Timing Adjustment

   Adjustment Procedure

   a) Turn off the power.
   b) Connect the SMD-280 to the Exerciser.
   c) Turn on the spindle motor and set the CE disk.
   d) Return the head to track 00. Next move the head to track 40 using the STEP switch on the Exerciser.
   e) Using the Exerciser, check that the index burst timing in the range 90-350 usec. If the timing in outside this range, adjust the index burst adjustment resistor (VR1).

4. Track 00 Sensor Position Adjustment

Adjustment Procedure

a) Turn off the power.
b) Connect the SMD-280 to the Exerciser.
c) Check that the offtrack adjustment has been completed by CE disk.
d) Set the measuring conditions of the oscilloscope as follows:

Channel	CH1
AC-GND-DC	DC
VERT-MODE	CH1
INVERT	-
VOLTS/DIV	1 V
TIME/DIV	0.1 msec

e) Connect TP-1 to CH1 of the oscilloscope and short the terminal 1 and 4 of J4 by wire.
f) Turn on the power.
g) Set the normal disk and turn on the Spindle motor. Move the head carrige unit to the outermost track.
h) Check whether the output at TP-1 is 1 V or less at track 2 using the oscilloscope.
i) Next, check whether the output at track 1.
j) Whn the outputs are more than 1 V at track 2 and less than 4 V at track 1, adjust them as follows.
k) Insert the Phllips screwdriver through the shield cover or main board unit and loosen the track 00 sensor mounting screw.
l) Next, insert the flat screwdriver btween the main frame groove and track 00 sensor mounting board.
m) While observing the oscilloscope, rotate the flat screwdriver and adjust the output at TP-1 until it is 1 V less at track 2 and 4 V or more at track 1.
n) Tighten the track 00 sensor mounting screw.

HDD/HDC
(3.3" Hard Disk Drive and Controler)

You have reached this TIP since HDD/HDC is suspected of the cause of the failure.

The symptom may be one of the follows.

1. After the Power-On Diagnostics, the system is hung up instead of T&D program running.

2. Any error status appears during HDD operation.

WARNING

All data on the HDD will be lost permanently during this Trouble Isolation Procedure (e.g. : write operation in T&D mode).

Go to **HDD/HDC-1** for the symptom 2 of the above.

Go to **HDD/HDC-4** for the symptom 1 of the above.

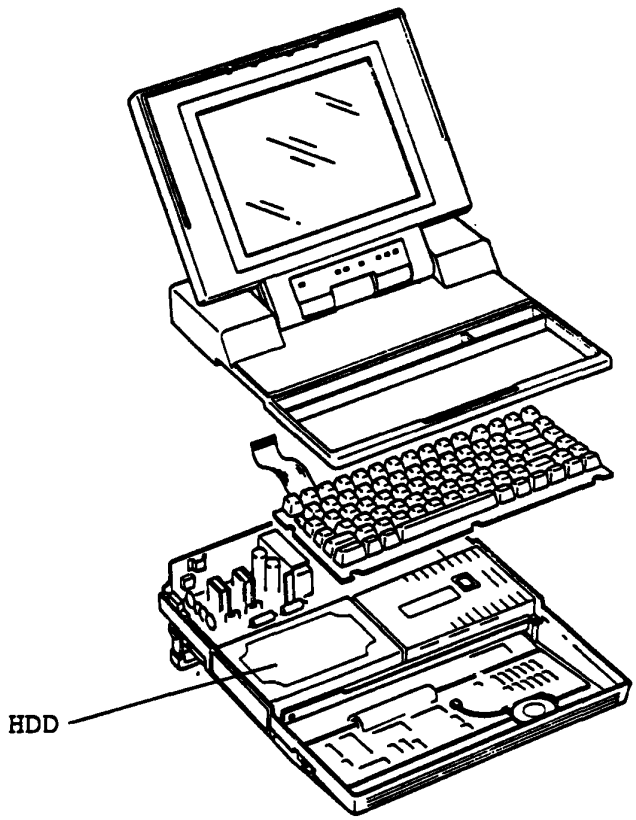


Figure 4-33 T3100 System Unit

LED check

1. Insert the MS-DOS System Disk to FDD.
2. Turn ON the power switch of the System Unit.
3. Check the LED (Disk in Use) left of indicator lighting.

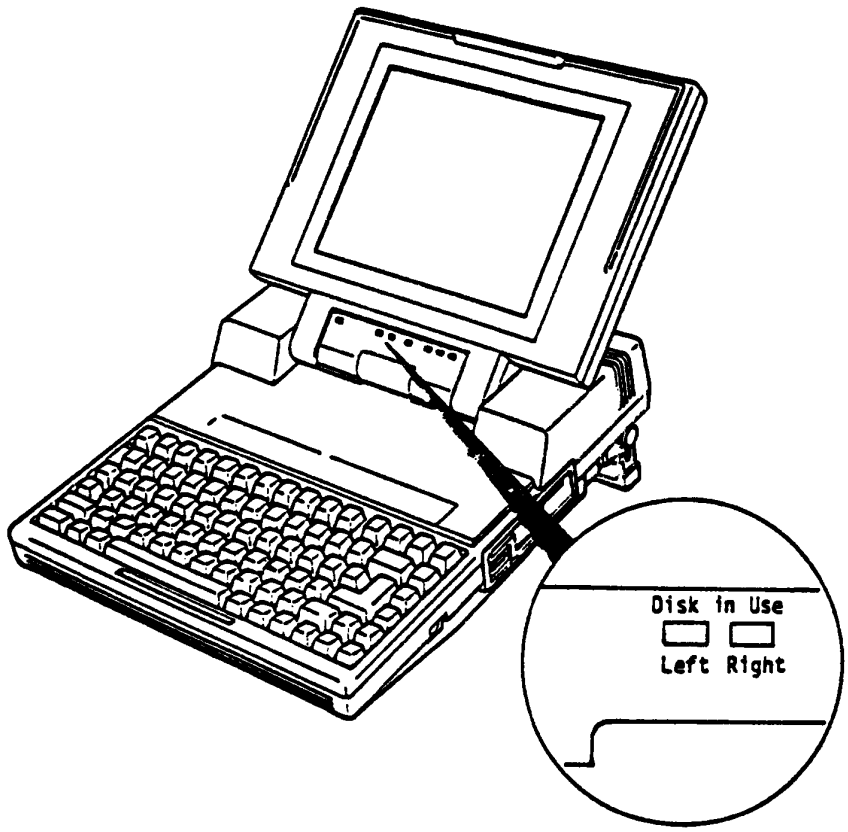


Figure 4-34 LED Check

Is the LED lighting ?

Yes: Go to **HDD-2.**

No: Go to **HDD-4.**
If you have disassembled the System Unit before, confirm that the Indicator cables is connected correctly to the Indicator board.

Diagnostic Menu

1. After MS-DOS loading, run to the Test & Diagnostics.
2. Press "1" then "ENTER" keys to display the DIAGNOSTIC MENU.
3. Confirm that the following DIAGNOSTIC TEST MENU appears on the screen.

```
TOSHIBA personal computer T3100 DIAGNOSTICS
version X.XX (c) copyright TOSHIBA Corp 1986

DIAGNOSTIC TEST MENU :

   1 - SYSTEM TEST
   2 - MEMORY TEST
   3 - KEYBOARD TEST
   4 - DISPLAY TEST
   5 - FLOPPY DISK TEST
   6 - PRINTER TEST
   7 - ASYNC TEST
   8 - HARD DISK TEST
   9 - REAL TIMER TEST
  88 - FDD & HDD ERROR RETRY COUNT SET
  99 - EXIT TO DIAGNOSTICS MENU




 PRESS [1]-[9] KEY
```

Is the above message displayed ?

Yes: Go to **HDD/HDC-3** .

No: Go to **FDD.**

Hard Disk Test

1. After press "8" then "ENTER" keys appear the following message on the screen.

   Test drive number select (1: HDD1, 2: HDD2, 0: HDD1&2)

   1: Executes the test of only drive 1.
   2: Executes the test of only drive 2.
   3: Executes the test of drive 1 and drive 2.

2. After choose the above number, then press it.

3. Confirm that the following screen appears for test selection.

```
HARD DISK TEST                          XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Sequential read
02 - Address uniquence
03 - Random address/data
04 - Cross talk & peek shift
05 - Write/read/compare(CE)
06 - Write specified address
07 - Read  specified address
08 - ECC circuit (CE cylinder)
99 - Exit to DIAGNOSTIC TEST MENU


SELECT SUB-TEST NUMBER  ?
```

To be continued.

Hard Disk Test (continued)

4. Execute each subtest in accordance with T&D operation procedures in PART 8.

WARNING

The data on the HDD will be lost permanenty during the write operations in subtests 2, 3, 4, 6, and 8.

Current disk contents will be completely destroyed. Save the data on Hard Disk before execute this program if you don't want to do so.

If you execute the subtest 2, 3, 4, 6, and 8, must set the partition of HDD. (Refer to PART 8)

Any error message or hung up ?

Yes: Go to **HDD/HDC-4** .

No: HDD is good.
Another unit would be suspected.

Connector check

1. Turn OFF the power switch of the System Unit.
2. Remove the Upper Cover and Power Supply Unit. (Refer to PART 5)
3. Check the connector and cable between HDD and System PCB for damage or disconnection.

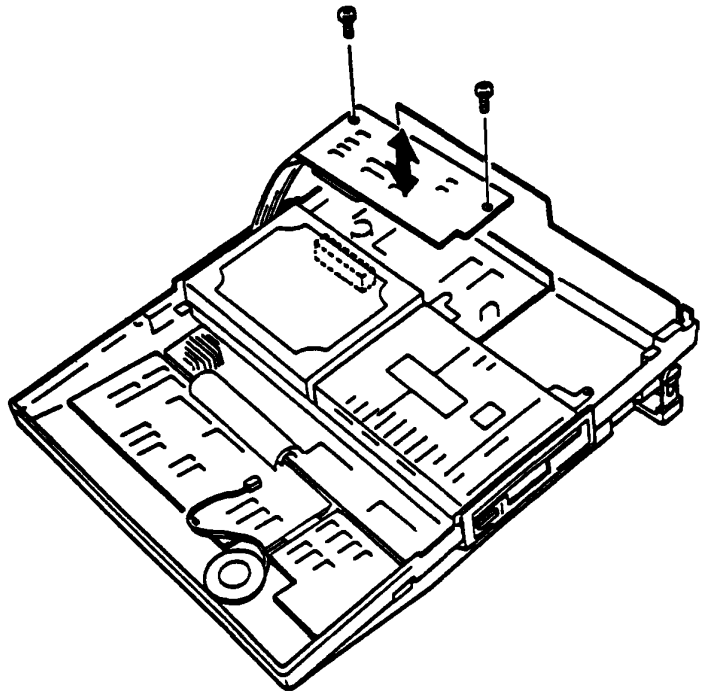


Figure 4-35 Connector Check

Is there any damage on the HDD cable or disconnection with the connector & correctly

Yes: In the case of the HDD cable disconnection, connect it, then repeat the T&D operation to verify it.
In the case of the HDD cable is damaged, replace the keyboard cable, then repeat the T&D operation to verify it.
If the failure remains, go to **HDD-5.**

No: Go to **HDD-5.**

Voltage check

1. Connect the Power Supply cable to System PCB, then put it rear of System Unit.

2. Turn ON the power switch of the System Unit.

3. Check the voltages at each connector pin with AVO meter. Refer to)
   Note: Ground point is mounting screws(A).

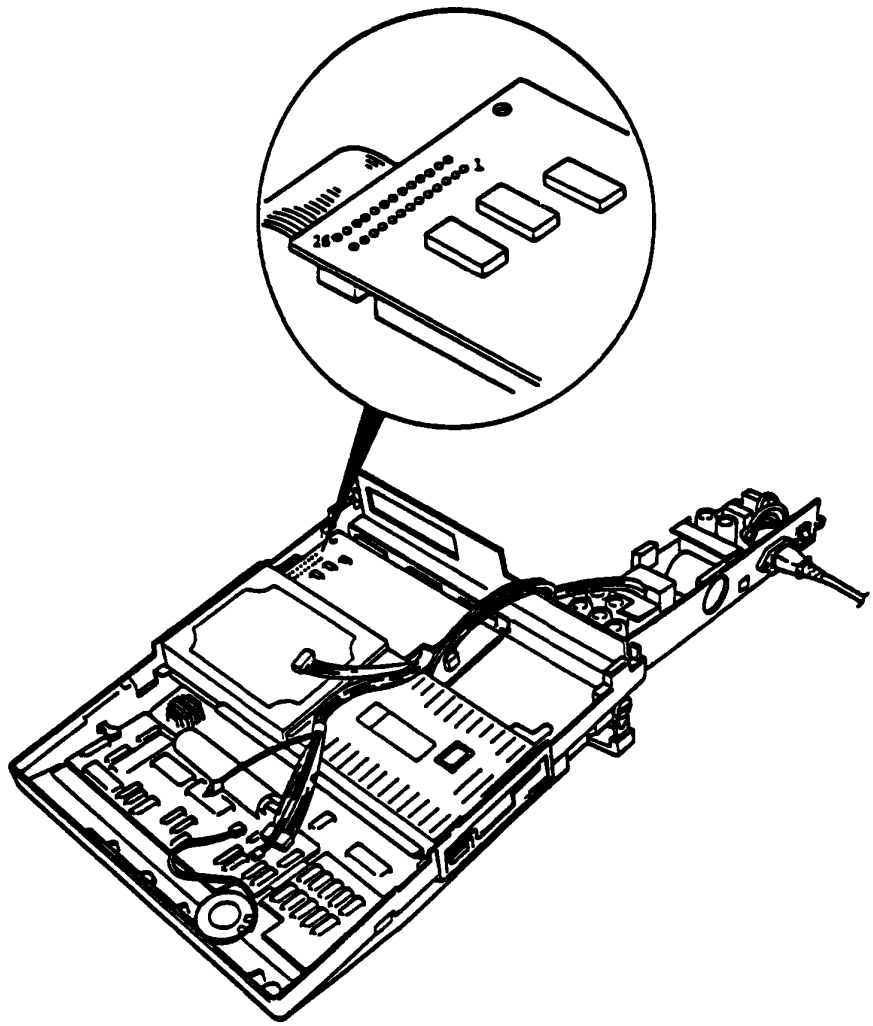


Figure 4-36 Voltage Check

To be continued.

Voltage Check (Continued)

Voltage Tolerance

Pin		Voltage		
+ Lead	- Lead	Normal Vdc	Min Vdc	Max Vdc
22	GND	+ 5	+ 4.75	+ 5.25
24	GND	+ 5	+ 4.5	+ 6.0
26	GND	+ 12	+ 11.4	+ 12.6

Are the voltage within the torelances ?

Yes: Go to **HDD/HDC-6** .

No: Go to **HDD/HDC-5** .

HDC replascement

1. Replace the suspected HDC with a good spare HDC.
2. Turn ON the power switch of the System Unit.
3. Repeat the T&D operation to verify it.

Does the failure remain ?

Yes: The HDC is good. Go to **HDD/HDC-7** .

No: The HDC is faulty.

HDD replacement

1. Peplace the suspected HDD with a good spare HDD.
2. Turn ON the power switch of the System Umit.
3. Repeat the T&D operation to verify it.

Does the failure remain ?

Yes: The HDD is good. Another Unit may be suspected.

No: The HDD is faulty.

You have reached this TIP scince Keyboard is suspected of the cause of the failure.
You need good key-switch for maintenance and key cap remover for remove the key switch..

The symptom may be one of follows.

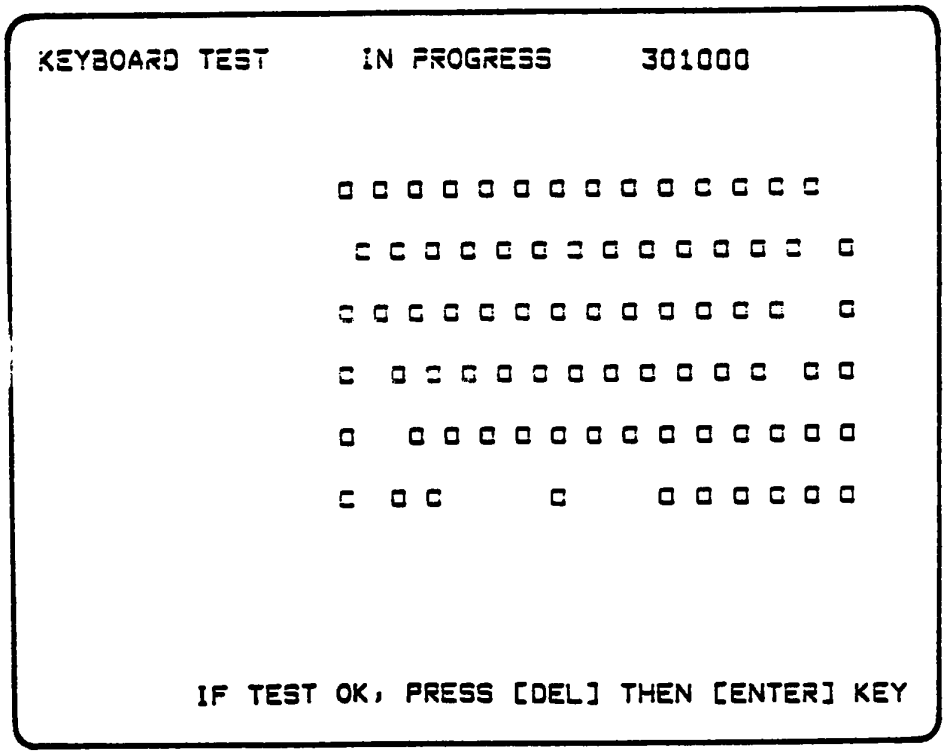
1. Character(s) are lost or changed incorrectly during key-in operation.

2. Excessive character(s) are transferred from the Keyboard to the System Unit.

Go to **KEYBOARD-1** for the symptom 1 and 2 of the above.

T&D Operation

1. Insert the MS-DOS program disk to the Int. FDD Unit of the System Unit.
2. Turn ON the power switch of the System Unit.
3. Execute the T&D program for keyboard in accordance with the T&D operation procedure of "PART 8".



Does all input operation function correctly ?

Yes: Another unit is suspected.

No: Go to next page.

T&D Operation (Continued)

The symptom may be one of follows.

1. All input operation do not function correctly:

   Go to **KEYBOARD-2.**

2. Specified input operation do not function correctly:

   Refer to Key Matrix and key number (See next page), then judge the Keyboard cable faulty or Key-switch faulty.
   If Keyboard cable faulty, go to **KEYBOARD-3.**
   If Key-switch faulty, go to **KEYBOARD-4.**

3. One or two input operation does not function correctly:

   The Key-switch may be faulty. Go to **KEYBORD-4.**

T&D Operation (Continued)

Table 4-1 Key Matrix

KBSCNb \ KBRTa	0	1	2	3	4	5	6	7
A	84							
9	14	80	71	28	41	54	55	82
8	13	72	26	27	77	40	53	58
7	11	12	25	75	38	39	52	83
6	9	10	23	24	36	37	51	50
5	7	8	21	22	35	48	49	57
4	5	6	19	20	33	34	47	46
3	3	4	17	18	31	32	44	45
2	1	2	15	16	30	29	42	43
1	60	70	62	73	64	66	68	56
0	59	69	61	81	63	65	67	79

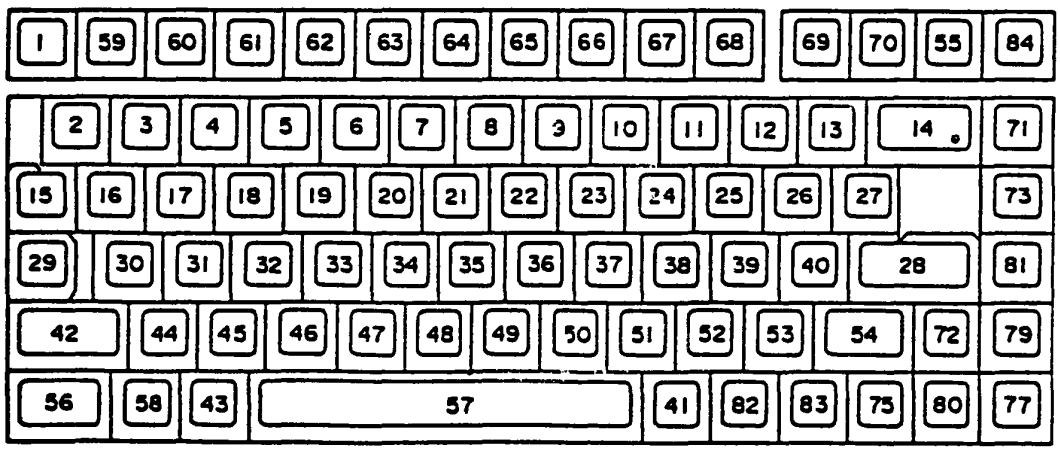


Figure 4-37 Key number

Connector check

1. Turn OFF the power switch of the System Unit.
2. Disassenble the System Unit cabinet. (Refer to PART 5)
3. Check that the keyboard cable connect on the System PCB.

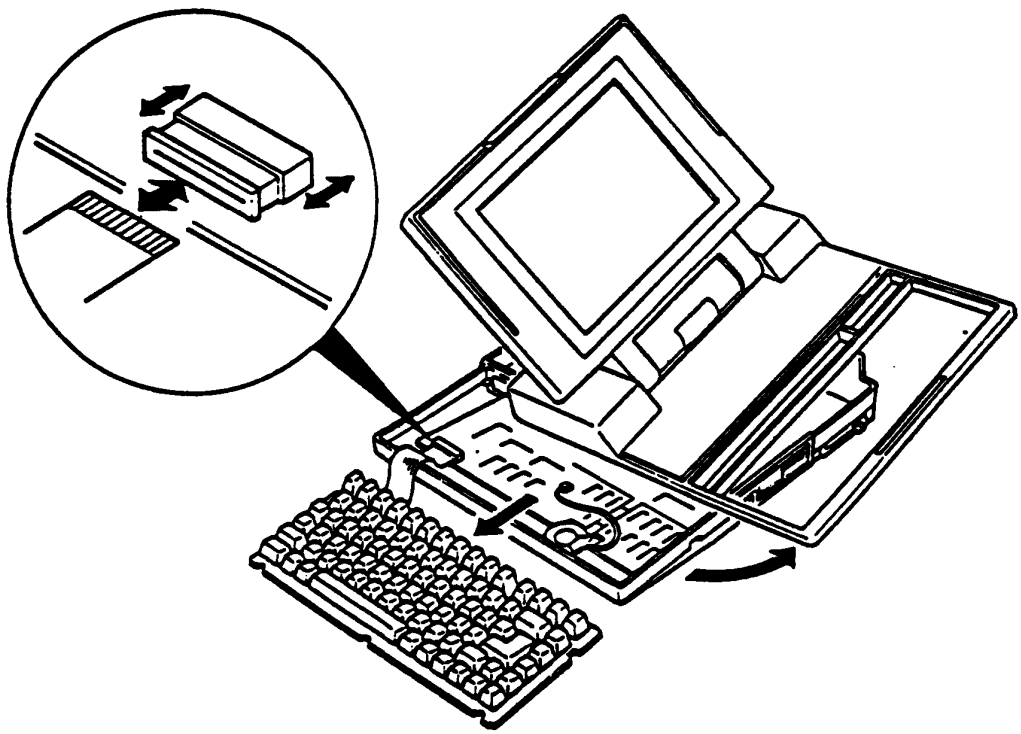


Figure 4-38 Connector check

Does the keyboard cable connect ?

Yes: Go to **KEYBOARD-3.**

No: Connect them, then repeat the operation to verify it.

Connector check for damage

1. Check the Keyboard cable for damage with AVO meter.

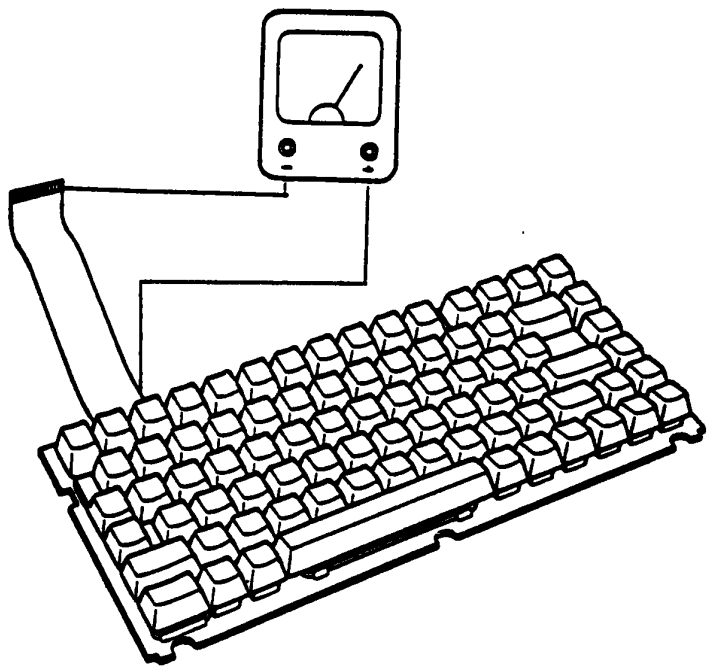


Figure 4-39 Check for Damage

Is there any damage on the Keyboard cable ?

Yes: Replace the Keyboard cable, then repeat the T&D opresion to verify it.
If the failure remains, go to **KEYBOARD-5.**

No: Go to **KEYBOARD-5.**

Key-switch replacement

1. Turn OFF the power switch of the System Unit.
2. Disassenble the System Unit cabinet. (Refer to PART 5)
3. Remove the Keyboard from the System Unit.
4. To replace a key cap, hold the cap with the attached key cap remover as in the bellow and pull it out right above. When fixing a key cap, push the key cap just a bit below.
5. Replace the Key-switch with good spare one.

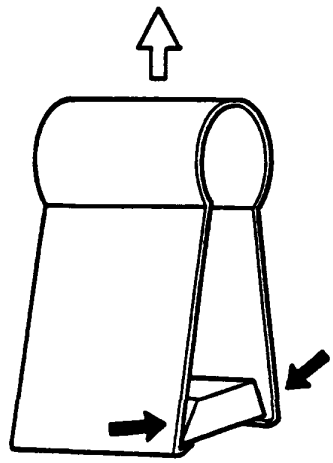


Figure 4-40 Key cap remover

Does the failure remain ?

Yes: Go to **KEYBORD-4.**

No: Key-switch is faulty.

Keyboard replacement

1. Replace the Keyboard and Keyboard Cable with good spare ones. (Refer to PART 5)
2. Turn ON the power switch of the System Unit.
3. Run the T&D program of Keyboard for verification.

Does the failure remain ?

Yes: The Keyboard is good. Another Unit may be suspected.

No: The Keyboard Unit is faulty.

PLASMA DISPLAY

You have reached this TIP since Plasma Display is suspected of the cause of the failure.

The symptom may be one of the follows.

1. Neither of character nor graph appear on the Plasma Display while the system is running.
2. Pictures on the Plasma display are distorted.

WARNING

High voltages exist in a Plasma Display Unit and it is harmful to the human body. It is recommended that only Plasma Display Unit replacemnet will be done in the field as the maintenance service except by qualified and trainned person.

Go to **DISPLAY-1** for the symptom 1 of the above.

Go to **DISPLAY-14** for the symptom 2 of the above.

Display check

1. Turn ON the power switch of the System Unit.
2. Check that the display indicats all dots for a second momentarily.

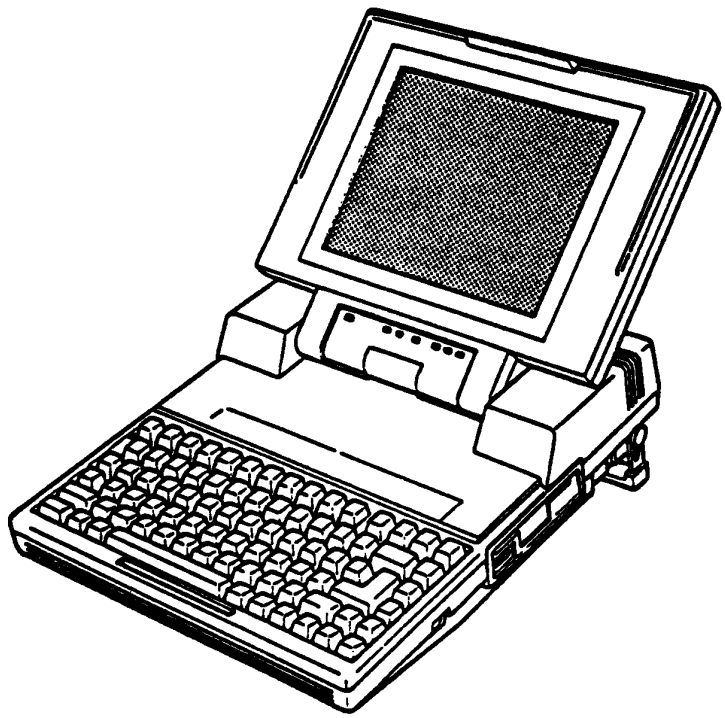


Figure 4-41 Display Check

Are the above all dots displayed ?

Yes: Go to **DISPLAY-2**

No: In the case of Plasma Display isn't displayed all dots, go to **DISPLAY-14.**
In the case of Plasma Display isn't displayed some dots, go to **DISPLAY-17.**

DISPLAY-2

Screen check at the start up time

1. Turn ON the power switch of the System Unit.
2. After the display indicats all dot, confirm that the following message on the display screen.

MEMORY TEST XXX KB

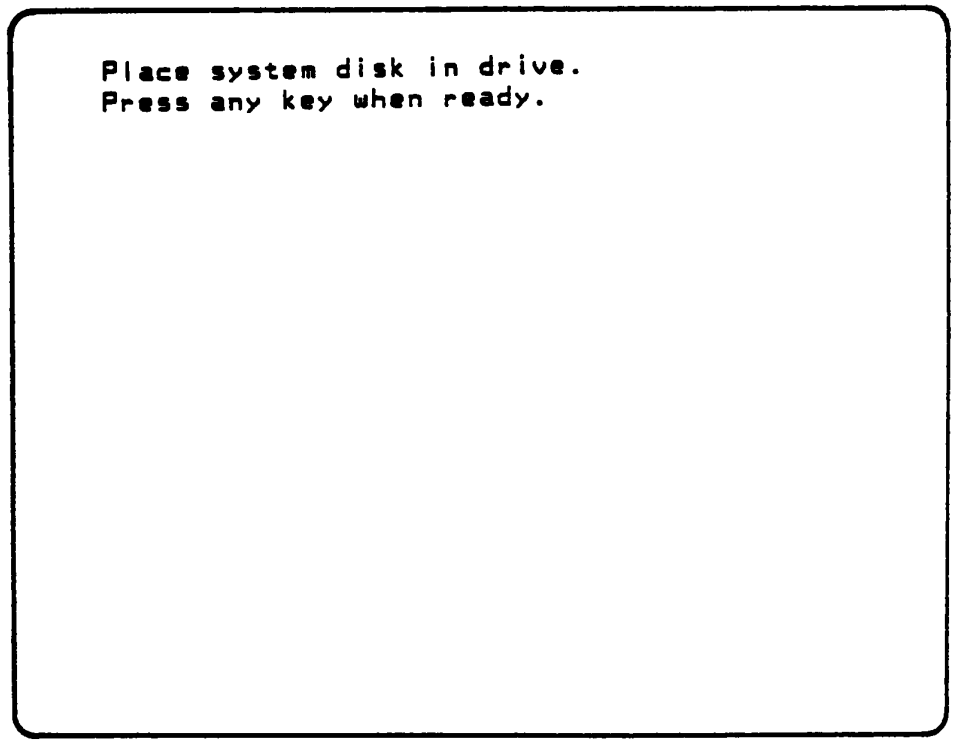
Does the above message appears ?

Yes: Go to **DISPLAY-3.**

No: Go to **DISPLAY-14.**

Message check

1. After **"MEMORY TEST XXX KB"** message appears on the display screen, confirm that the following message appears on the display screen.



Does the above message appear ?

Yes: Go to **DISPLAY-4.**

No: Go to **DISPLAY-14.**

Display Test Menu check

1. After the MS-DOS loading, run the Test & Diagnostic.
2. Press "4" then "Enter" keys for selecting the Display test of **DIAGNOSTIC TEST MENU.** (Refer to PART 8)
3. Confirm that the following Display Sub-test Menu appears on the display screen.

```
DISPLAY TEST                                XXXXXXX


SUB-TEST      : XX
PASS COUNT: XXXXX       ERROR COUNT: XXXXX
WRITE DATA: XX          READ  DATA : XX
ADDRESS   : XXXXXX      STATUS     : XXX

SUB-TEST MENU :

01 - VRAM read/write
02 - Character attributes
03 - Character set
04 - 80 * 25 Character display
05 - Graphics display (color set 0/1)
06 - 640 * 200 Graphics display
07 - 640 * 400 Graphics display
08 - Display page
09 - "H" pattern display
99 - Exit to DIAGNOSTIC TEST MENU


SELECT SUB-TEST NUMBER  ?
```

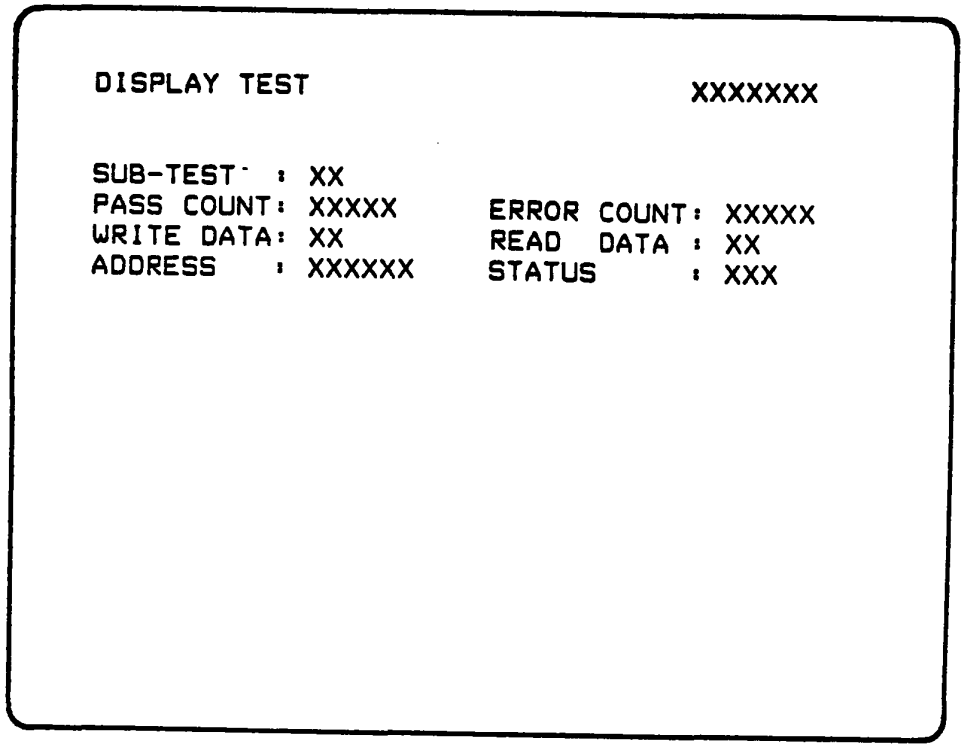
Does the above message appear ?

Yes: Go to **DISPLAY-5.**

No: Go to **DISPLAY-14.**

(01) VRAM read/write

1. Press **01** then keys on the Display test menu.
   The following message appears on the screen for very short time,then it returns to the Display Test Menu.



Does the error message appear ?

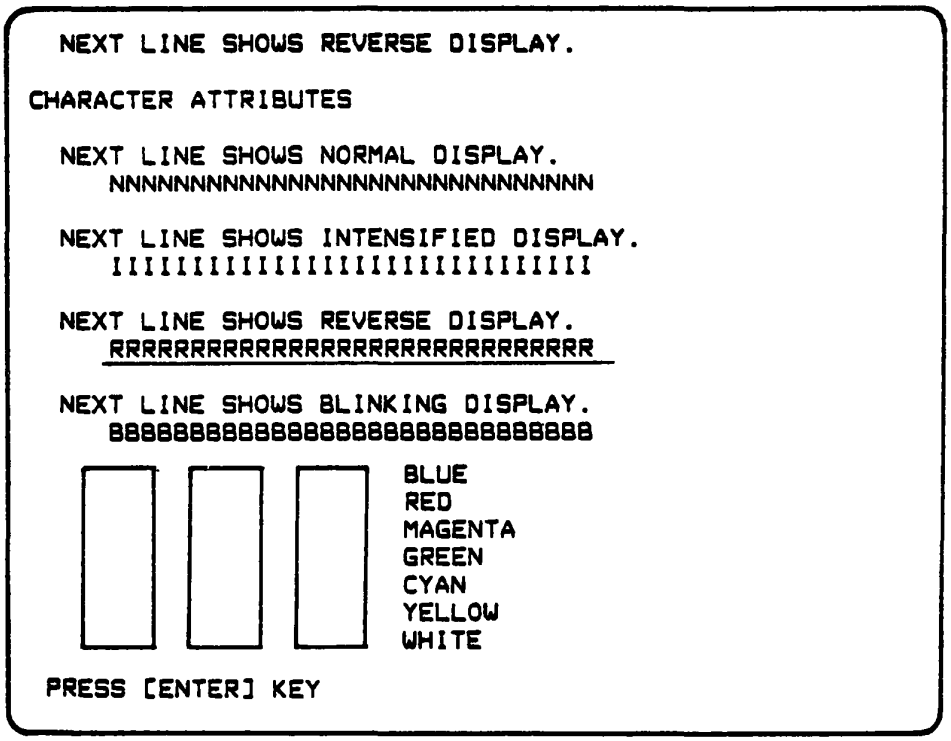
Yes: System PCB is faulty.
Replace the System PCB. (Refer to PART 3)

No: Go to **DISPLAY-6.**

(02) Character attributes

1. Press **02** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.
   Note: Underline position of the following screen display "**R**.........." to turn on and off.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly

Yes: Go to **DISPLAY-7.**

No: System PCB is faulty.
Replace the System PCB, then check it again.

(03) Character set

1. Press **03** then **ENTER** keys on the Display Test Menu, then the following pattern appears on the screen.
2. Press **ENTER** key to return to the Display Test Menu.

Is the above pattern displayed correctry ?

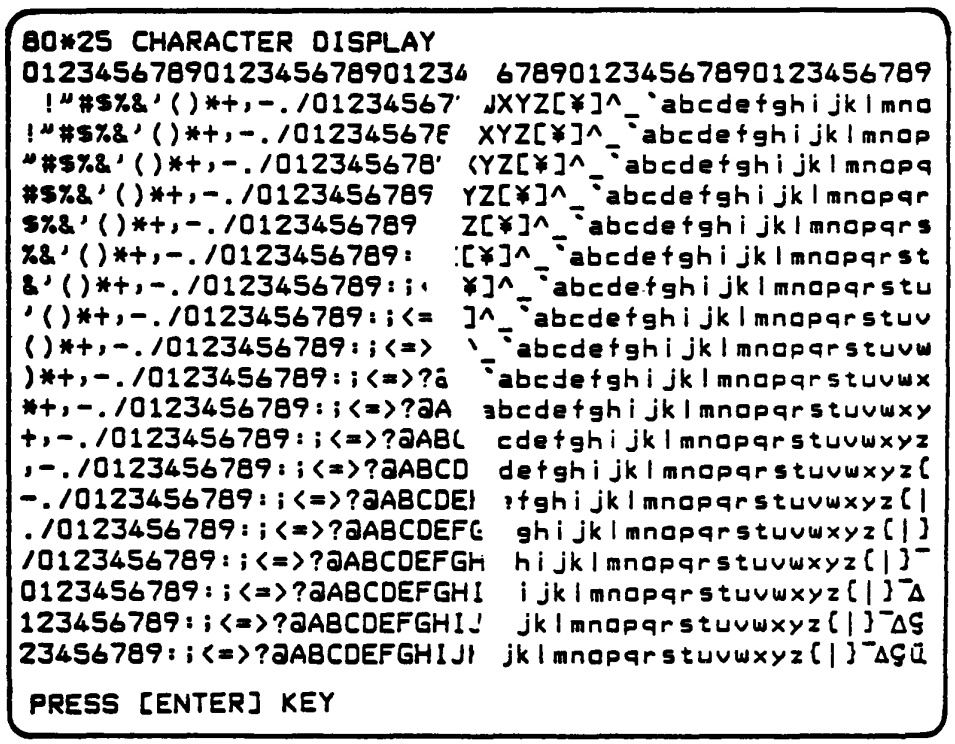
Yes: Go to **DISPLAY-8.**

No: System PCB is faulty.
Replace the System PCB, then check it again.

(04) 80 * 25 Character display

1. Press **04** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appear on the screen.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

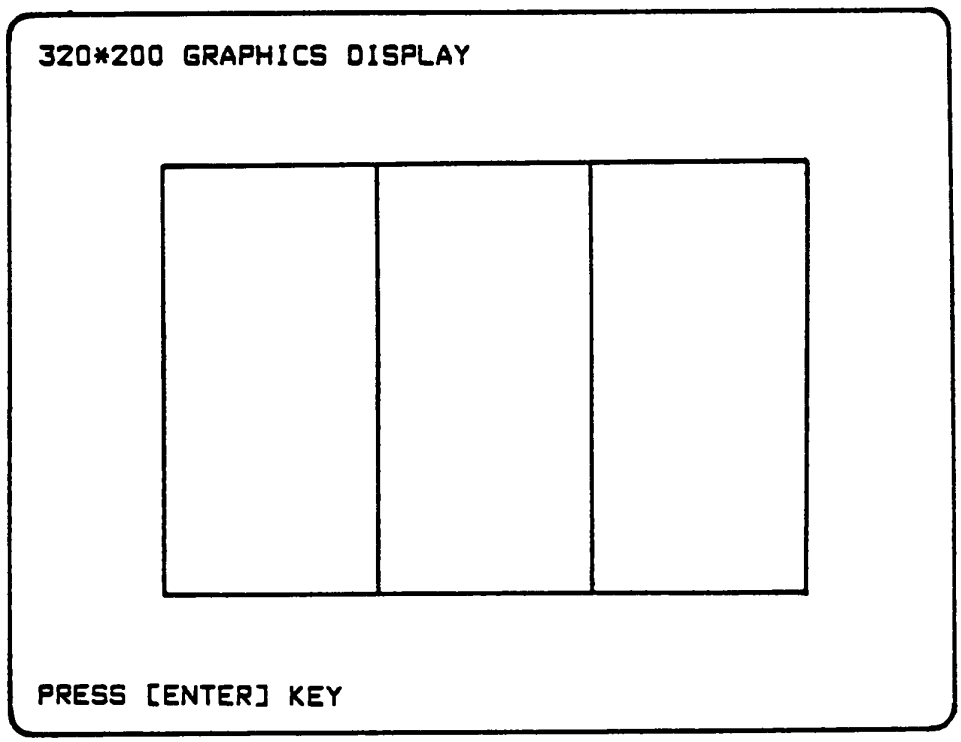
Yes: Go to **DISPLAY-9.**

No: System PCB is faulty.
Replace the System PCB, then check it again.

(05) Graphics display (color set 0/1)

1. Press **05** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.
   Note: Right most block is the brightest.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

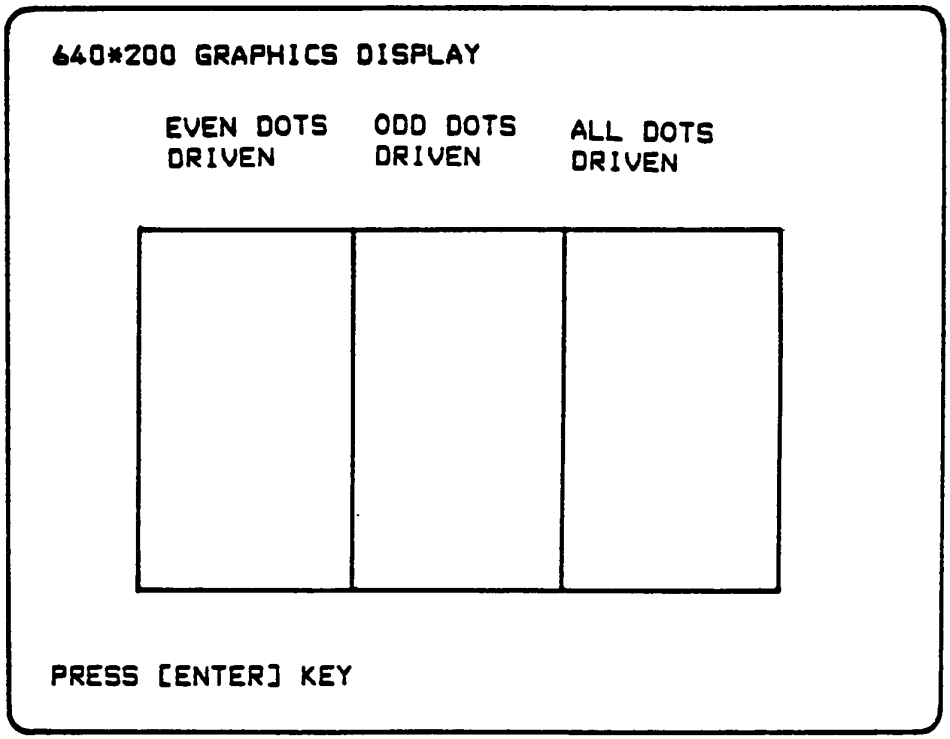
Yes: Go to **DISPLAY-10.**

No: System PCB is faulty.
Replace the System PCB, then check it again.

(06) 640 * 200 Graphics display

1. Press **06** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.
   Note: Right most block (ALL DOTS DRIVEN) is the brightest.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

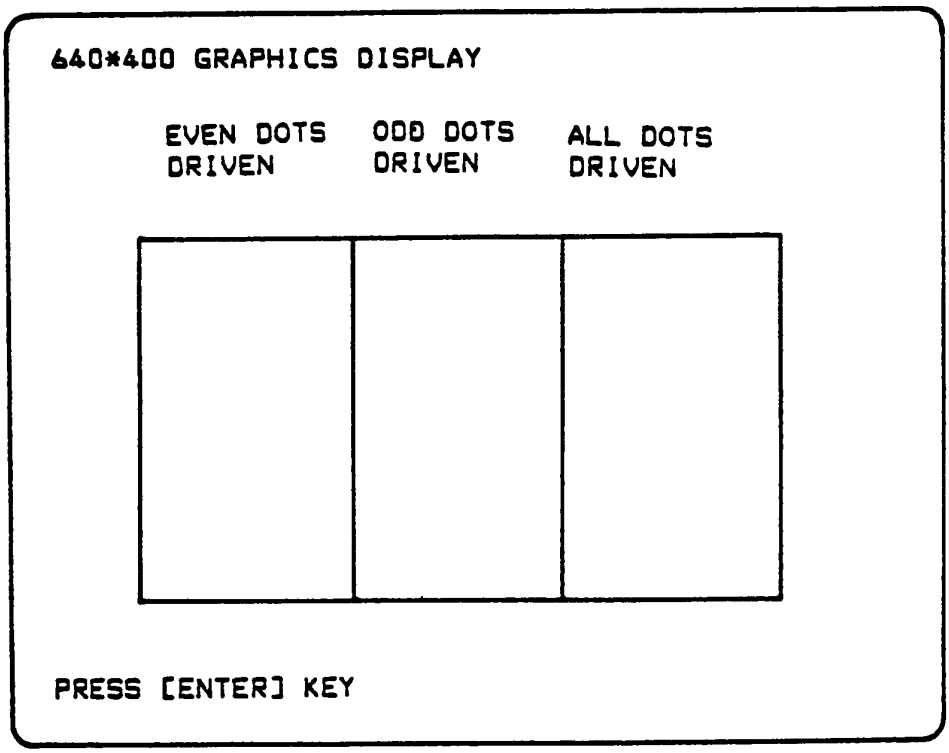
Yes: Go to **DISPLAY-11.**

No: System PCB is faulty.
Replace the System PCB, then check it again.

(07) 640 * 400 Graphics display

1. Press **07** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.
   Note: Right most block (ALL DOTS DRIVEN) is the brightest.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

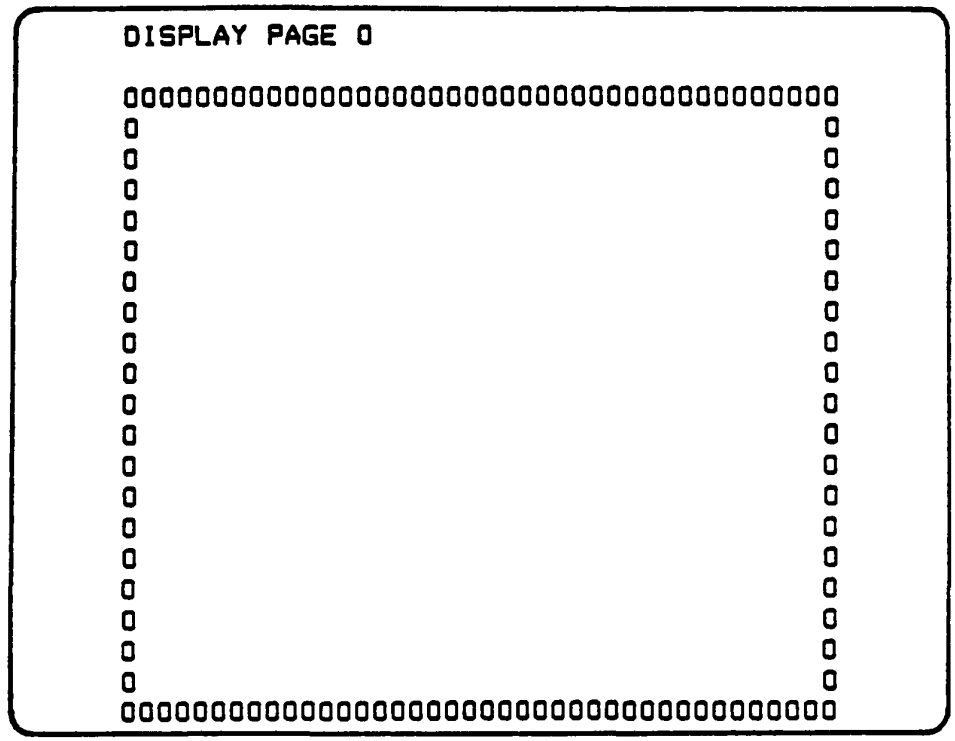
Yes: Go to **DISPLAY-12.**

No: System PCB is faulty.
Replace the System PCB, then check it again.

(08) Display page

1. Press **08** then **ENTER** keys while the Display Test Menu appears.
   The following patturn appears on the screen.
   Note: The following ~~the~~ screen change a page number (0-7).

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

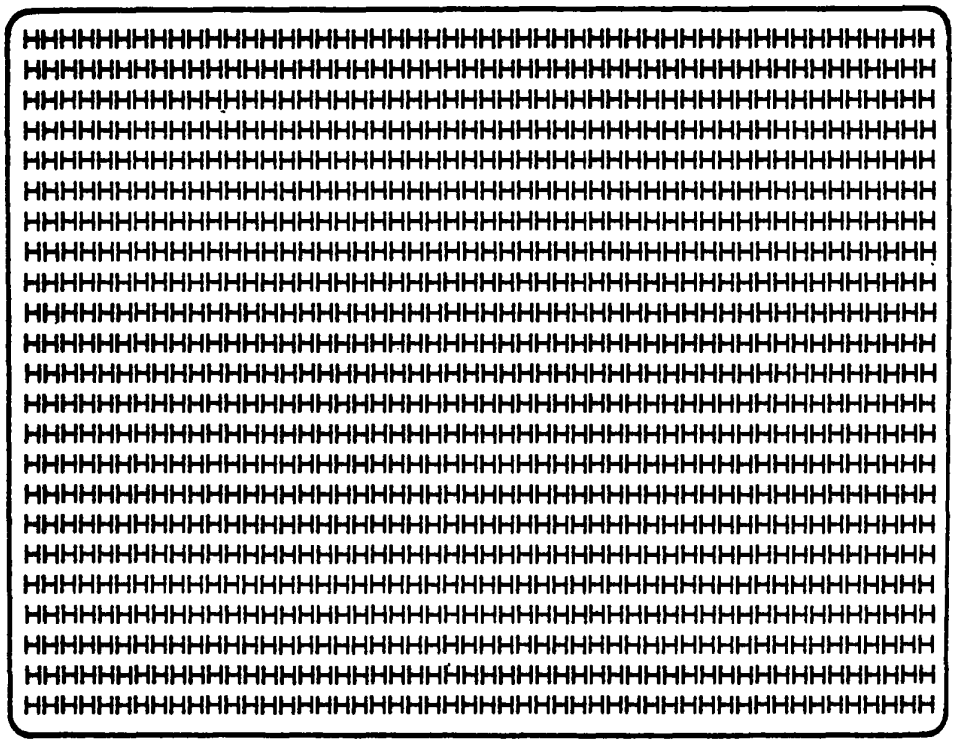
Yes: Go to **DISPLAY-13.**

No: System PCB is faulty.
Replace the System PCB, then check it again.

(09) "H" pattern display

1. Press **09** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

Yes: Go to **DISPLAY-14.**

No: System PCB is faulty.
Replace the System PCB, then check it again.

Connector Check

1. Turn OFF the power switch of the System Unit.
2. Remove the PDP (Plasma Display Panel), but the three cables of PDP.
   And put it on the Keyboard.
3. Check the PDP connectors and cables are connected correctly & securely.

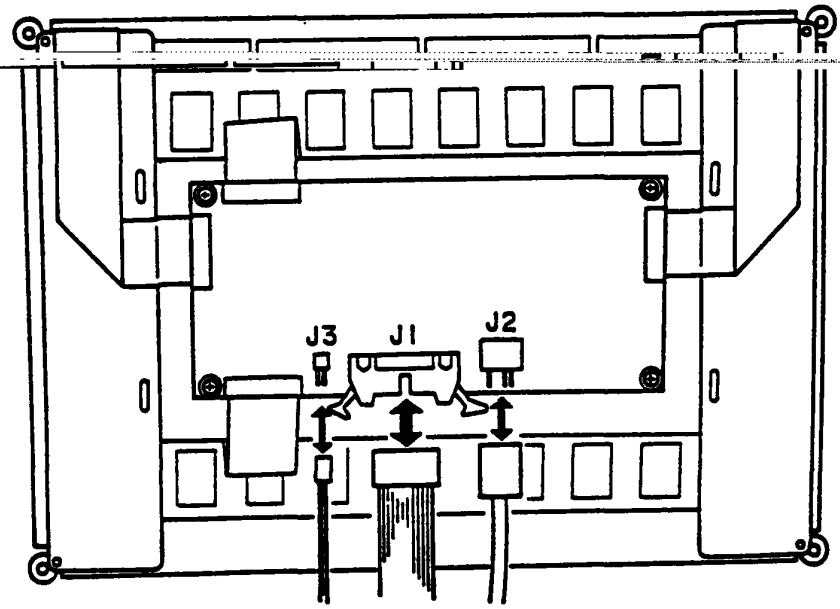


Figure 4-42 Connector Check

Are the connectors and cables connected correctly & securely ?

Yes: Go to **DISPLAY-15.**

No: Correct then and repeat the T&D operation to verify.

Voltage check

1. Check the power voltage at the PDP connector for the appropriate voltage with AVO meter.

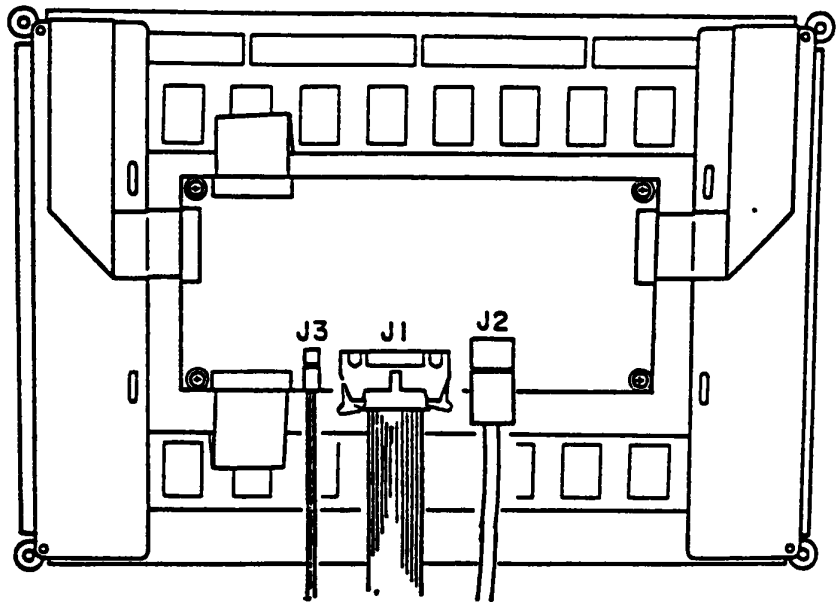


Figure 4-43 Voltage Check

Voltage Tolerance

Connector	Pin		Voltage		
	+ Lead	- Lead	Nomal Vdc	Min Vdc	Max Vdc
J 2	1	2	+ 5	+ 4.9	+ 5.1
	3	2	+ 205	+ 185	+ 225
J 1	13,14	2,4,15	+ 5	+ 4.9	+ 5.1

Are the voltages in tolerance ?

Yes: Go to **DISPLAY-16.**

No: Go to **POWER.**

Plasma Display PCB replacement

1. Turn OFF the power switch of the System Unit.
2. Replace the suspected Plasma Display PCB with a good spare Plasma Display PCB.
3. Turn ON the power switch of the System Unit.
4. Repeat the T&D operation to verify it.

Does the failure remain ?

Yes: The Plasma Display PCB is good. Go to **DISPLAY-17.**

No: The Plasma Display PCB is faulty.

Plasma Display Panel Replacement

1. Turn OFF the power switch of the System Unit.
2. Replace the suspected Plasma Display Panel with a good spare Plasma Display Panel.
3. Turn ON the power switch of the System Unit.
4. Repeat the T&D operation to verify it.

Does the failure remain ?

Yes: The Plasma Display Panel is good. Another Unit may be suspected.

No: The Plasma Display Panel is faulty.

Ext. FDD
(5.25" External Floppy Disk Drive)

You have reached this TIP since Ext. FDD (External FDD) is suspected of the cause of the failure.
For the trouble shooting, you will need one good spare 5.25" Ext. FDD for the replacement.

External FDD is composed of following components.
You will isolate the faulty component from them in this TIP.

External FDD components

* FDD assembly
* FDD PCB (FDD5C1)
* Ni-Cd Battery Unit
* AC Adaptor
* Ext. FDD Cable

You need to prepair the following tools for this TIP.

Tools

* AVO meter
* MS-DOS System Disk (including T&D program file)
* Work Disk (formatted)
* Spair Ext. FDD Unit and Ext. FDD Cable
* Cleaning Disk (5.25")
* Screwdriver (phillips screwdriver)

Start from **Ext. FDD-1** for any trouble-shooting of Ext. FDD.

Set up for the FDD test

1. Connect the Ext. FDD cable to the T3100 System and the Ext. FDD.
2. Connect the AC adaptor to the Ext. FDD, and plug in AC plug of the AC adaptor to a wall-outlet.
3. Set the PRT/FDD select switch of the T3100 System to PRT position.
4. Insert the MS-DOS disk (including T&D program file) to the Int. FDD of the T3100 System.
5. Turn ON the power switches of the T3100 System & the Ext. FDD, then run the FDD test program according to the operation procedure of T&D (PART 8: TEST & DIAGNOSTICS).

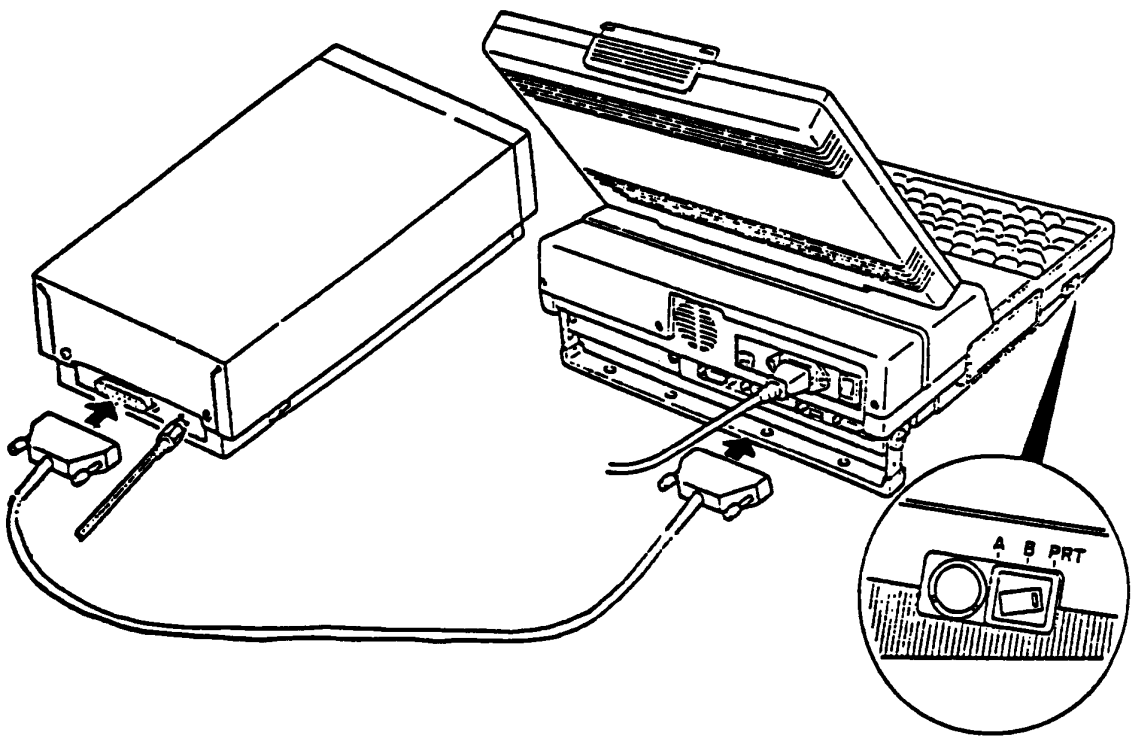


Figure 4-44 Set the External FDD

Go to **Ext. FDD-2.**

FDD test menu

1. Proceed the T&D program to FDD test menu (FDD test menu is as follow).

2. Set the PRT/FDD select switch of the System Unit to "A" position.

3. Insert the good 5-inch work disk (error free) into the Ext. FDD.

4. Run all subtests of the FDD test program according to the T&D program operation procrdure. (refer to PART 8: TEST & DIAGNOSTICS)
   Following figure is an example screen of FDD Test program.

```
FLOPPY DISK                              501000


SUB-TEST   : 01
PASS COUNT: 00000      ERROR COUNT: 00000
WRITE DATA: 00         READ  DATA : 00
ADDRESS    : 000000    STATUS     : 000

SUB-TEST MENU :

01 - Sequential read
02 - Sequential read/write
03 - Random address/data
04 - Write specified address
05 - Read specified address
99 - Exit to DIAGNOSTIC TEST MENU



SELECT SUB-TEST NUMBER  ? 01
TEST  LOOP (1:YES/2:NO) ? 2
ERROR STOP (1:YES/2:NO) ? 1
```

Does any error message apperar?

Yes: Clean the Read/Write head of the Ext. FDD with cleaning disk. For head cleaning, insert a cleaning disk to the Ext. FDD then select "HEAD CLEANING" on a DIAGNOSTIC MENU of T&D program. (refer to PART 8: TEST & DIAGNOSTICS)
If it leads you here again, go to **Ext. FDD-3** .

No: The Ext. FDD is good.

Voltage check

Check the voltages of the Ext. FDD as following.

1. Turn OFF the power switches of the T3100 System Unit and Ext. FDD.

2. Open the upper cover of the Ext. FDD. (Refer to PART 5: REPLACEMENT/ADJUSTMENT)

3. Turn ON the power switch of the Ext. FDD, then check the voltages for the FDD assembly by a AVO meter.
   (All check points are shown in the Tables on next page.)

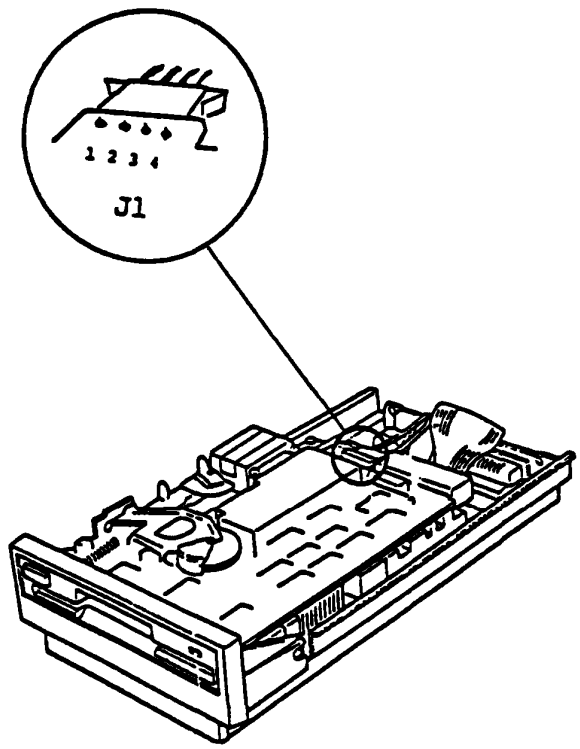


Figure 4-45 Voltage Check

To be continued.

Voltage check (continued)

Voltage Tolerances

Connector	Pin		Voltage		
	+Lead	-Lead	Normal Vdc	Min Vdc	Max Vdc
J1	1	2,3	+12	+11.5	+14.5
	4		5	+ 4.5	+ 5.3

Are the voltages within the torelance.

Yes: Go to **Ext. FDD-5**

No: Go to **Ext. FDD-4.**

Voltage check

If the voltages to FDD assembly are not in tolerance, one of the AC adaptor, FDD PCB or Ni-Cd battery is suspected.
Check all of them by a AVO meter as follows.

Note: Ni-Cd batter must be charged at least for an hour before the check.

1. Turn OFF the power switch of the Ext. FDD then pull out the DC plug of the AC adaptor from the Ext. FDD.

2. Check the voltage at the battery connector on the FDD PCB. (All check points are shown in the tables on next page.)

3. Check the output voltage of the AC adaptor at DC plug.

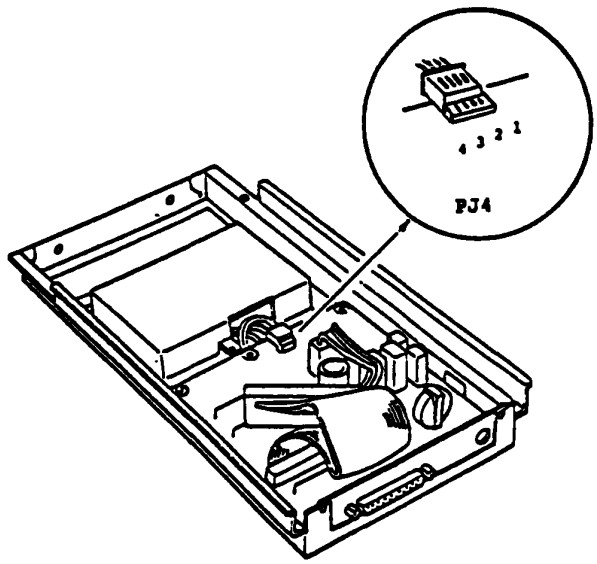


Figure 4-46 Voltage Check

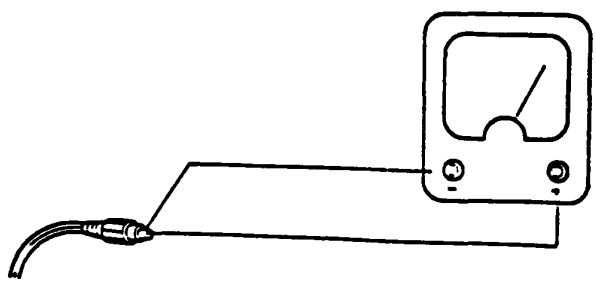


Figure 4-47 AC Adaptor

To be continued.

Voltage check (continued)

Voltage Tolerances

Output of Ni-Cd Battery

Connector	Pin		Voltage
	+Lead	-Lead	
PJ4	1,2	3,4	More than 12 Vdc

Output of AC adaptor

Pin		Voltage		
+Lead	-lead	Normal Vdc	Min Vdc	Max Vdc
Inner Contact	Outer Contact	+20	+18	+22

If output voltage of Ni-Cd battery is out of tolerance:
==> Change the battery.

If output voltage of AC adaptor is out of tolerance:
==> Change the AC adaptor.

If both output voltages of the battery & the AC adaptor are in the tolerance:
==> Change the FDD PCB.

Connector & jumper strap check

1. Check all connectors of the suspected FDD assembly whether they are connected properly and securely.
2. Check the jumper strap settings on the FDD assembly PCB.

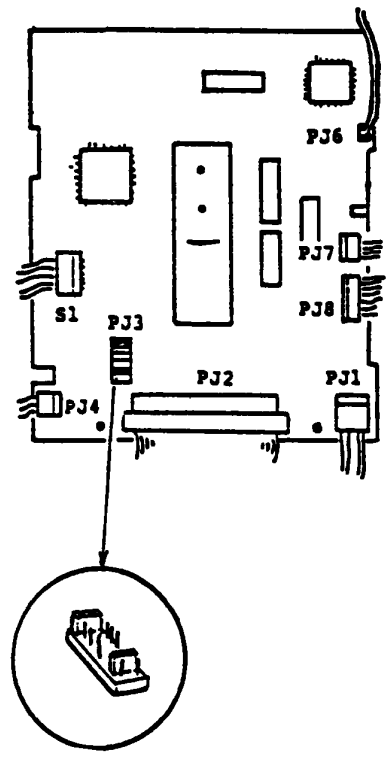


Figure 4-48 Jumper of FDD PCB

Are the connectors and jumper straps set properly?

Yes: Go to **Ext. FDD-6.**

No: Set the connector or the jumper strap properly then repeat to run FDD test program to verify.
If it leads you here again, go to **Ext. FDD-6.**

FDD change

1. Turn OFF the power switches of the Ext. FDD & the T3100 System Unit.
2. Change the FDD assembly with a good one for checking.
3. Run FDD test program for the Ext. FDD.
   If an error occurs again, the FDD PCB (FFD5C1) or Ext. FDD cable are suspected.

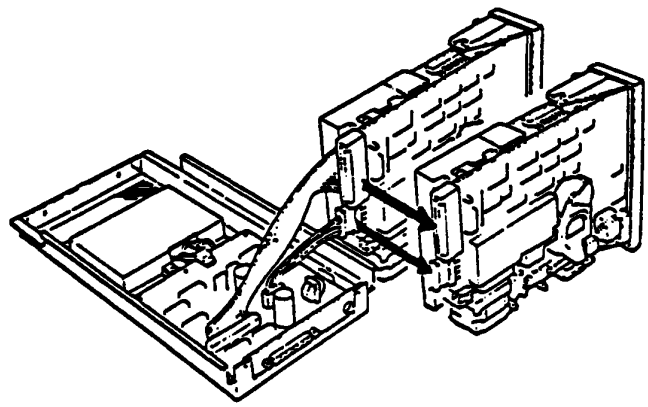


Figure 4-49 FDD Change

Does any error occurs?

Yes: Go to **Ext. FDD-7.**

No: The FDD assembly is faulty.
Change the FDD assembly with spare one.

FDD cable change

The FDD PCB and EXT. FDD cable are still suspected.
In this entry, you will isolate the faulty component from them.

1. Turn OFF the power switches of the Ext. FDD & the T3100 System Unit.
2. Change the Ext. FDD cable with good one for checking.
3. Turn on the power switches of the Ext. FDD and the T3100 System Unit then run the FDD test program for Ext. FDD.

External FDD Unit

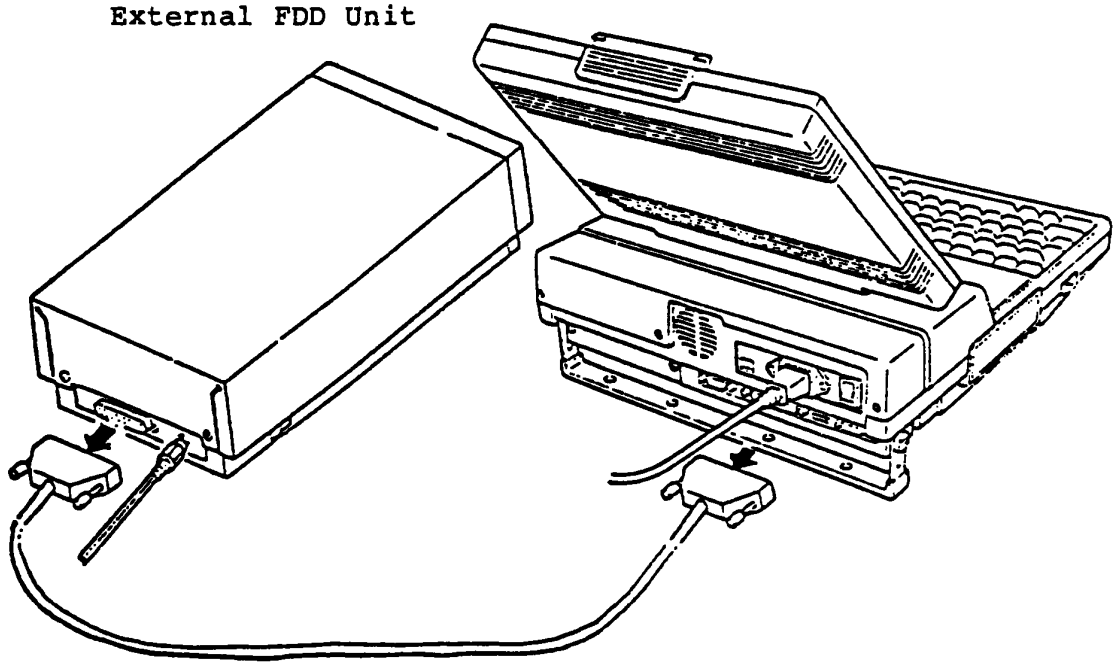


Figure 4-50 FDD Cable Change

Does any error occurs?

Yes: Go to **Ext. FDD-8.**

No: The Ext. FDD cable is faulty.
Change the Ext. FDD cable with spare one.

FDD PCB change

The FDD PCB is suspected.
Change the FDD PCB (FFD5C1) refering to PART 5: REPLACEMENT /ADJUSTMENT.

1. Turn OFF the power switches of the Ext. FDD and the T3100 System Unit.

2. Replace the Ext. FDD PCB then run FDD test program for the Ext. FDD.

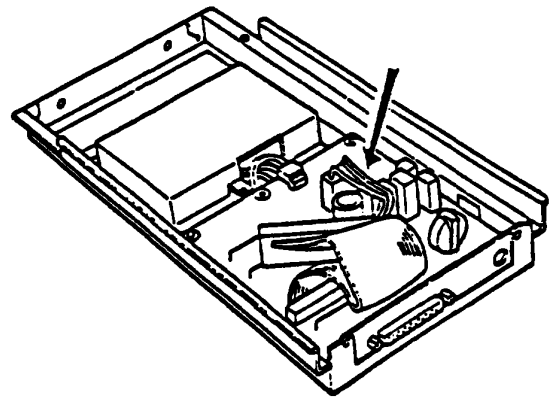


Figure 4-51 FDD PCB Change

Does any error occurs?

Yes: Ext. FDD UNIT is good.
The System board of the T3100 System Unit is suspected.
Go to the TIP of **System PCB.**

No: The FDD PCB of the Ext. FDD is faulty.
Change the FDD PCB.

5.1 BEFORE REMOVAL/REPLACEMENT

PREPARE

1. Turn OFF the power switch of the System Unit then remove all connectors on the rear panel of the System Unit.

2. To stand the handle, pull it straightly (from the view point where you face the rear panel), turn it to the downward and push it into the groove vertically.

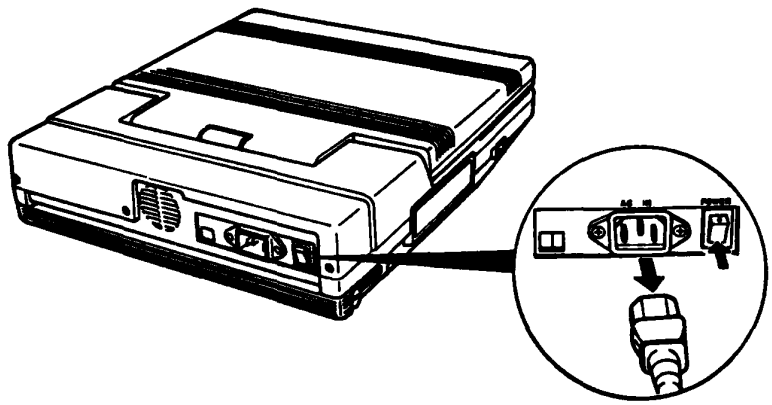


Figure 5-1 Turn OFF the Power

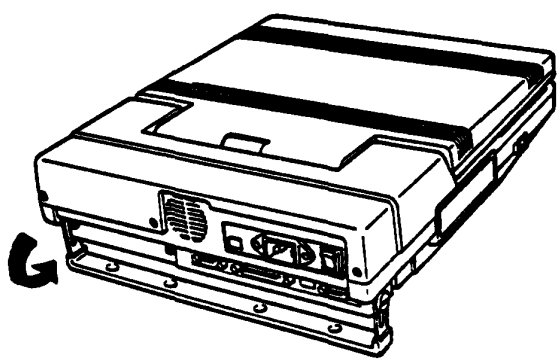


Figure 5-2 Stand the Handle

5.2 DISASSENBLING OF THE SYSTEM UNIT CABINET

1. Stand the System Unit, then remove five screws (A) on the bottom of the System Unit.

2. Turn the System Unit to normal position, then remove the three screws (B) on the rear panel (C) of the System Unit.

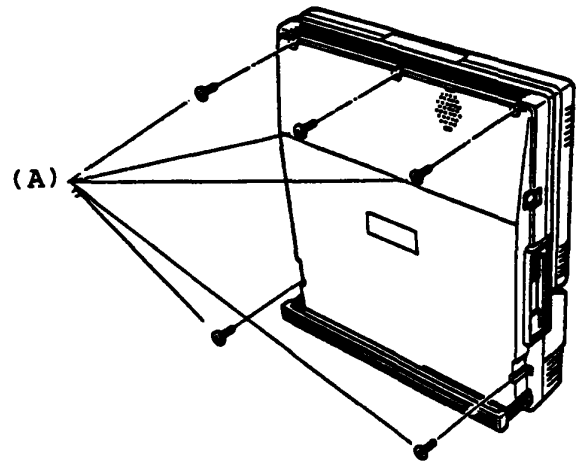


Figure 5-3 Remove Five Screws

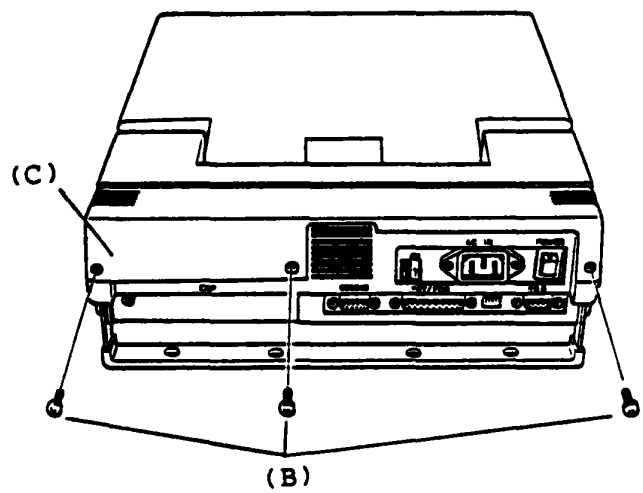


Figure 5-4 Remove Three Screws

4. Turn the Upper Cover (D) to the left side by lifting it.

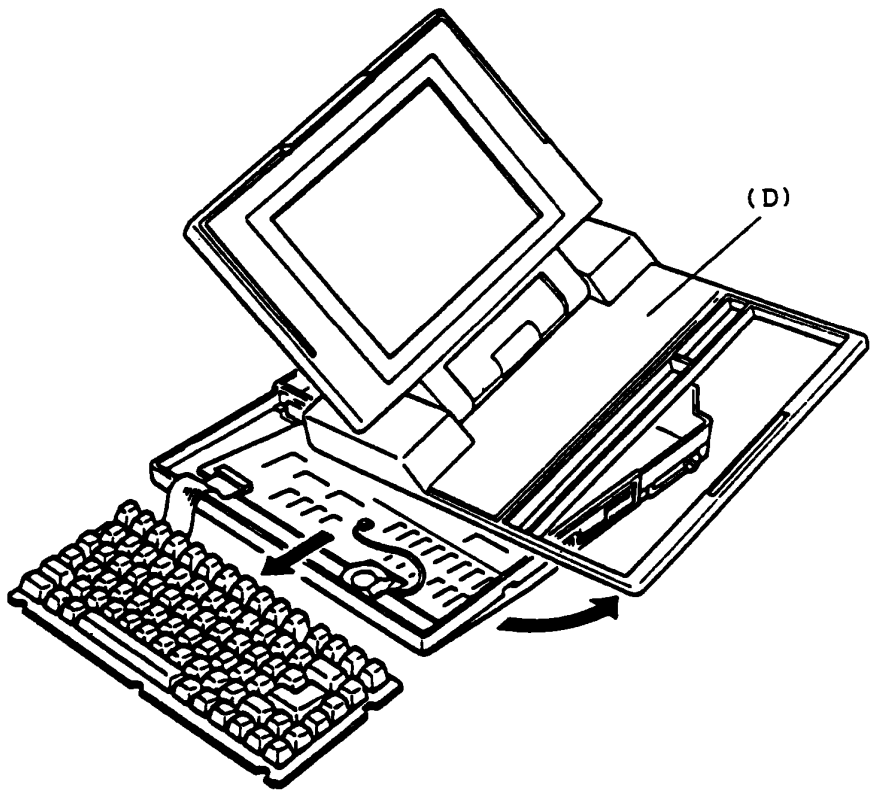


Figure 5-5 Lift Up the Upper Cover

REPLACEMENT

Follow the reverse procedure.

5.3 PDP MASK REMOVAL/REPLACEMENT

REMOVAL

1. Push the Latch (A) of the Plasma Display, then open the Plasma Display.

2. Peel the indicater seal (B) with a pair of tweezers and remove from Plasma Display Panel (PDP) Mask (C).
   Note: Repeating of removal and replacement of the seal will make it's adhensiveness to be in effective.

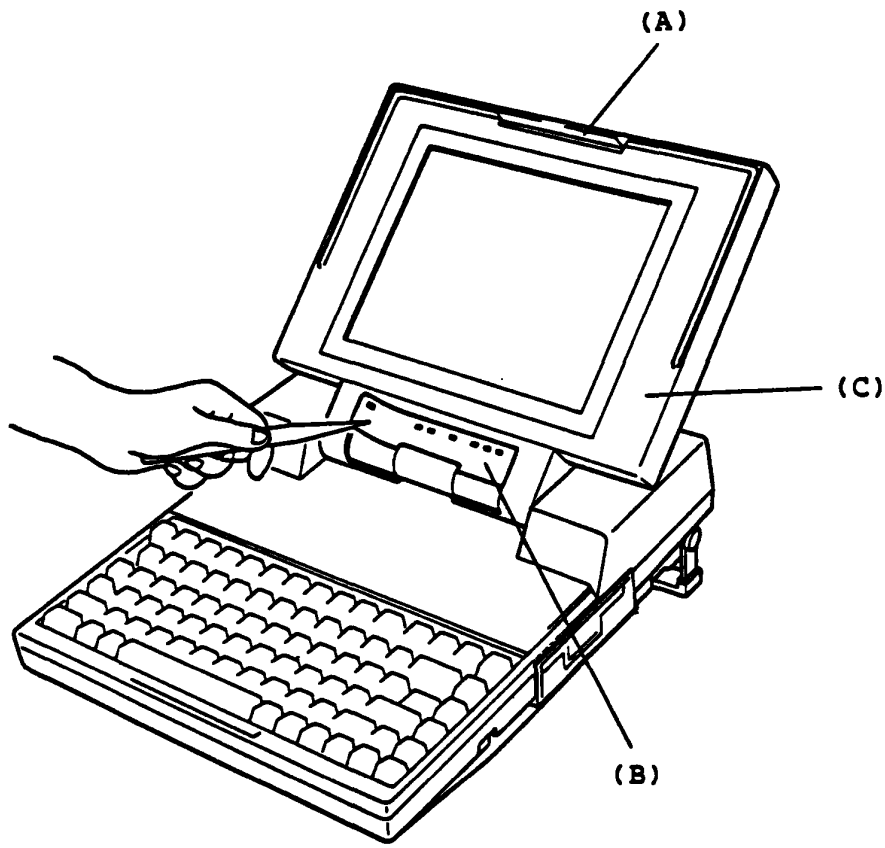


Figure 5-6 Peel the Indicater Seal

To be continued.

3. Remove two Screws (D) on the Plasma Display Panel (PDP) Mask (C).

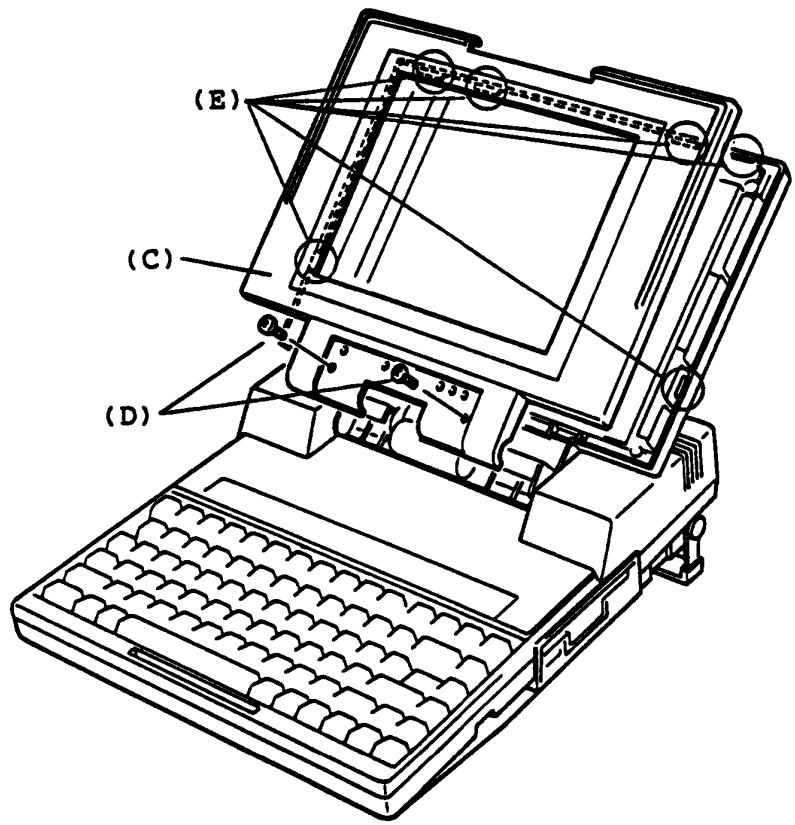


Figure 5-7 PDP Mask Removal

REPLACEMENT

Follow the reverse procedure.
Confirm that the six nails (E) of PDP Cover get into the PDP Mask (C).

5.4 COVER LATCH REMOVAL/REPLACEMENT

REMOVAL

1. Remove the PDP Mask from the PDP Shield Board (A).
   (See section 5.3)

2. Pinch off the Latch (B) from the PDP Shield Board (A) by fingers.

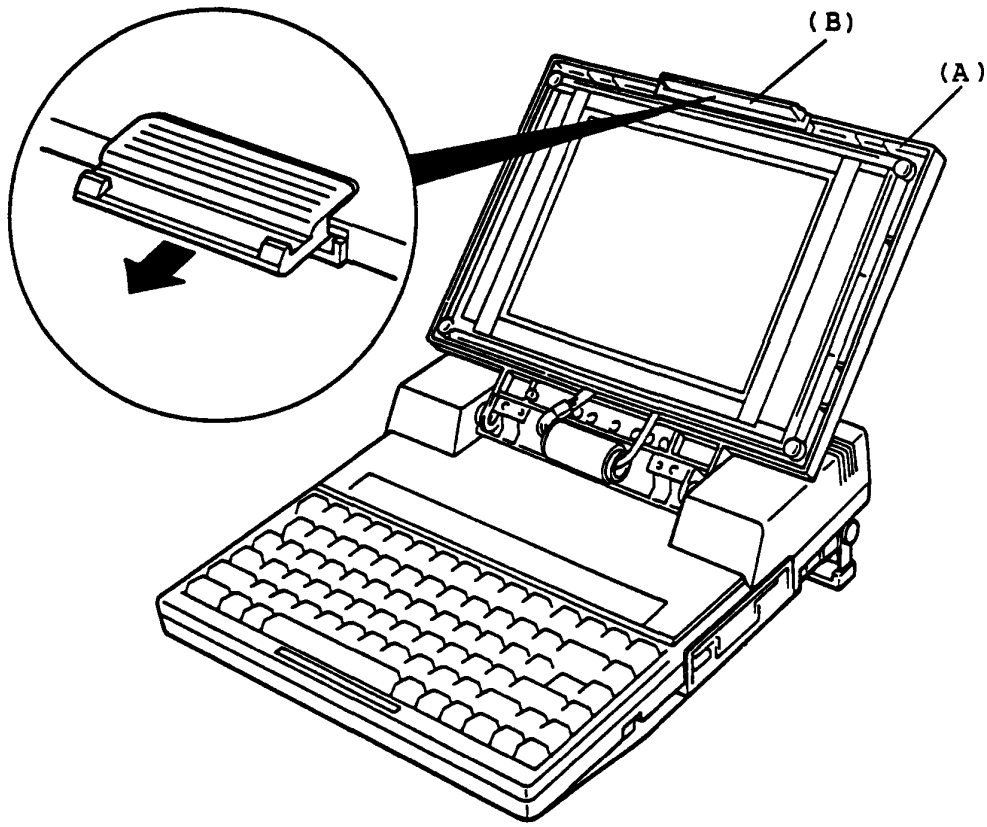


Figure 5-8 Latch Removal

REPLACEMENT

Follow the reverse procedure.

5.5 PDP REMOVAL/REPLACEMENT

WARNING : Dangerous high voltage is surppried to the PDP.
Pay enough attention on handling.
It takes few minuts after Power off to the discherge the electricity.

REMOVAL

1. Remove the PDP Mask from the PDP Shield Board.
(See section 5.3)

2. Remove four tap screws (A) on the PDP.

3. Lift up the PDP, then put it on the Keyboard Unit.

4. Disconnect the three cables (B) from the rear of PDP (C) to remove.

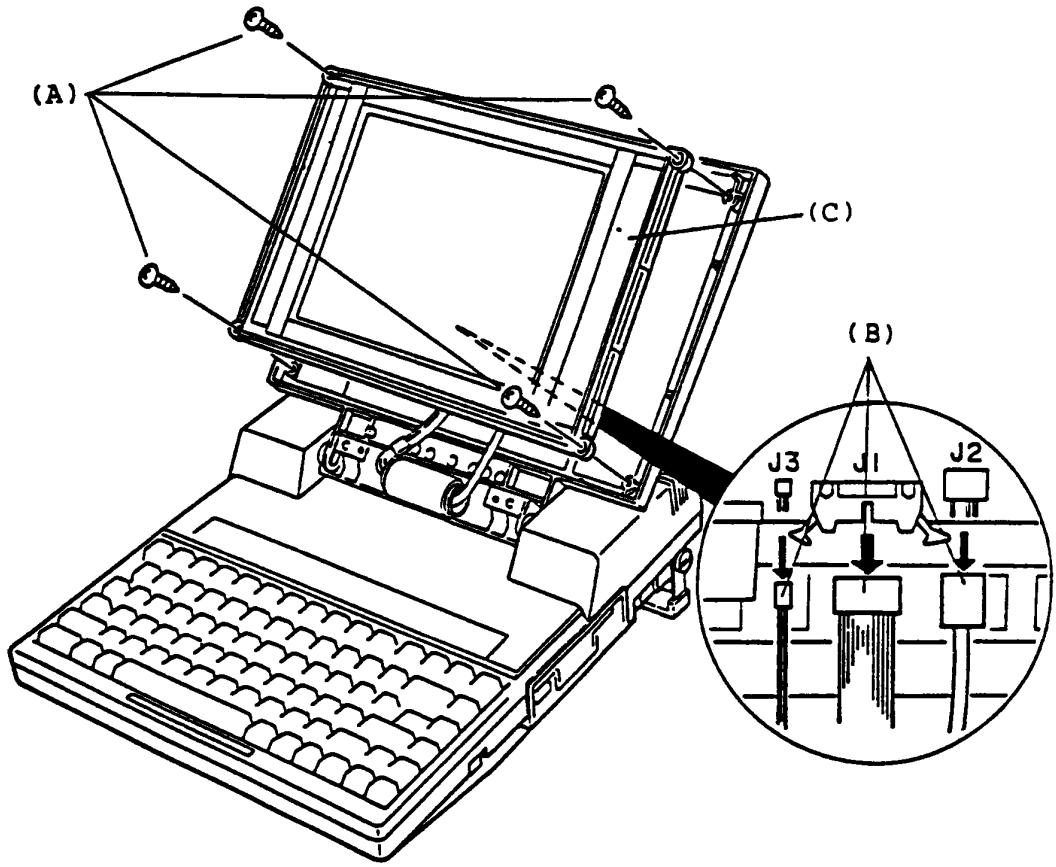


Figure 5-9 PDP Removal

REPLACEMENT

Follow the reverse procedure.

5.6 INDICATOR BOARD and CABLE GUIDE REMOVAL/REPLACEMENT

REMOVAL

1. Remove the PDP Mask and PDP. (See section 5.3 and 5.4)
2. Pull the ground cable (A) from the PDP Shield Board.
3. Lift up the indicater board and disconnect a Indicater cable (B) from the Indicater board to remove.
4. Take off the five cables from Cable Guide (C), then remove the Cable Guide.

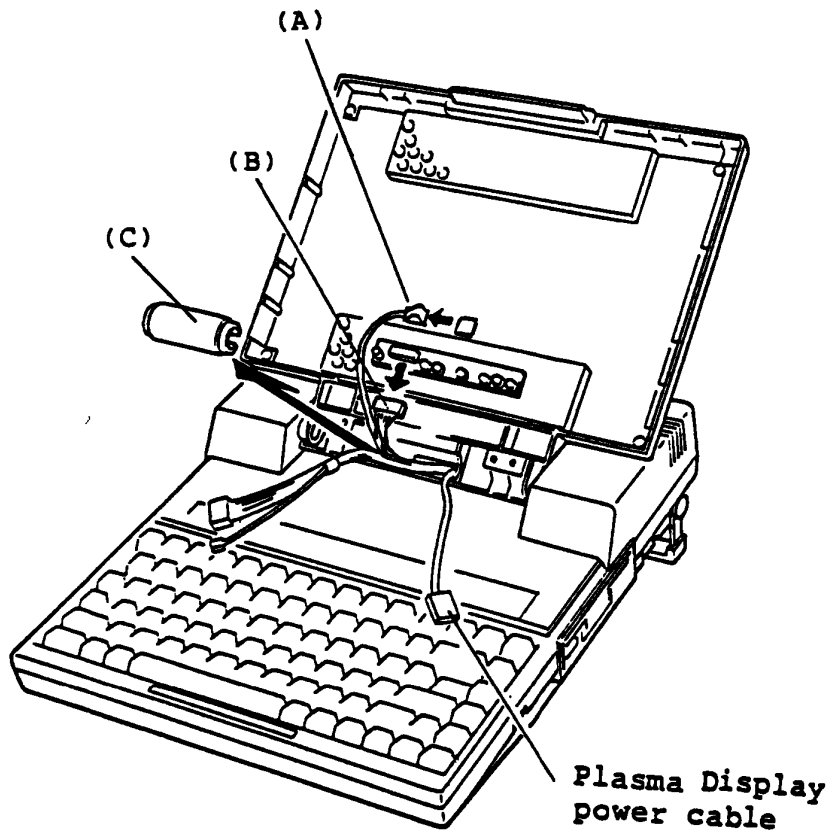


Figure 5-10 Indicater Board and Cable Guide Removal

REPLACEMENT

Follow the reverse procedure.
When you set the five cables to Cable Guide, separate Plasma Display power cable (right) from another cables (left).
A thick part of Cable Guide is on the upper side.

5.7 PDP COVER REMOVAL/REPLACEMENT

REMOVAL

1. Remove the PDP Mask, PDP, Indicater Board and Cable Guide. (See section 5.3 - 5.5)
2. Remove two screws (A) from the two hinges (B).
3. Sift two hinges (B) to inside, then remove it.

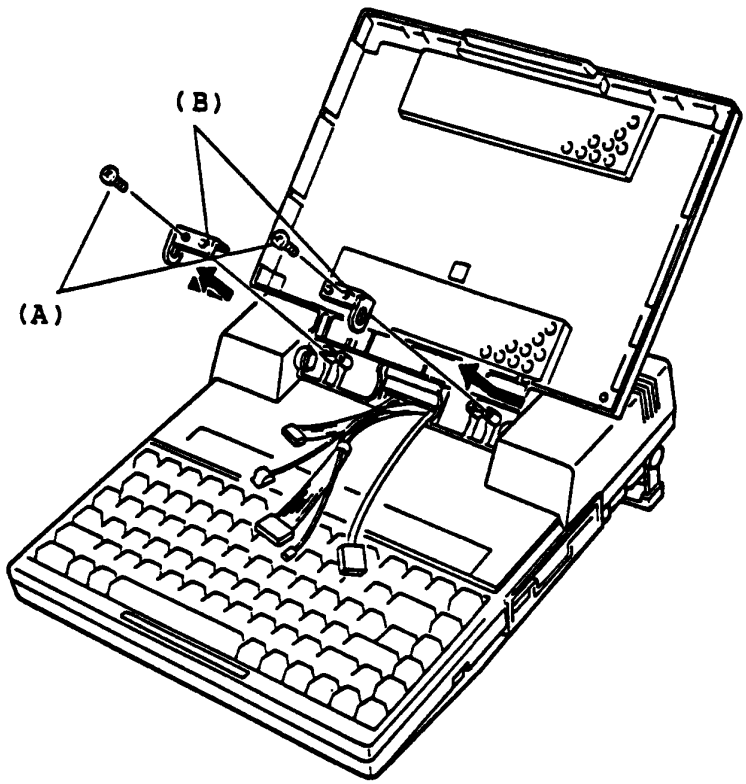


Figure 5-11 Hinges Removal

To be continued.

4. To remove the PDP Shield Board (C), turn the rear cover down then lift it up.

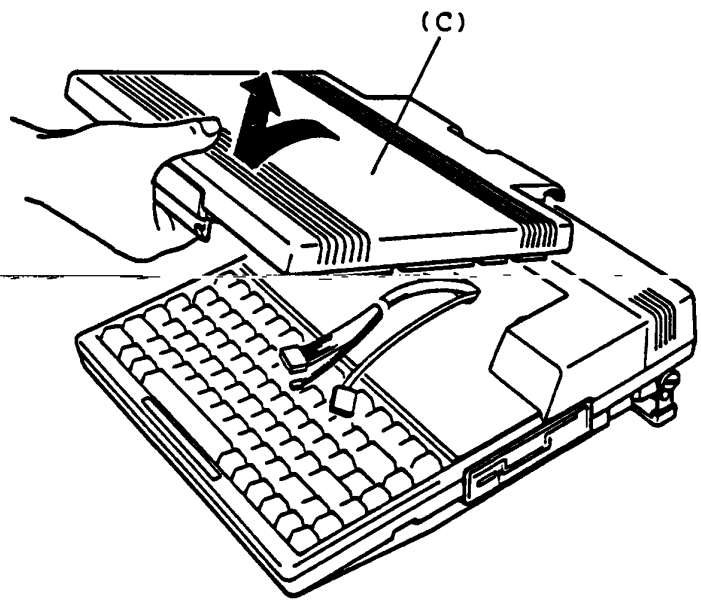


Figure 5-12 Rear Cover of Plasma Display Removal

REPLACEMENT

Follow the reverse procedure.

5.8 UPPER COVER REMOVAL/REPLACEMENT

REMOVAL

1. Before Upper Cover removal, remove the Plasma Display Unit. (See section 5.3 - 5.6)

2. Stand the System Unit, then remove the five screws (A) on the bottom of the System Unit. (Refer to Fugire 5-3)

3. Turn the System Unit to normal position, then remove the three screws (B) on the rear panel (C).

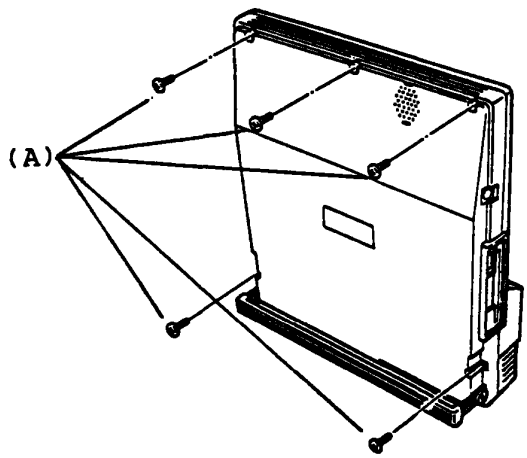


Figure 5-13 Remove Five Screws

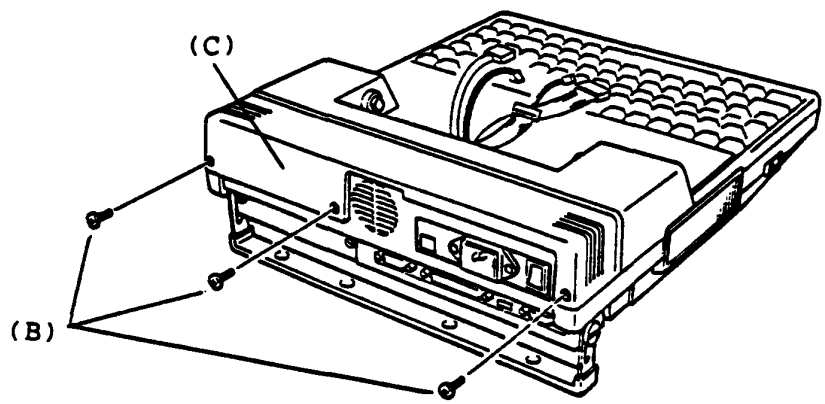


Figure 5-14 Remove Three Screws

To be continued.

4. Take a front of the Upper Cover (D), then lift up it.

5. Pass the cable through a slit the upper cover to remove the Upper Cover (D).

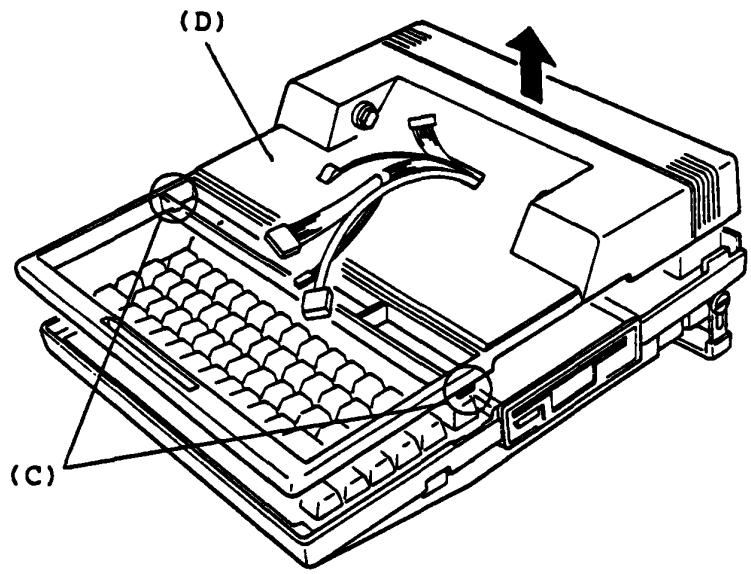


Figure 5-15 Remove the Upper Cover

REPLACEMENT

Follow the reverse procedure.
Confirm that the two nails (C) of Lower Cover get into Upper Cover.

5.9 KEYBOARD REMOVAL/REPLACEMENT

REMOVAL

1. Disassemble the System cabinet and slide the Upper Cover backward. (See section 5.2)

2. Lift up the keyboard unit and put it in front of the System Unit.

3. Pull the pressure plate (A) from connector, then pull out the keyboard cable from the System PCB (B) to remove it.

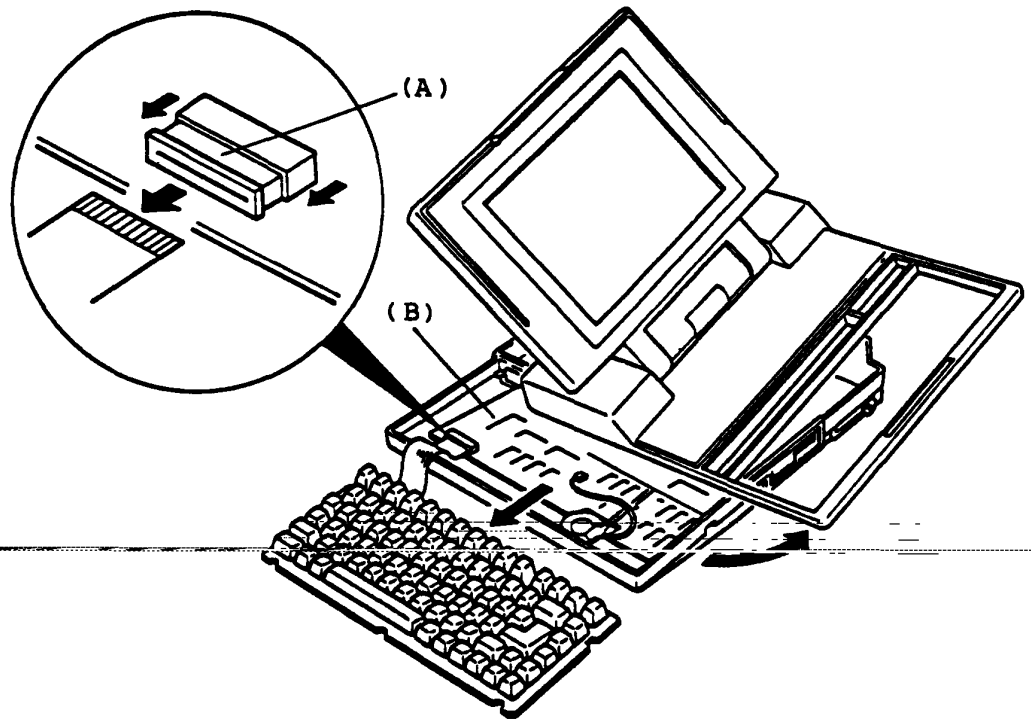


Figure 5-16 Keyboard Unit Removal

REPLACEMENT

Follow the reverse procedure.
The keyboard cable (flat cable) is fixed to the keyboard connector with pressure plate. To connect the keyboard connector insert the cable into the connector then press the pressure plate securely.

5.10 SPEAKER AND BATTERY REMOVAL/REPLACEMENT

REMOVAL

1. Disassemble the System cabinet and slide the Upper Cover backward. (see section 5.2)

2. Put the keyboard unit side. (see section 5.9)

3. Disconnect the speaker cable (A) from the System PCB (B).

4. The speaker (C) is mounted on the lower cover with a locking lever.
   Push the locking lever outward so that the speaker is free to move then pull out the speaker from the lower cover.

5. Disconnect the Battery cable (D) from the System PCB (B).

6. Lift up the Battery (E) to remove it.

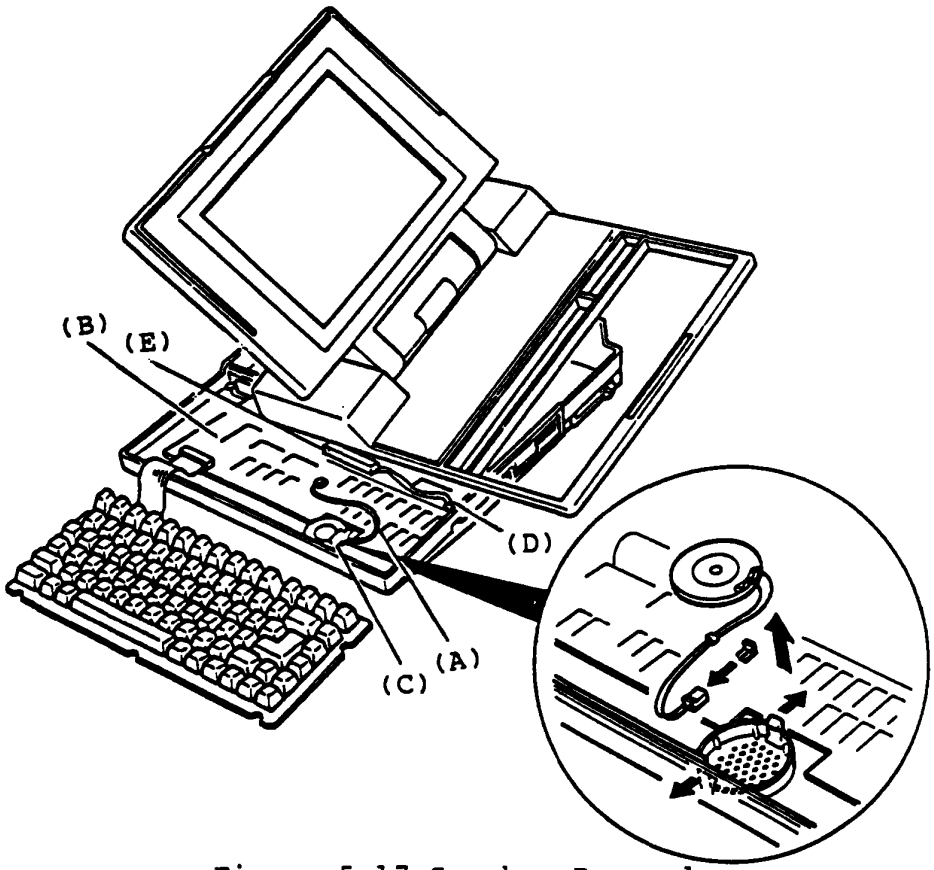


Figure 5-17 Speaker Removal

REPLACEMENT

Follow the reverse procedure.

5.11 MEMORY CARD REMOVAL/REPLACEMENT

REMOVAL

1. Disassemble the System cabinet and slide the Upper Cover backward. (see section 5.2)

2. Lift up the Keyboard unit, then put in the front of the System Unit. (see section 5.9)

3. Pull out the Memory Card (A) from the System PCB (B).

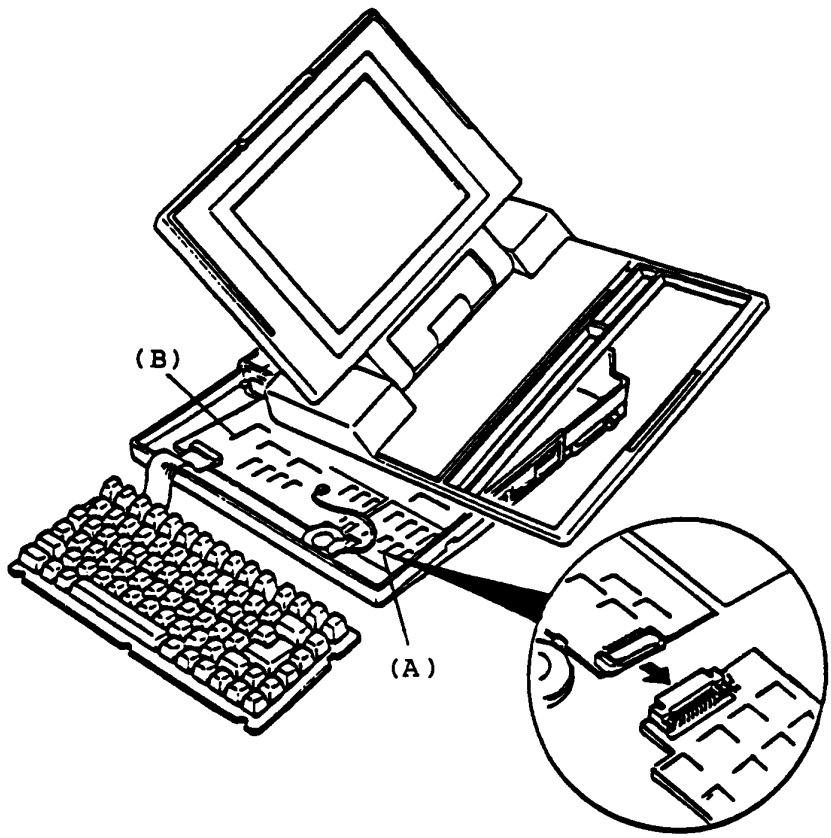


Figure 5-18 Memory Card Removal

REPLACEMENT

Follow the reverse procedure.

5.12 POWER SUPPLY UNIT REMOVAL/REPLACEMENT

WARNING : Dangerous high voltage is suppried to the Power Supply Unit. Pay enough attention on handling.
It takes few minutes after Power off the discherge the electricity.

REMOVAL

1. Remove the Plasma Display Unit and the Upper Cover. (see section 5.3 - 5.6)
2. Remove the three screws (A)(B)(C), then remove the Power Supply Unit Cover (D).
   Note: GND cable (E) is fixed screw (A) to Power Supply Unit Cover (D). Screw (C) has one washer.

3. Remove the five screws (F) and spread between Power Supply Unit and rear panel of Lower Cover, then lift up the Power Supply Unit.
   Note: Power Supply Cable (G) is fixed adhesive tape to Disk Support (H).

4. Disconnect two cables from the System PCB (I) to remove it.

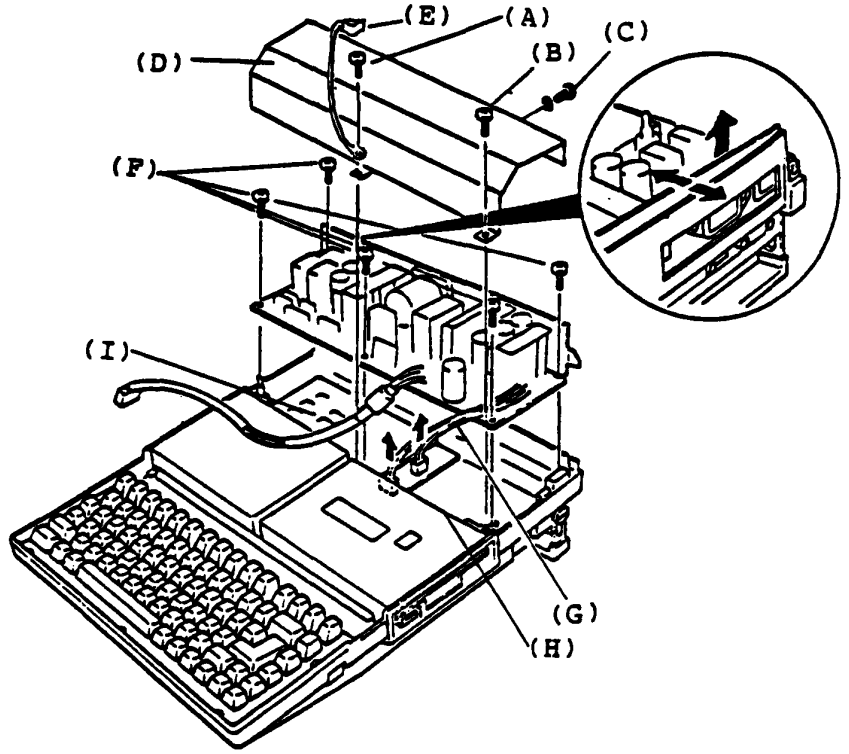


Figure 5-19 Power Supply Unit Removal

REPLACEMENT

Follow the reverse procedure.

5.13 POWER SUPPLY UNIT ADJUSTMENT

Following is a procedure to adjust the voltage of +5V DC for optimum value. It might be done before the installation of new Power Supply Unit to the System Unit.

1. Plug in AC Power cord to the Power Supply Unit and wall outlet.

2. Set the dummy load resister (2 ohm, 20 W) to the System PCB power connector. (from pin-1 to pin-3 or from pin-2 to pin-4)

3. Turn ON the power switch of Power Supply Unit.

4. Check the voltage of +5V DC power at pins of the power connector for System PCB by an AVO meter.

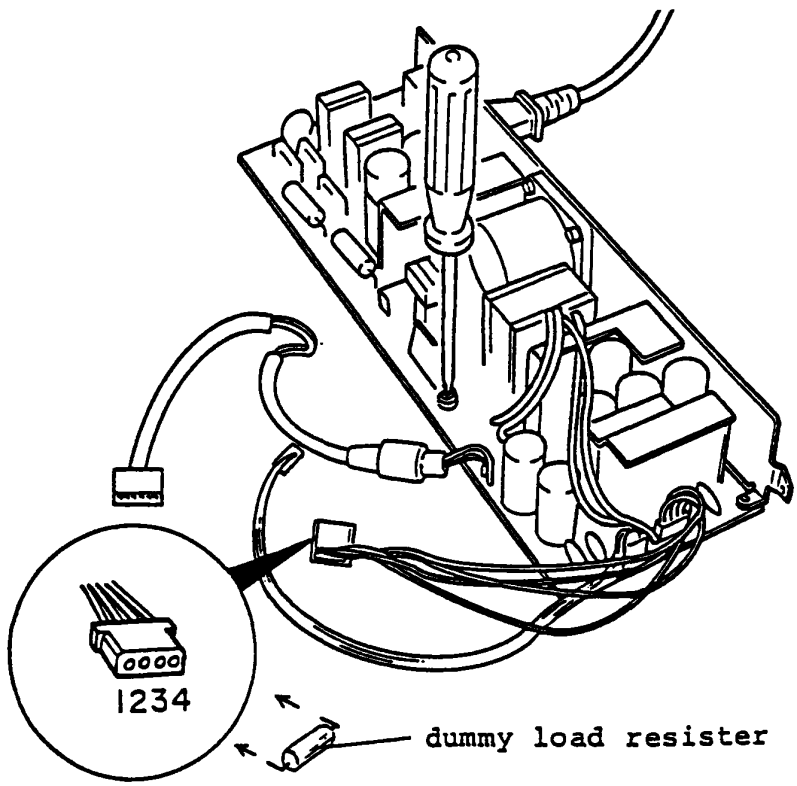


Figure 5-20 Power Supply Adjustment

System PCB connector

Pin		Voltage	
+ Lead	- Lead	Min Vdc	Max Vdc
1 , 2	3 , 4	+ 4.75	+ 5.25

5.14 COOLING FAN REMOVAL/REPLACEMENT

REMOVAL

1. Remove the Plasma Display Unit and Upper Cover. (See section 5.3 - 5.6)

2. Remove the Power Supply Unit. (See section 5.12)

3. Disconnect the Cooling Fan cable (A) from the Power Supply PCB (B).

4. Remove the three screws (C) from the Cooling Fan (D).
   Note: Screws (C) has six washers (E), three spacers (F) and three nuts (G).

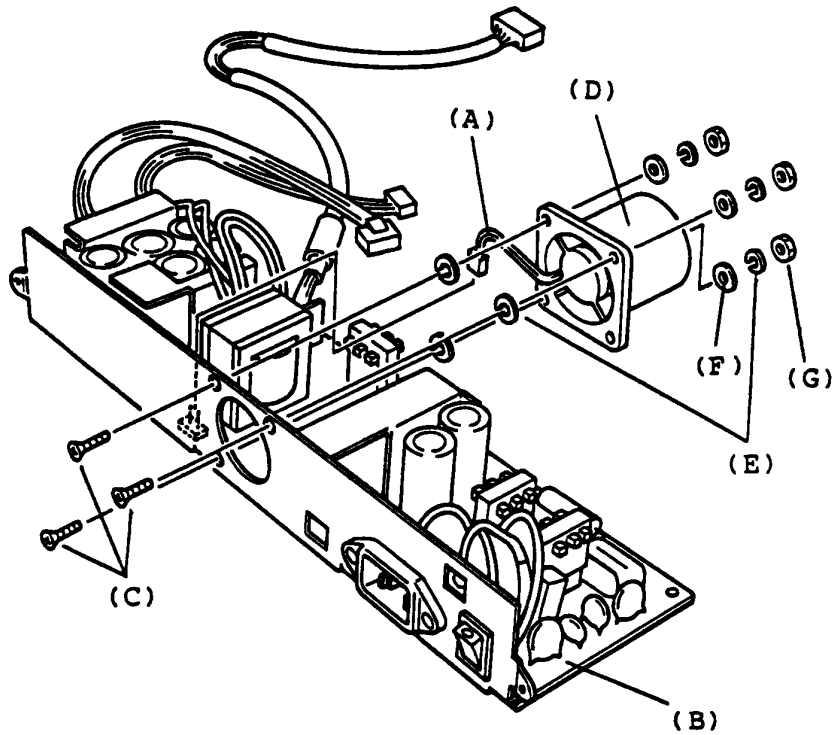


Figure 5-21 Colling Fan Replacement

REPLACEMENT

Follow the reverse procedure.

5.15 HDC REMOVAL/REPLACEMENT (Only F/H type)

REMOVAL

1. Remove the Plasma Display Unit.
   (See section 5.8, 5.12 and 5.14).

2 Remove the Upper Cover and Power Supply Unit
   (See section 5.7 and 5.12)

3. Remove the two screws (A) on the HDC PCB (B).

4. Unplug the connector of the HDC PCB on the System PCB (C) to remove.

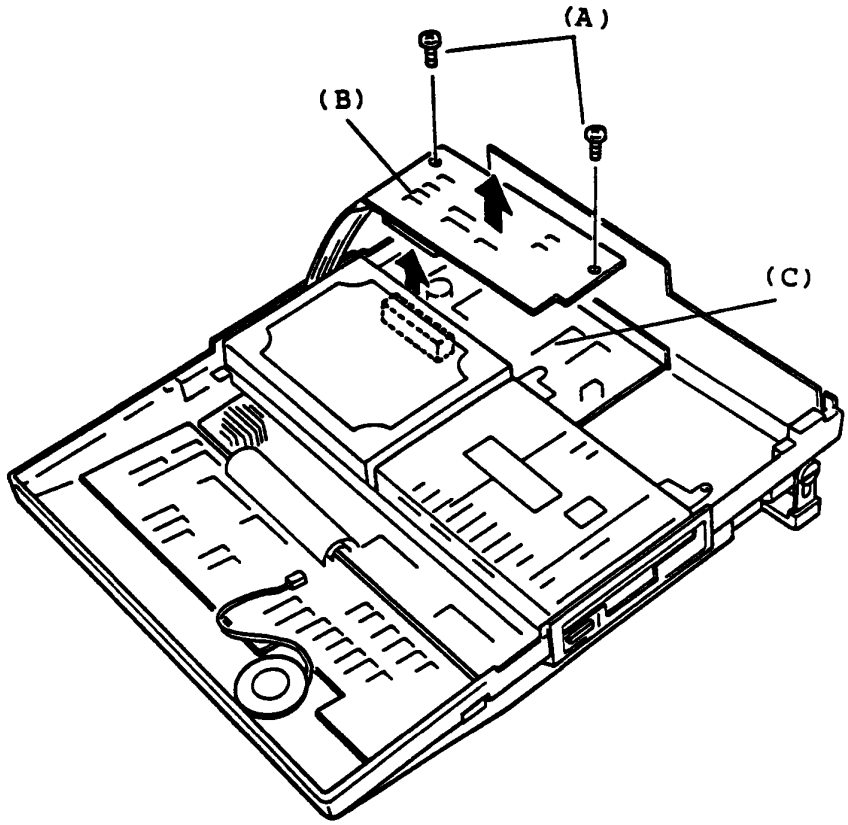


Figure 5-22 HDC PCB Removal

REPLACEMENT

Follow the reverse procedure.

5.16 FDD (or FDD and HDD) REMOVAL/REPLACEMENT

REMOVAL

1. Remove the Plasma Display Unit and Upper cover.
   (See section 5.3- 5.7)

2. Remove the Keyboard Unit and the Power Supply Unit.
   (See section 5.8 and 5.12)

3. Remove four tap screws (A) of the Disk Support (B).

4. Lift up the Disk Support, then disconnect FDD (HDC) cable from the System PCB (C) to remove the FDD (FDD and HDD).
   (NOTE) In the case of F type is one FDC cable.
   In the case of F/F type is two FDC cable.

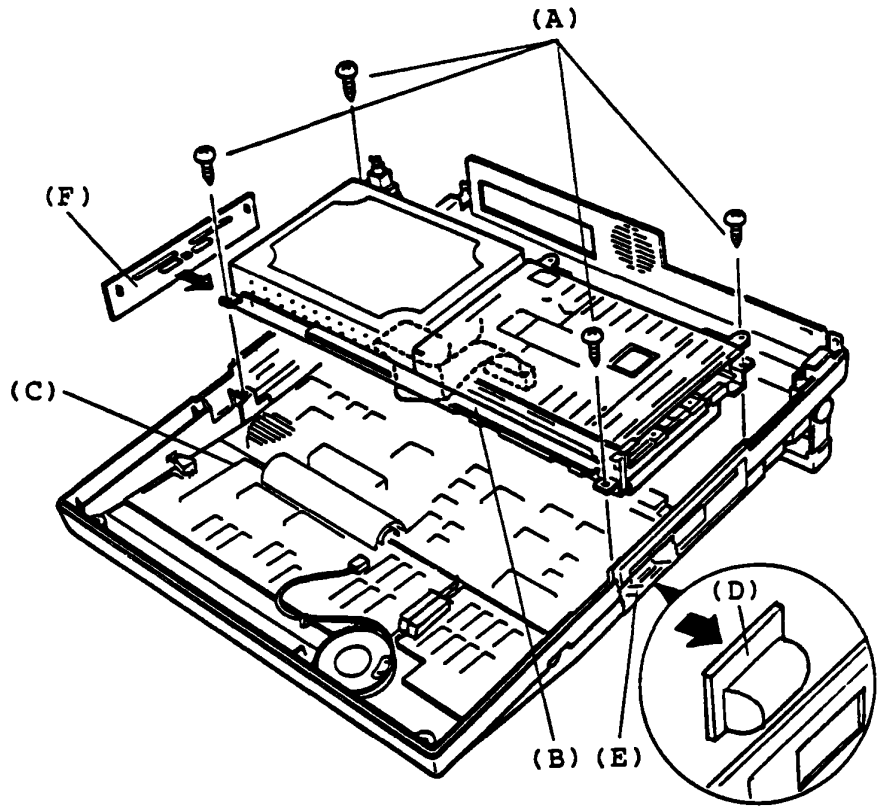


Figure 5-23 Disk Support Removal

REPLACEMENT

Follow the reverse procedure.
When you fit the Eject button to Lower Cover, set the above (D).
(Refer to Figure 5-23)
Fix the Eject button to Lower Cover using adhesive tape(C).
In the case of the System Unit change from F/H type to F/F type, remove the Mask plate (D).

To be continued.

In the case of F/F type

6. Each FDD (F) unit is mounted on the Disk Support with three screws as below.

7. Turn the FDD Unit upside down then remove three screws.

8. Pass the FDD 1 cable through a slit of Disk Support to remove.

9. In the case of FDD 2, note two option FDD metal fittings (A) to remove.

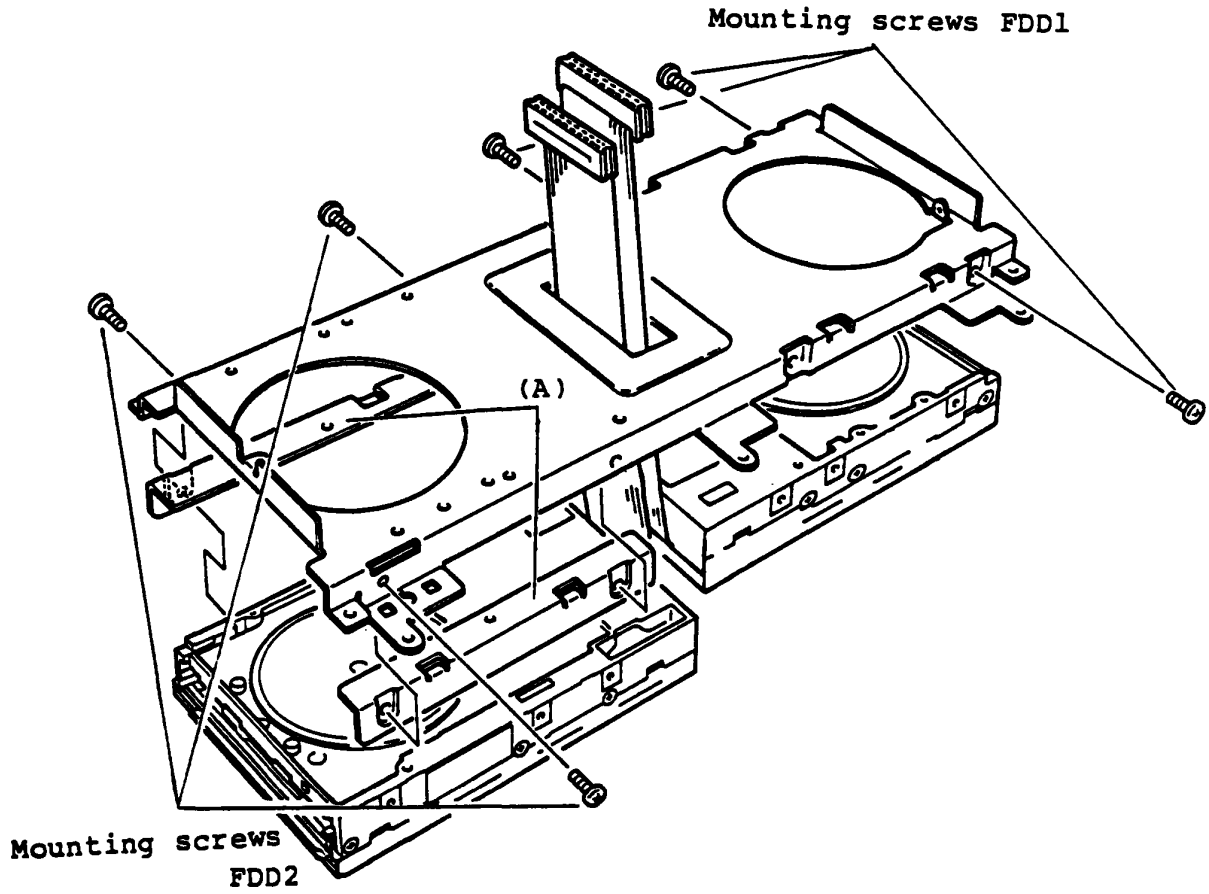


Figure 5-24 FDD Removal

REPLACEMENT

Follow the reverse procedure.
In the case of the System Unit change from F/H type to F/F type, fit up the two option FDD metal fittings.

In the case of F/H type.

6. FDD (F) and HDD (H) unit are monuted on the Disk Support with six screws as below.

7. For FDD removal, see previous page.

8. For HDD removal, turn the Disk Support upside down then remove the three screws (A) on the Disk Support to remove.

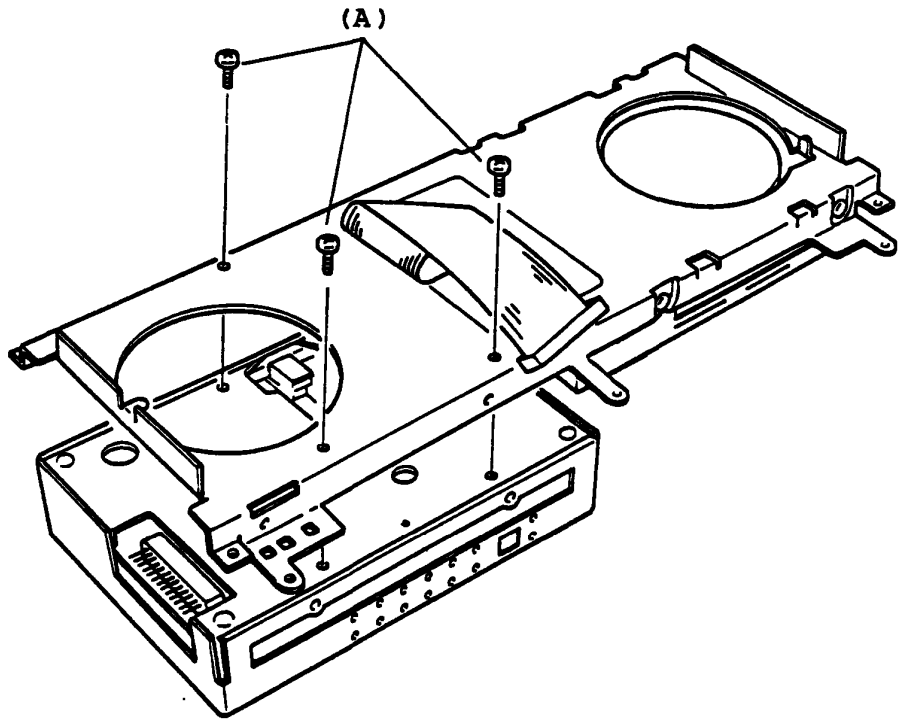


Figure 5-25 HDD Removal

REPLACEMENT

Follow the reverse procedure.

5.17 SENSOR GUIDE REMOVAL/REPLACEMENT

REMOVAL

1. Remove the Plasma Display Unit and Upper Cover. (See section 5.3 - 5.7)

2. Remove the Keyboard Unit and the Power Supply Unit. (See section 5.8 and 5.12)

3. Remove the Disk Support. (See section 5.15)

4. Push the two positions (A) of the Sensor Guide, then lift up the Sensor Guide.

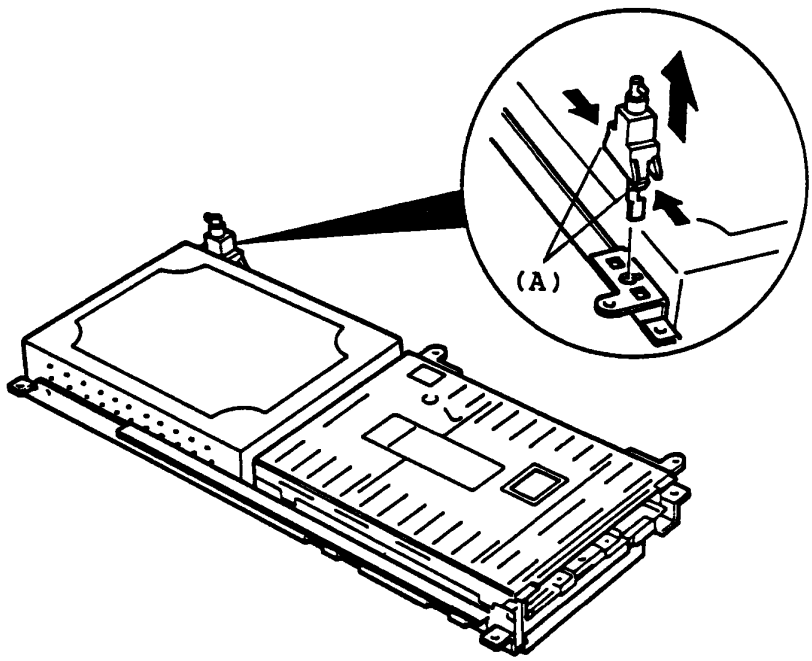


Figure 5-26 Sensor Guide Removal

REPLACEMENT

Follow the reverse procedure.
Note: Note the direction of the Sensor Guide when you repeat it.

5.18 SYSTEM PCB REMOVAL/REPLACEMENT

REMOVAL

1. Remove the Plasma Display Unit and the Upper cover.
   (See section 5.3 - 5.7)

2. Remove the Keyboard, Power Supply Unit, HDC (Only F/H type) and FDD (or FDD and HDD) Unit.
   (See section 5.8 and 5.12 - 5.15)

3. The System PCB is mounted to the Lower Cover of the System Unit with ten screws (A) (B) on the System PCB and one screw (C) on the rear panel.
   Remove the eleven screws (A) (B).
   Note: In the case of the F/H type System, screws (B) are spacer screws.

4. Lift up the System PCB to remove.
   (NOTE) Can not disconnect the PDP (Plasma Display Unit) on the System PCB.

5. Peel the Insulater (D) to remove.

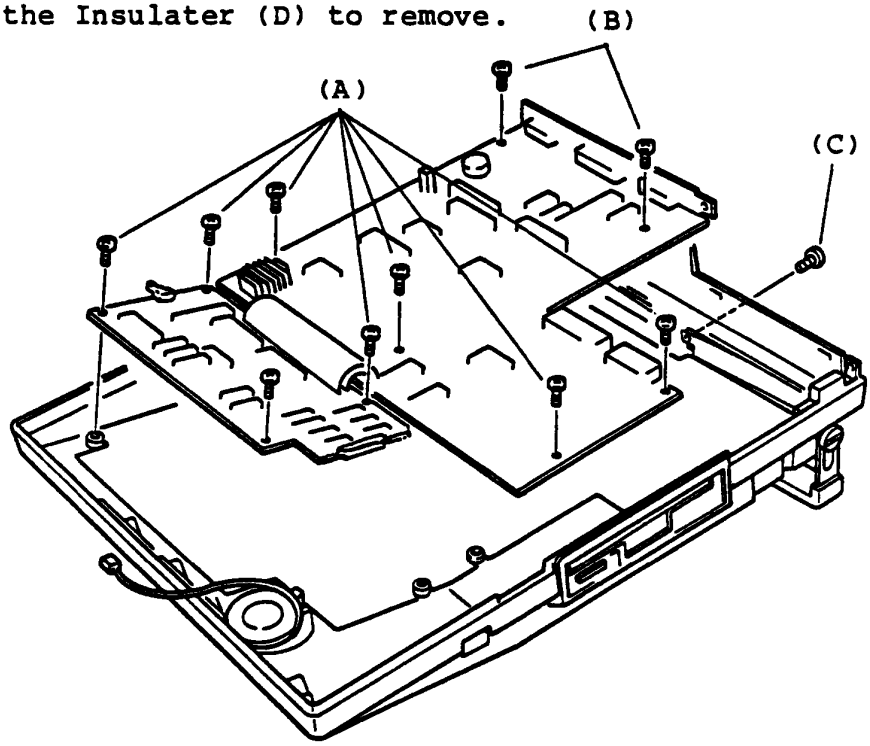


Figure 5-27 System PCB Removal

REPLACEMENT

Follow the reverse procedure.
You need to set the DIP switch of new System PCB properiy after replacement. (Refer to page 1-10)

5.19 HANDLE REMOVAL/REPLACEMENT

REMOVAL

1. Remove the two screws (A) on the both side of the Lower Cover, then remove the Handle Cover.

2. Pull the Handle backward to remove.

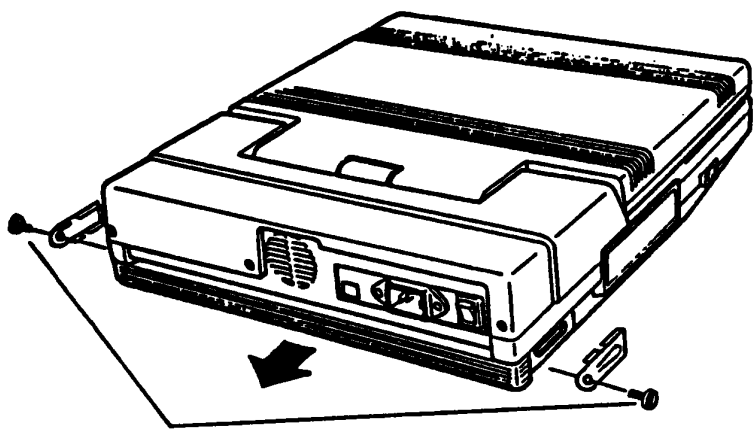


Figure 5-29 Handle Removal

REPLACEMENT

Follow the reverse procedure.

5.19 HANDLE REMOVAL/REPLACEMENT

REMOVAL

1. Remove the two screws (A) on the both side of the Lower Cover, then remove the Handle Cover.

2. Pull the Handle backward to remove.

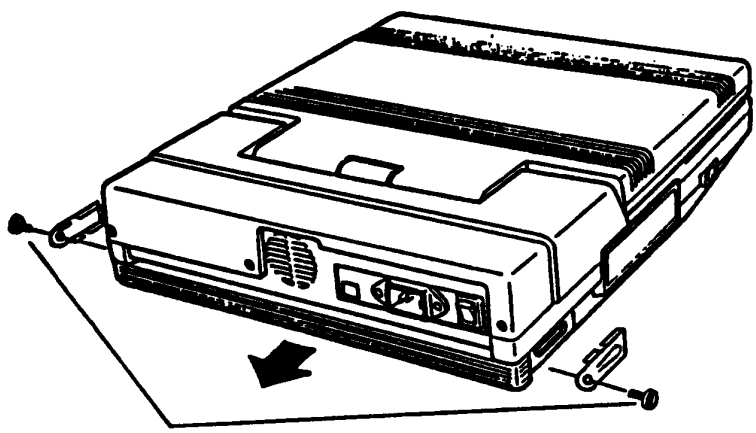


Figure 5-29 Handle Removal

REPLACEMENT

Follow the reverse procedure.

SYSTEM UNIT (Front View)

(A) System PCB

(B) Memory Card (Option)

(C) 3.5" Floppy Disk Drive
F/F type ... Two Floppy Disk Drive
F/H type ... One Floppy Disk Drive

(D) 3.5" Hard Disk Drive

(E) Keyboard

(F) Power Supply Unit

(G) Speaker

(H) Plasma Display

(I) Upper Cover

(J) Lower Cover

(K) Modem Card or I/O Expansion Card (Option)

(L) Battery

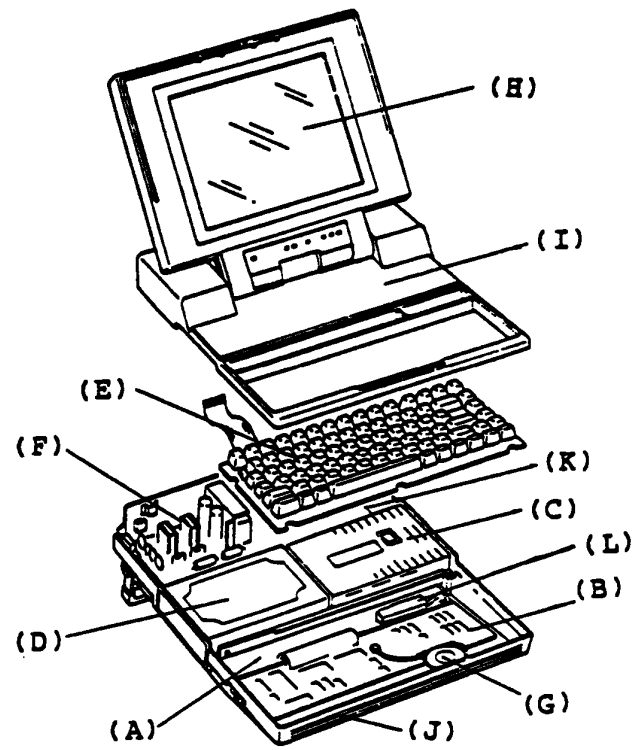


Figure 6-1 Front View of System Unit

SYSTEM UNIT (Rear Panel)

(A) Cooling Fan

(B) Power Switch

(C) AC Jack

(D) 115V/230V Select Switch

(E) Display Connector (for Color Display)

(F) DIP Switch

(G) Printer or Expansion FDD Connector

(H) RS232C Cable Connector

(I) Modem Card or I/O Expansion Card Slot

(J) Printer or FDD Select Switch

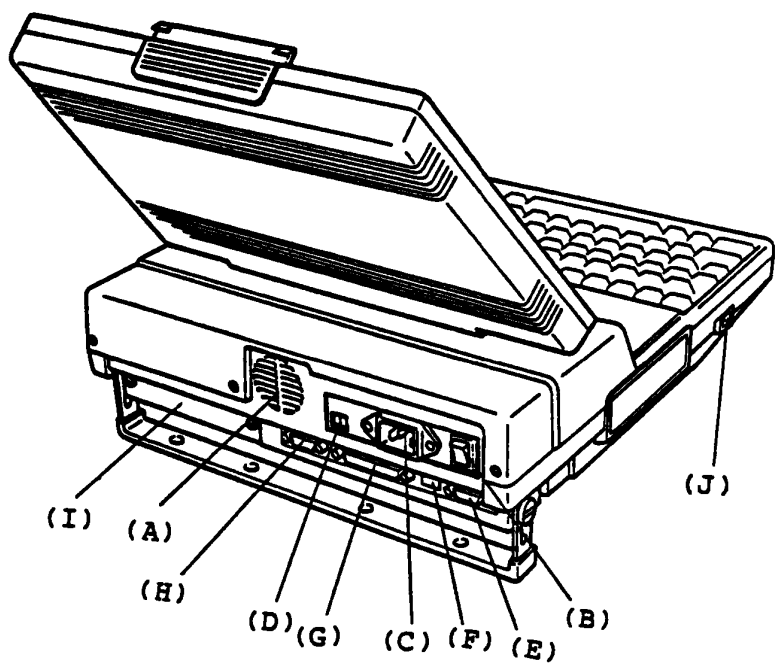


Figure 6-2 Rear Panel of System Unit

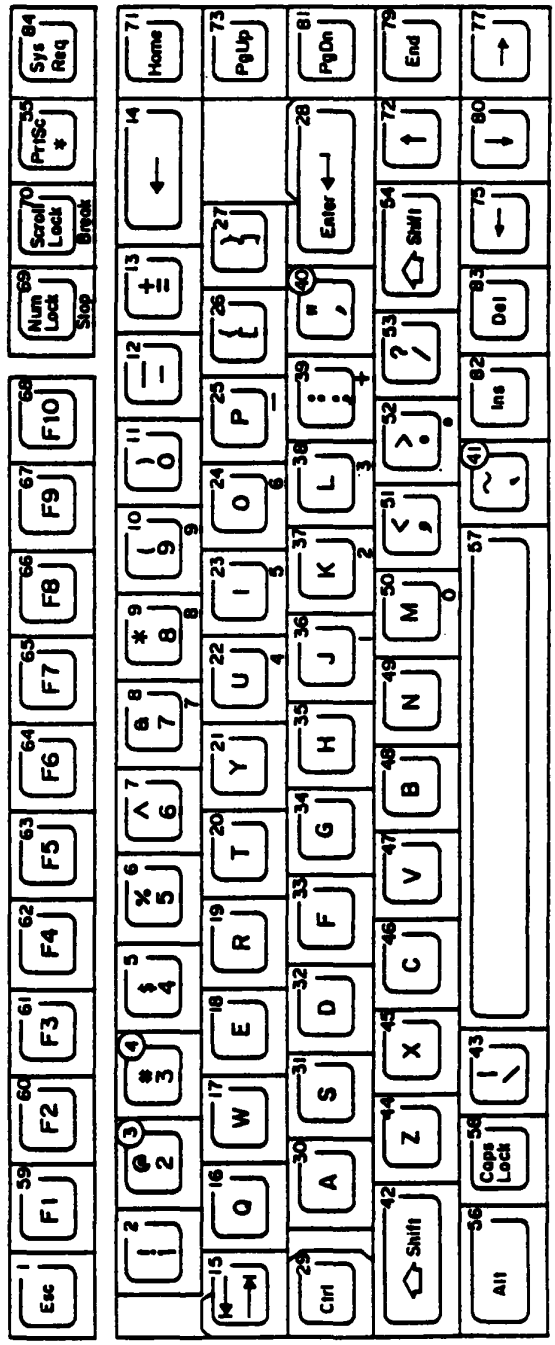


Figure 6-3 U.S.A. Version

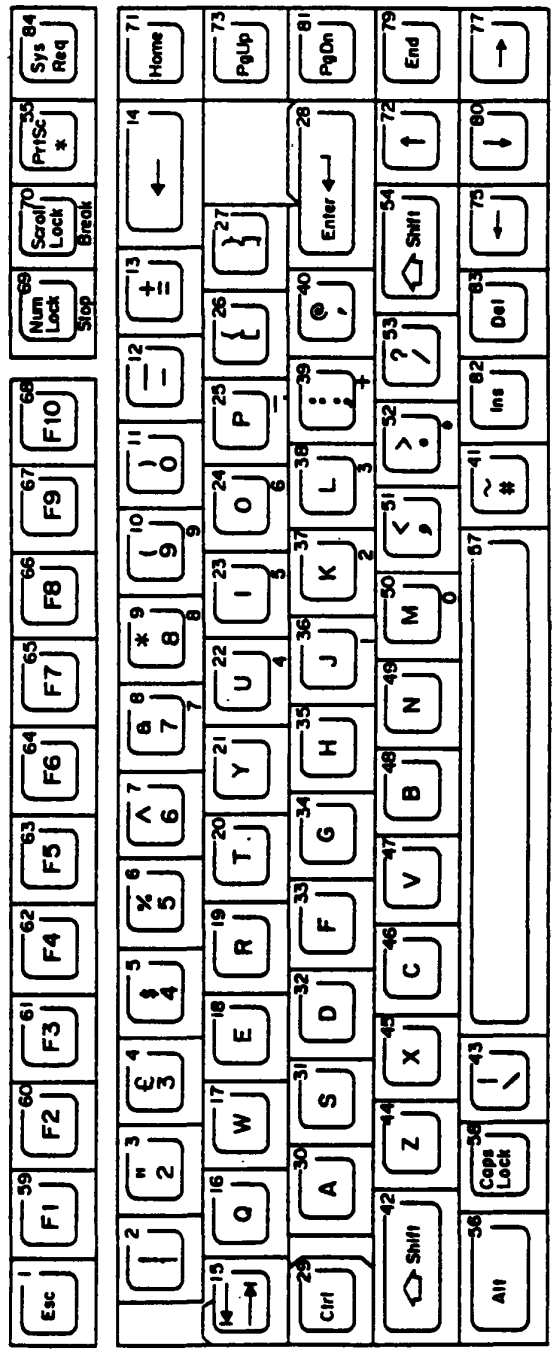


Figure 6-4 U.K. Version

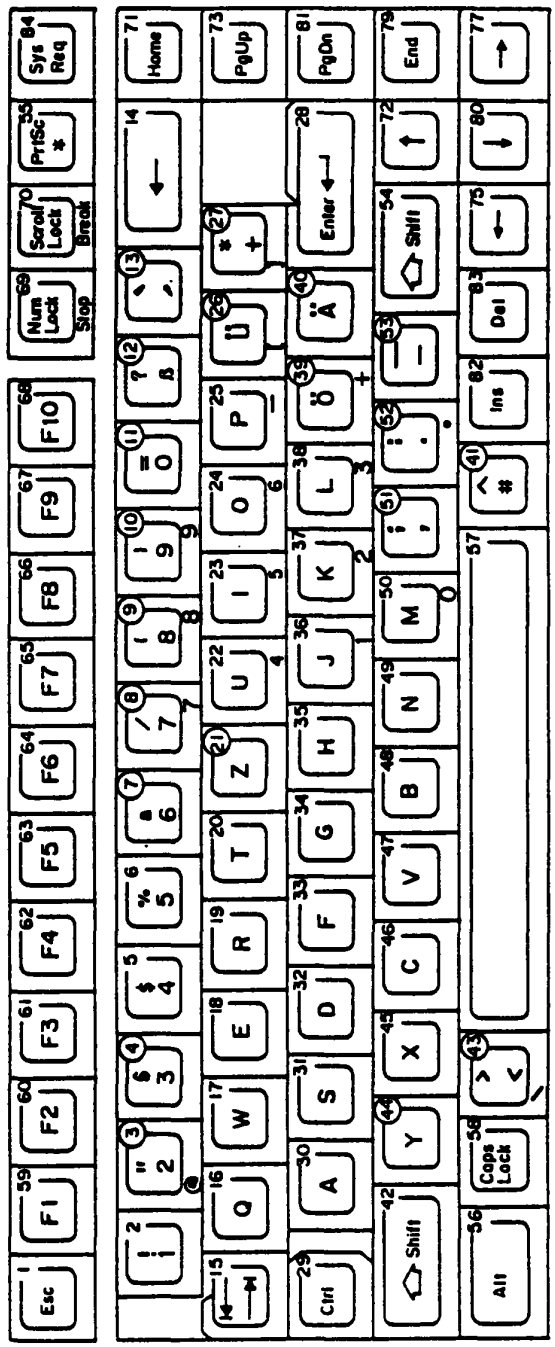


Figure 6-5 German Version

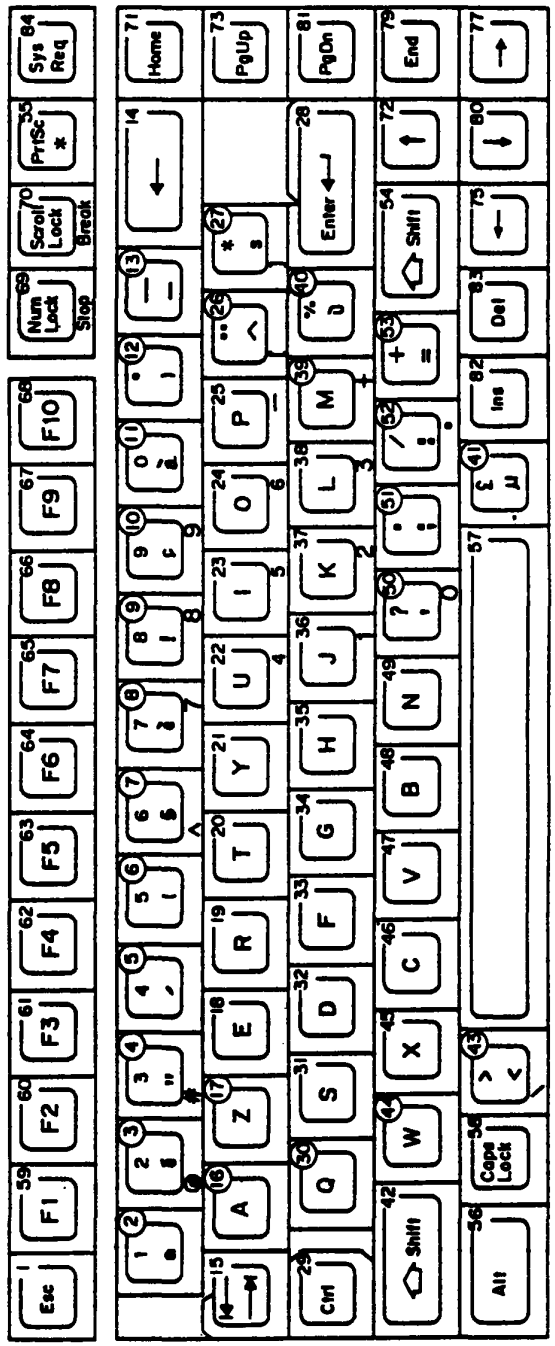


Figure 6-6 French Version

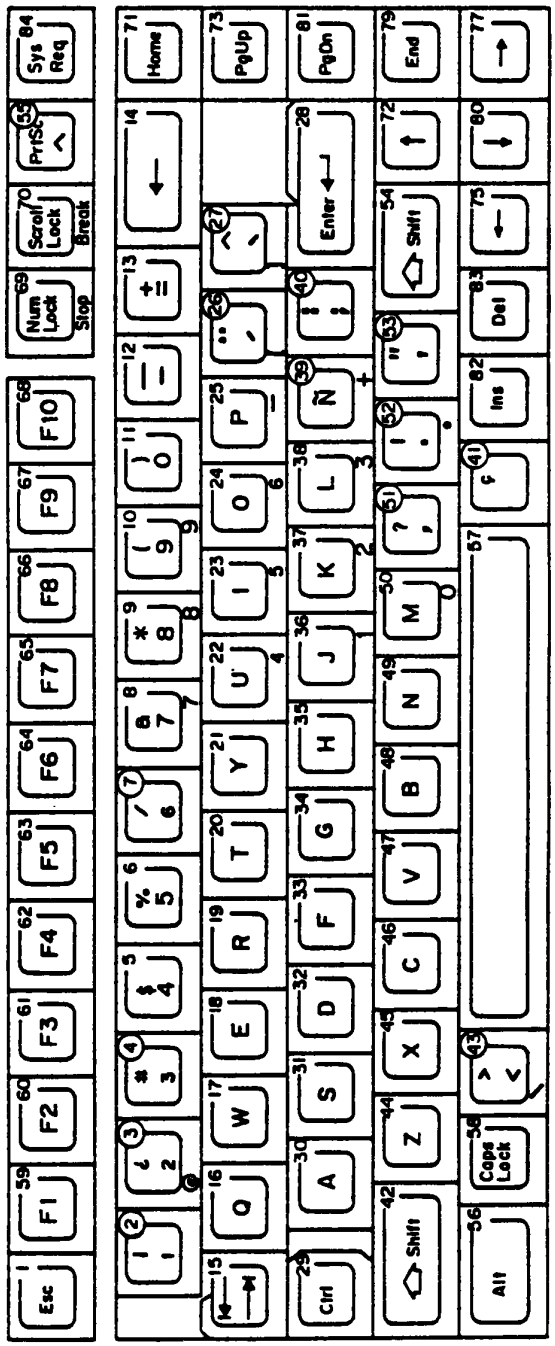


Figure 6-7 Spanish Version

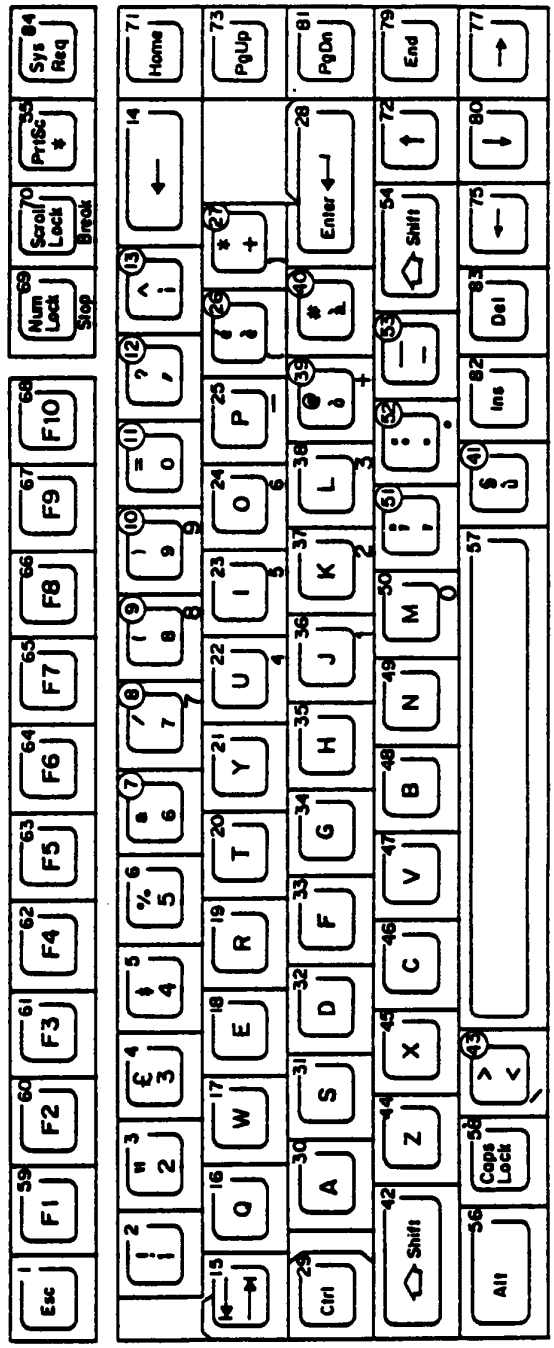


Figure 6-8 Italian Version

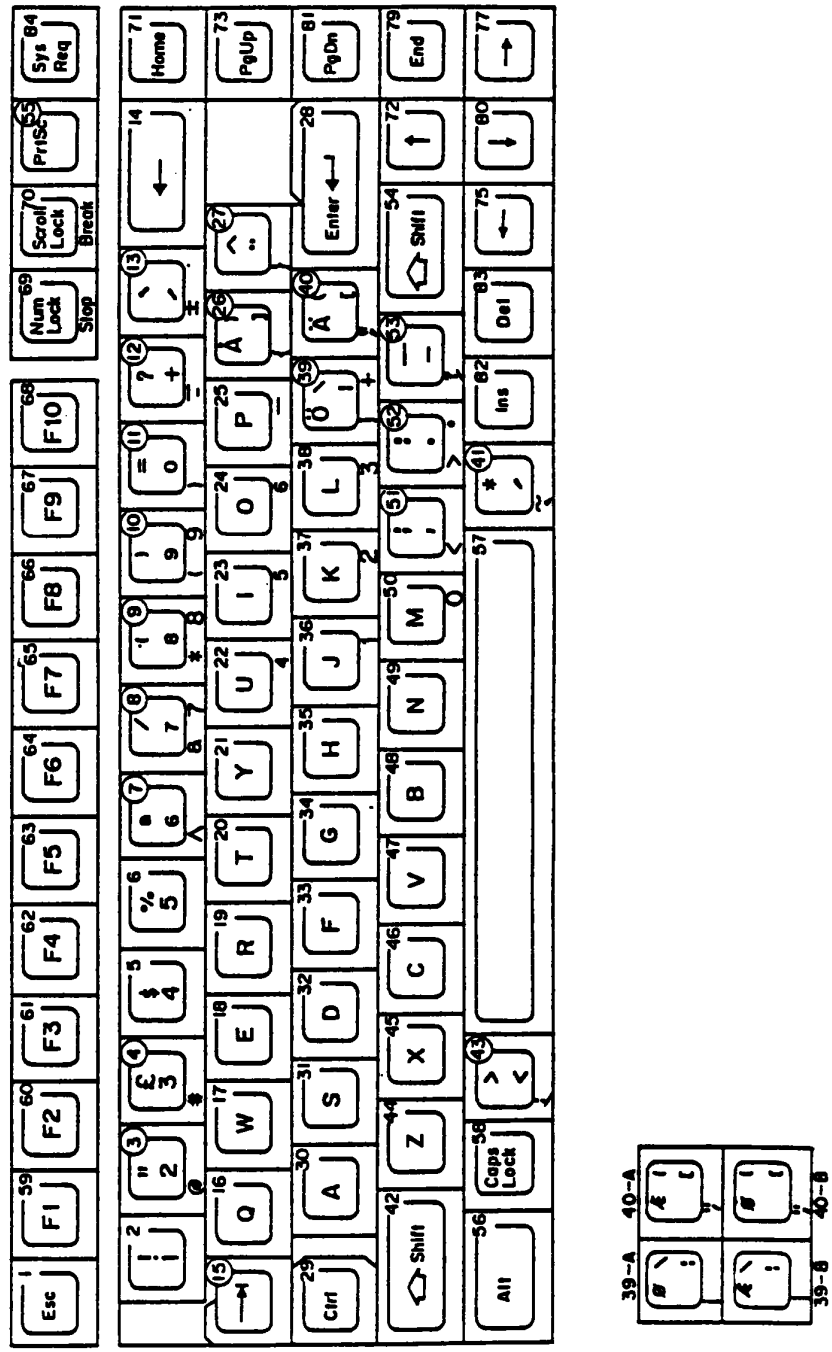


Figure 6-9 Scandinavian Version

HEXA DECIMAL VALUE	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BLANK (NULL)	►	BLANK (SPACE)	0	@	P	‘	p	Ç	É	á	⁞⁞	┌┐	╥	α	≡
1	☺	◄	!	1	A	Q	a	q	ü	æ	í	⁞⁞	┌┐	╥	β	±
2	●	↕	"	2	B	R	b	r	é	Æ	ó	⁞⁞	┌┐	╥	Γ	≥
3	♥	‼	#	3	C	S	c	s	â	ô	ú	┌┐	┌┐	╥	π	≤
4	♦	¶	$	4	D	T	d	t	ä	ö	ñ	┌┐	┌┐	╥	Σ	⌠
5	♣	§	%	5	E	U	e	u	à	ò	Ñ	╞╡	┌┐	╥	σ	⌡
6	♠	▬	&	6	F	V	f	v	å	û	ª	╞╡	┌┐	╥	μ	÷
7	•	↨	’	7	G	W	g	w	ç	ù	º	┌┐	┌┐	╥	τ	≈
8	◘	↑	(	8	H	X	h	x	ê	ÿ	¿	┌┐	┌┐	╥	Φ	°
9	○	↓	)	9	I	Y	i	y	ë	Ö	⌐	┌┐	┌┐	╥	Θ	•
A	◙	→	*	:	J	Z	j	z	è	Ü	¬	┌┐	┌┐	╥	Ω	•
B	♂	←	+	;	K	[	k	{	ï	¢	½	┌┐	┌┐	■	δ	√
C	♀	∟	,	<	L	\	l	¦	î	£	¼	┌┐	┌┐	■	∞	n
D	♪	↔	—	=	M	]	m	}	ì	¾	¡	┌┐	┌┐	■	φ	2
E	♫	▲	.	>	N	^	n	~	Ä	Pt	Ø	┌┐	┌┐	■	∈	■
F	☼	▼	/	?	O	_	o	⌂	Å	ƒ	»	┌┐	┌┐	■	∩	BLANK FF

Table 6-1 Code Table

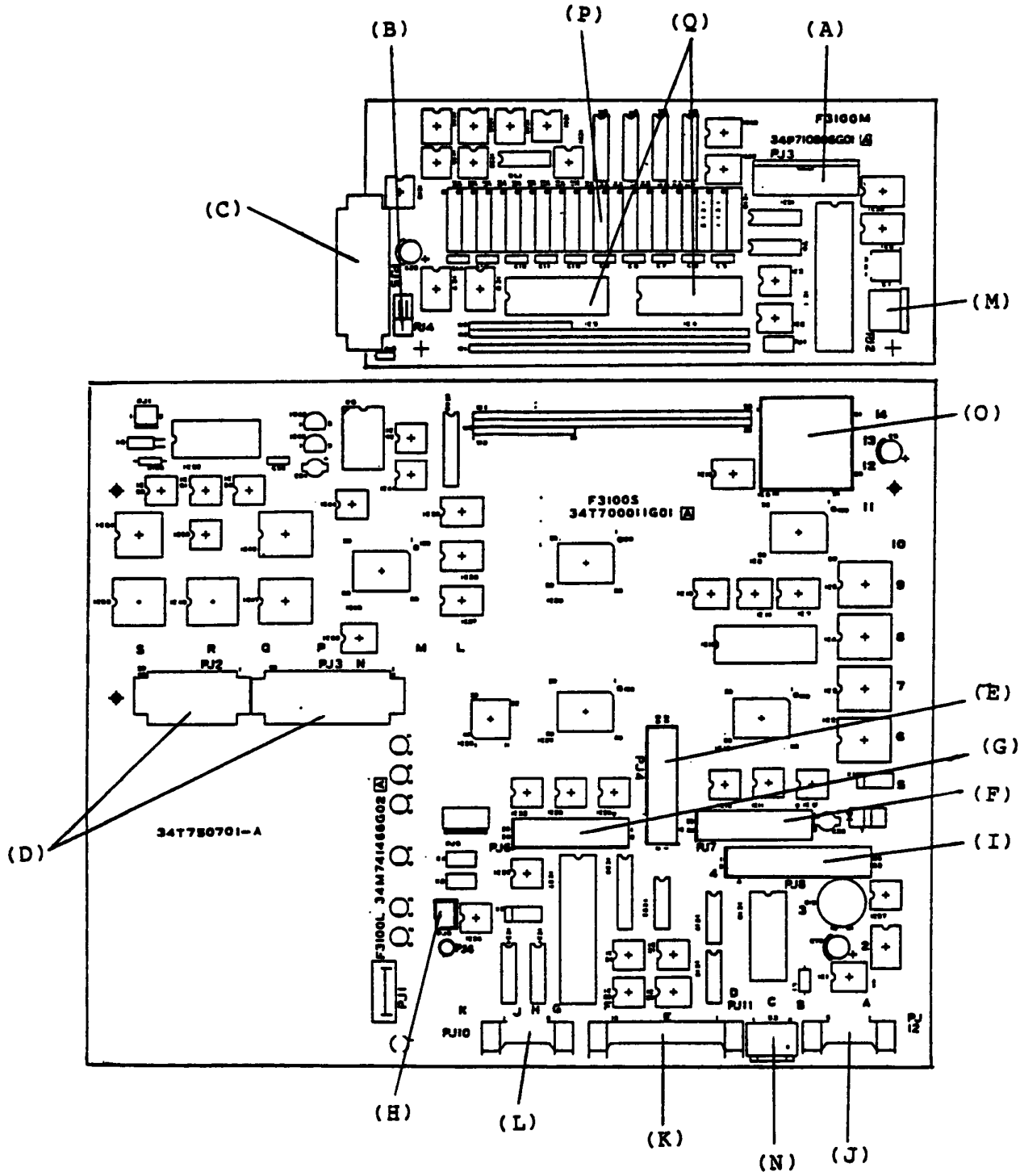


Figure 6-10 System PCB

SYSTEM PCB (Continued)

(A) Keyboard Connector

(B) Speaker Connector

(C) Expansion Memory Connector (Option)

(D) Modem Card or I/O Expansion Card Connector (Option)

(E) Plasma Display Connector

(F) FDD 2 Connector

(G) FDD 1 Connector

(H) Power Supply Connector

(I) HDC Connector (Option)

(J) Color CRT Display Connector

(K) External FDD and Printer Connector

(L) RS232C Connector

(M) Printer / External FDD Select Switch

(N) DIP Switch

(O) CPU

(P) Memory Chips (640 KB)

(Q) ROM (BOIS)

FLOPPY DISK DRIVE (FDD) (Top View of mechanical assembly)

(A) Head Assembly

(B) Stepping Motor

(C) Track 00 sensor

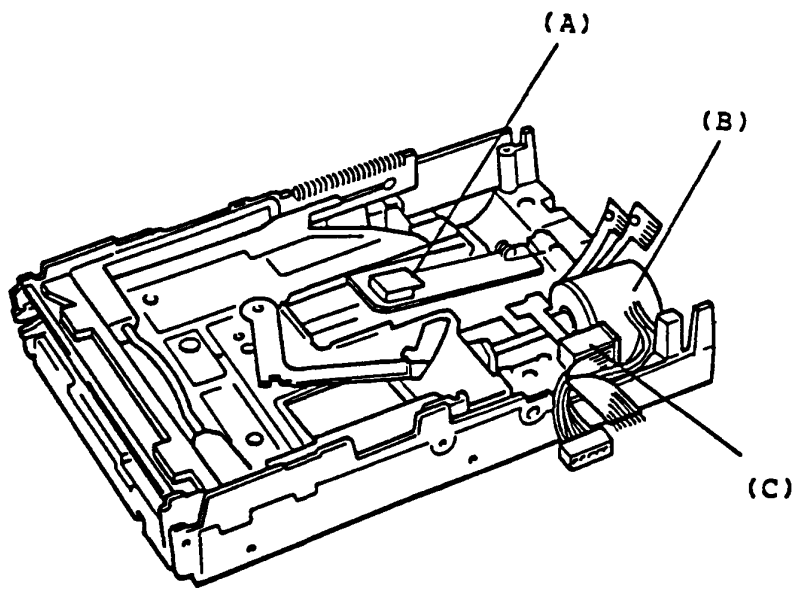


Figure 6-11 Top View of Mechanical Assembly

FLOPPY DISK DRIVE (FDD) (Bottom View)

(A) Drive Motor

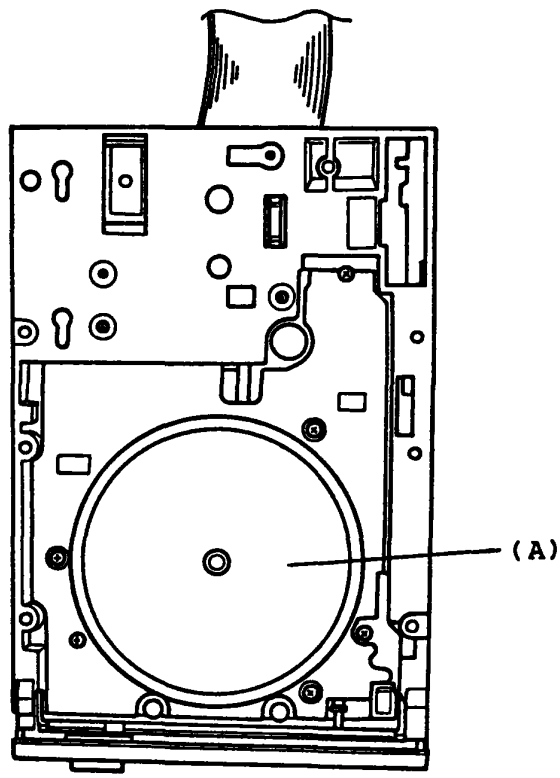


Figure 6-12 Bottom View of FDD

(A) PJ 2 Interface and power connector

(B) PJ 3 Sensor connector

(C) PJ 4 Sensor connector

(D) PJ 5 Step motor connector

(E) PJ 6 Read/Write head 0 connector

(F) PJ 7 Read/Write head 1 connector

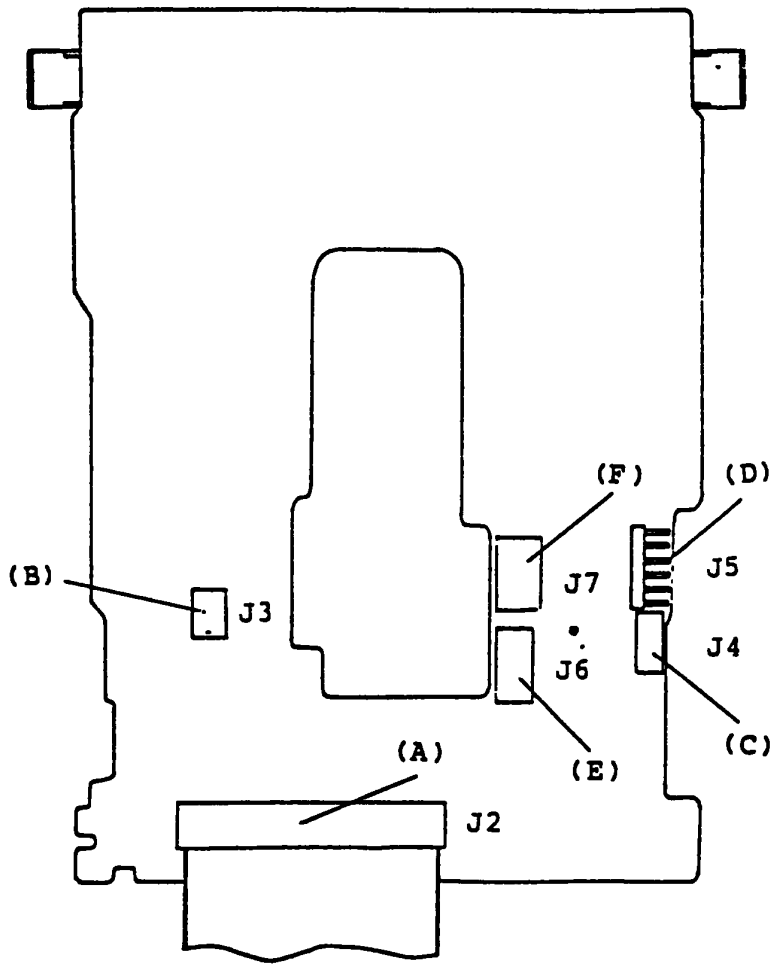


Figure 6-13 FDD PCB

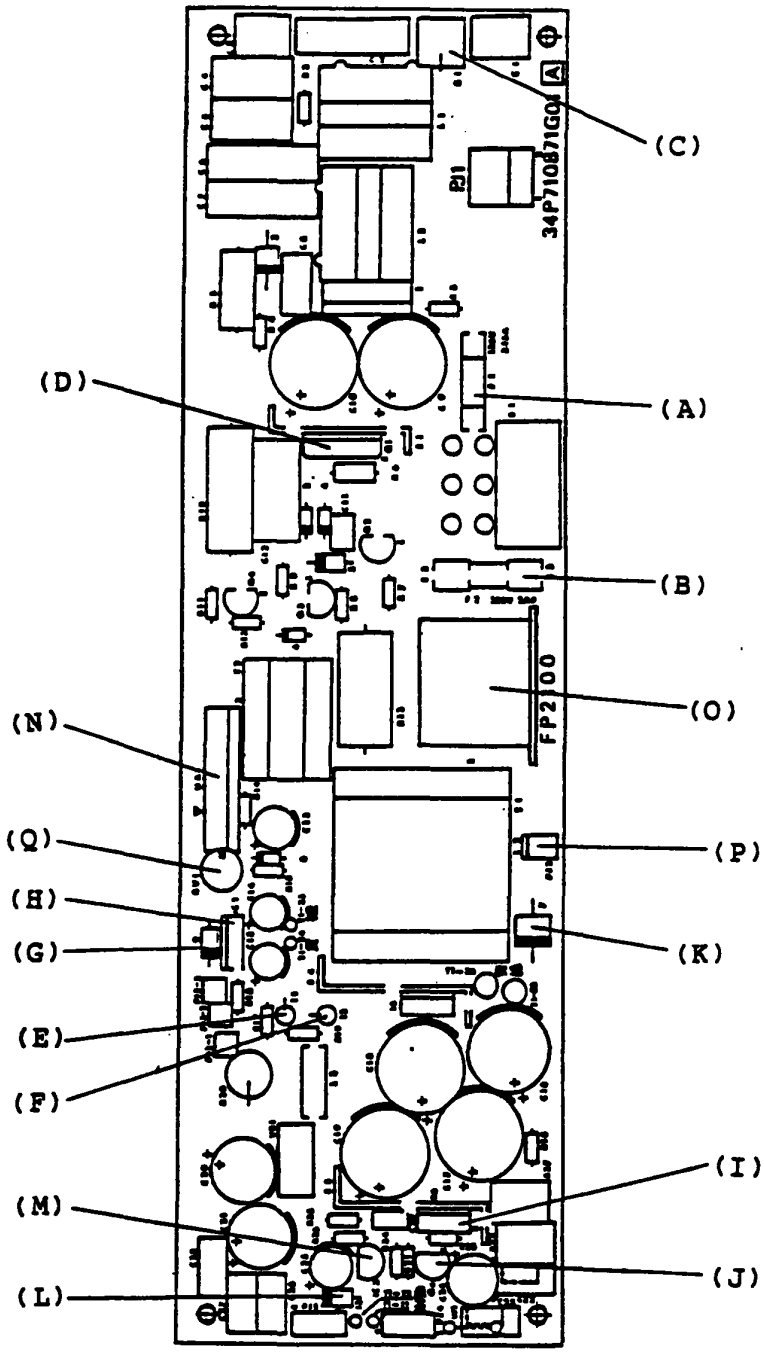


Figure 6-14 Power Supply PCB

POWER SUPPLY PCB (Continued)

(A) Fuse F1 (3.15A)

(B) Fuse F2 (2A)

(C) Resister R1 (2.2 ohm 5W)

(D) Transistor Q1 (2SC3261)

(E) Diode CR11 (1S1835)

(F) Diode CR12 (1S1835)

(G) Diode CR9 (1S1835)

(H) IC IC1 (TA78005AP)

(I) Transistor Q5 (2SC3346)

(J) Transistor Q6 (2SC336)

(K) Diode CR7 (3DH61)

(L) Diode CR13 (1S1835)

(M) IC IC2 (TL431C)

(N) Controller UA1

(O) Cooling Fan

(P) Cooling Fan Connector

(Q) VR1

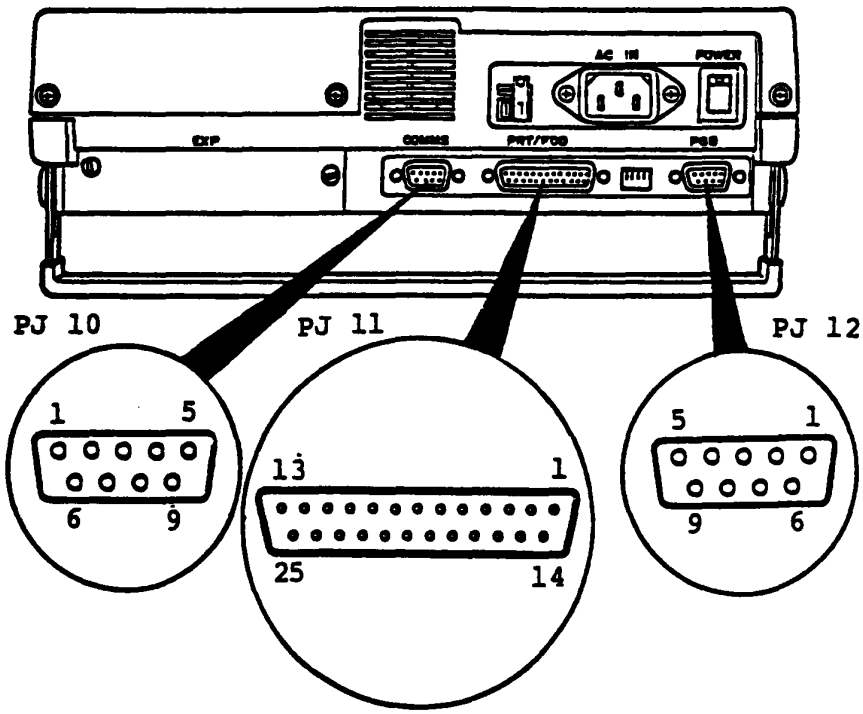


Figure 6-15 System Unit Rear Panel

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
PJ 12		**PJ 11**			
1	GND	1	STROB0	21	GND
2	GND	2	PD01	22	GND
3	CRV1	3	PD11	23	GND
4	CGV1	4	PD21	24	GND
5	CBV1	5	PD31	25	GND
6	CIV1	6	PD41		
7	NC	7	PD51		
8	CHSY1	8	PD61		
9	CVSY1	9	PD71		
		10	ACK0		
		11	BUSY1	**PJ 10**	
		12	PE1	1	DCD1
		13	SELEC1	2	DRD1
		14	AUTFD0	3	DTD1
		15	ERROR0	4	DTR1
		16	PINT0	5	GND
		17	SLIN0	6	DSR1
		18	GND	7	RTS1
		19	GND	8	CTS1
		20	GND	9	DRI1

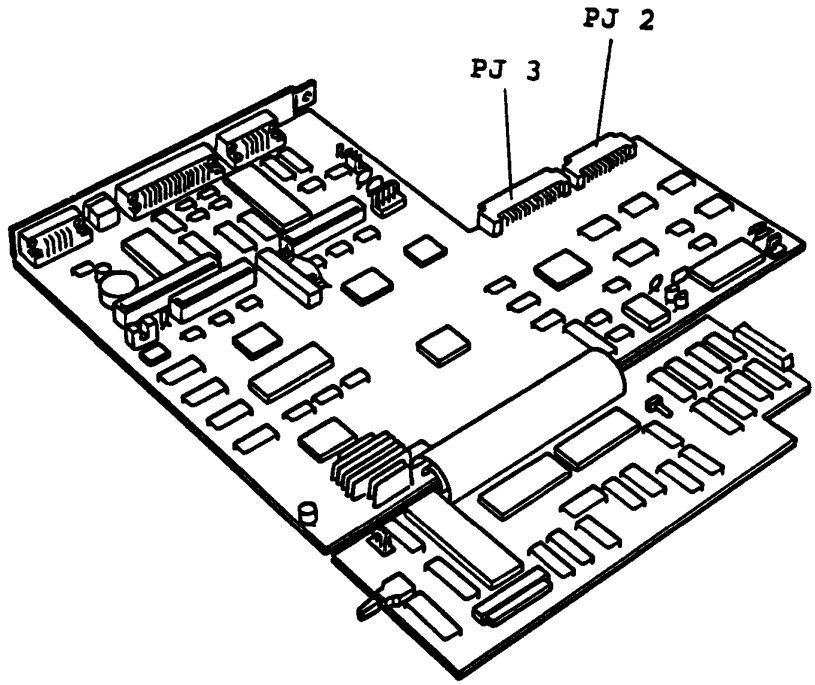


Figure 6-16 System PCB

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
PJ 2					
1	IRQ101	16	A231	31	IO160
2	IRQ141	17	DACK70	32	DRQ71
3	SD81	18	A211	33	DRQ61
4	SD91	19	A191	34	DRQ51
5	IRQ111	20	A201	35	DACK50
6	SD101	21	DACK60	36	MEMR0
7	SD111	22	GND	37	DRQ71
8	SD121	23	REFRSH0	38	MEMW0
9	IRQ121	24	A181	39	DACK0
10	GND	25	MASTER0	40	GND
11	SD131	26	A171		
12	SD141	27	SBHE0		
13	IRQ151	28	IOCHK0		
14	SD151	29	MEM160		
15	A221	30	GND		

To be continued.

CONNECTOR (System PCB) (Continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
PJ 3					
1	GND	21	A101	41	MWR0
2	VCC	22	A111	42	MRD0
3	M9VDC	23	A121	43	GND
4	P12VDC	24	A131	44	IOWR20
5	MDMSL0	25	A141	45	IORD20
6	COMCLK1	26	A151	46	TC1
7	MIRQ0	27	GND	47	BALE1
8	SPKTON0	28	A161	48	RSET1
9	GND	29	A171	49	DACK10
10	A001	30	A181	50	IRQ91
11	A011	31	A191	51	GND
12	A021	32	SYD01	52	VCC
13	A031	33	SYD11	53	SYSCLK1
14	A041	34	SYD21	54	IRQ51
15	A051	35	SYD31	55	DRQ31
16	A061	36	GND	56	DACK30
17	A071	37	SYD41	57	DMACK1
18	GND	38	SYD51	58	DRQ11
19	A081	39	SYD61	59	IORDY1
20	A091	40	SYD71	60	GND

7.1 System Unit

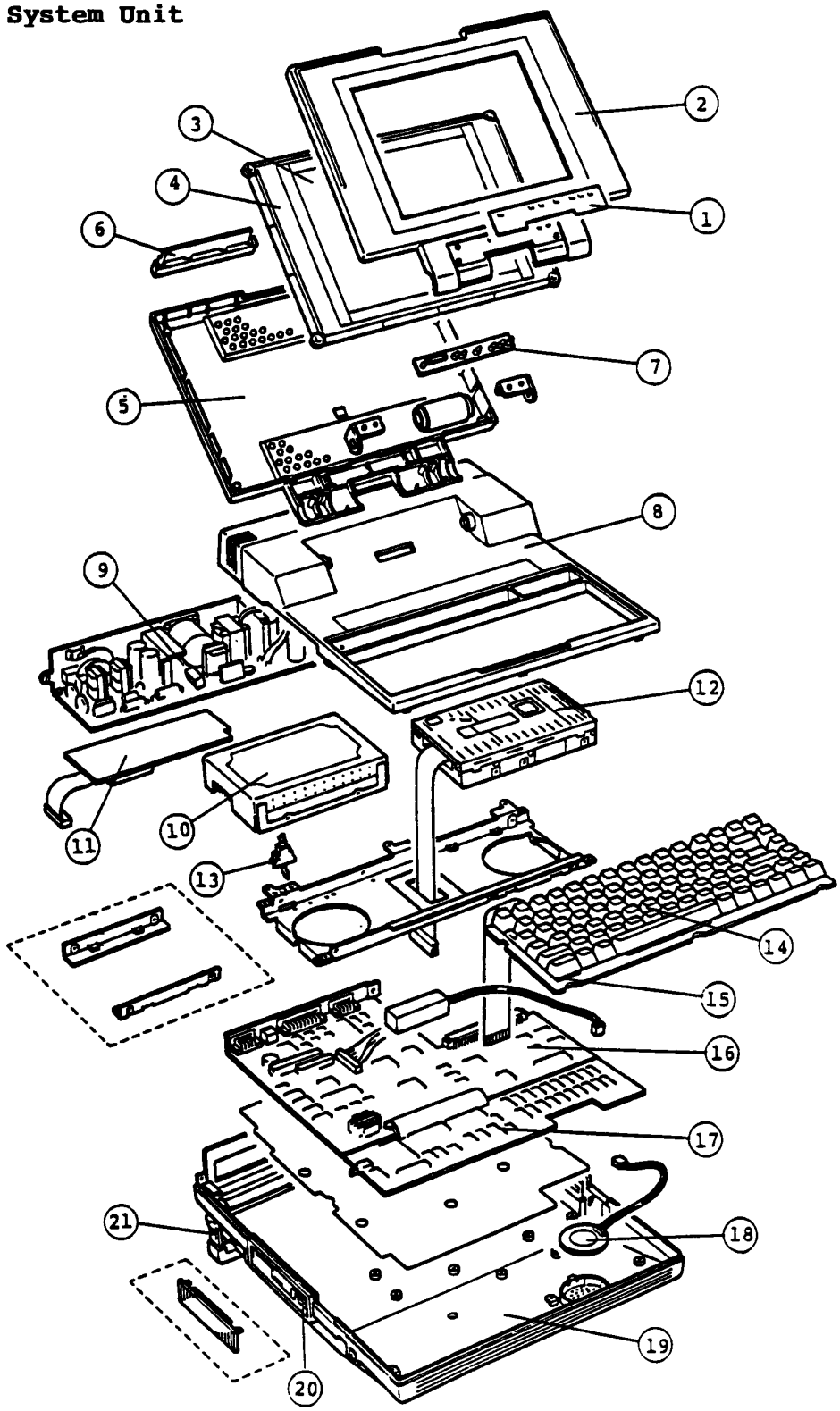


Figure 7-1 T3100 System

7.1 System Unit (Continued)

INDEX No.	PART NUMBER	DESCRIPTION	NOTE
1	47M139927P1	Indicater Seal	
2	47U100190P1	PDP Mask	
3	47K158483P1	PDP Filter	
4	VF0017P01	PDP (Plasma Display Panel)	
5	47M139726P1	PDP Shield Board	
6	47M139688P1 47M139689P1 47K158469P1	Latch A Latch B Pressure spring	
7	34M741466G01	Indicator (LED)	
8	47U100187P1	Upper Caver	
9	APS0513AZZ01	Power Supply Unit	
10	ZA0656P11	HDD (Hard Disk Drive)	
11	ZA0656P21	HDC (Hard Disk Controller)	
12	ZA0652P01	FDD (Floppy Disk Drive)	
13	47K158484G1	Sensor Guide	
14	UE0182P01 UE0182P02	Keyboard Keyboard	UK version USA version
15	SB0044P01	Key switch	
16	34T700096G01	System PCB 1	
17	34P710806G01	System PCB 2	
18	39K156042G1	Speaker	
19	47U100188P1	Lower Cover	
20	47M139694P1	FDD Eject Button	
21	47P127670G1	Handle	

7.2 5.25" External FDD

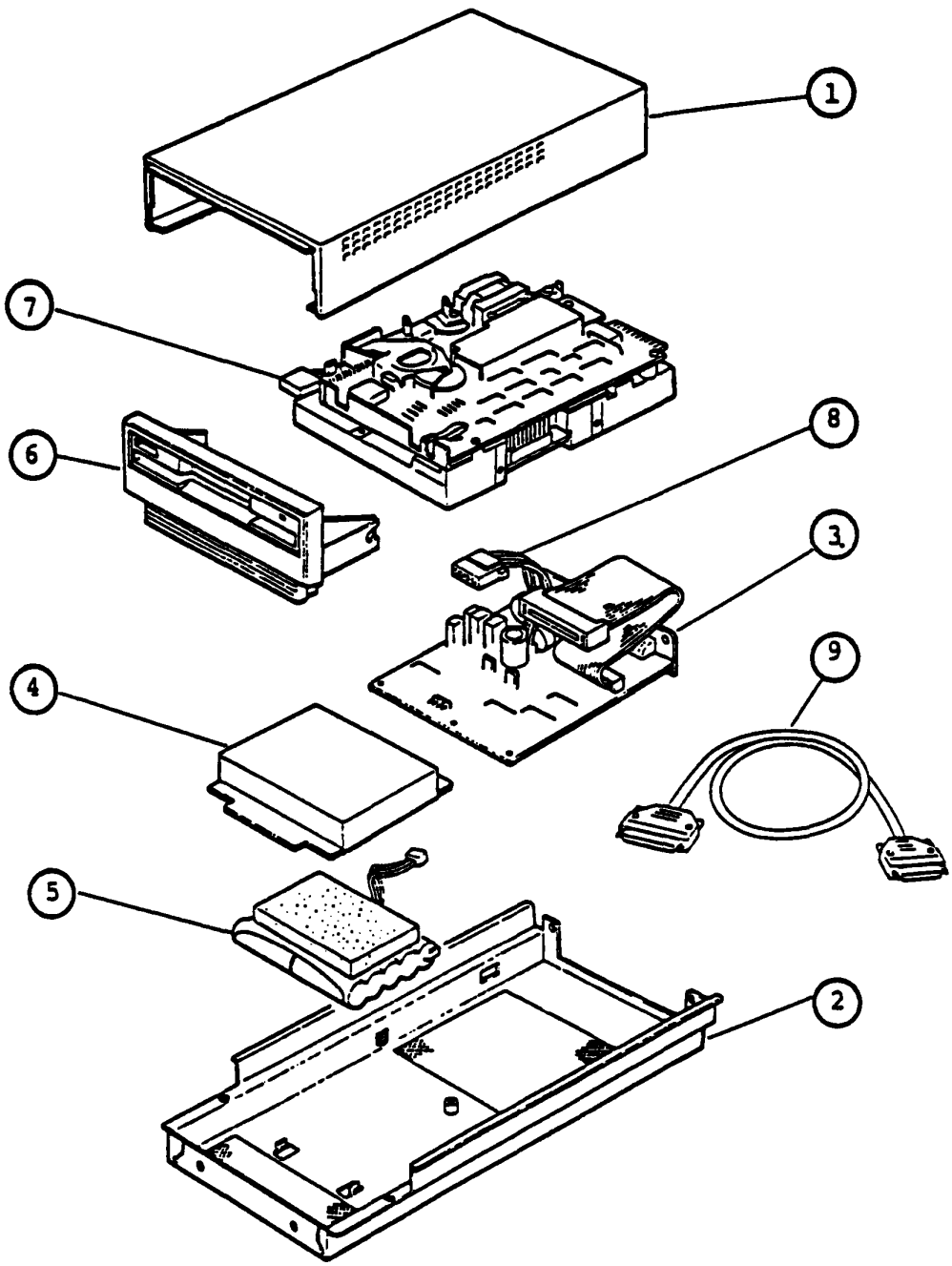


Figure 7-2 5.25" External FDD

7.2 5.25" External FDD (Contiuned)

INDEX No.	PART NUMBER	DESCRIPTION	NOTE
1	47P127086P1	Upper Cover	
2	47P127085P1	Lower Cover	
3	34P710241G01	PCB	
4	47M137924P1	Battery Cover	
5	XZ0067P01	Battery	
6	47P127089P1	Front Panel	
7	ZA0162P01	5.25 inch FDD	
8	UL0034P23	FDD PS Cable	
9	UL0046P13DD004	Cable	

8.1 INTRODUCTION

8.1.1 General

The purpose of this T3100 Test and Diagnostics is to check the functions of all hardware modules of the T3100 Personal Computer.

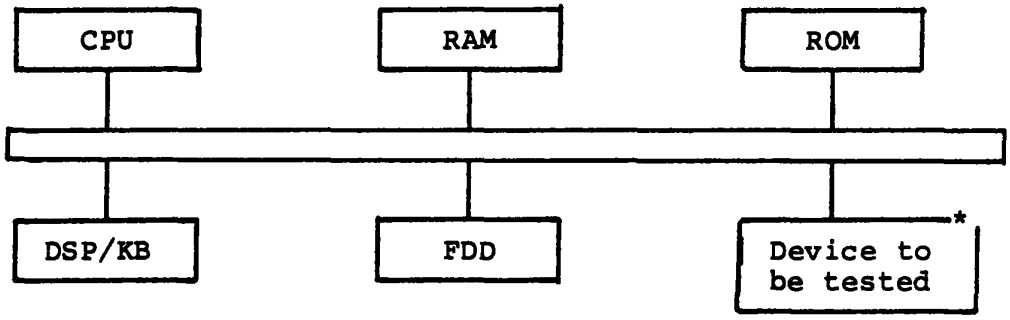
This T3100 Test and Diagnostics is structured under the MS-DOS, and consists of 18 programs covering all of the hardware modules supported in T3100 Personal Computer system as described in STRUCTURE section.

The **CE Diagnostic Test Program** is provided as a file in the MS-DOS System Disk. You have to run the MS-DOS before you load the CE Diagnostic Test Program.

The service engineer utilize these programs to isolate the trouble by selecting the appropriate program by the operation procedure described in OPERATION section.

8.1.2 Components Required

The following devices are required to execute the test program system.



Where:

CPU : Central Processer Unit

RAM : Random Access Memory ; 256KB

ROM : Read Only Memory; 32KB

DSP : Plasma Display Unit

KB : Keyboard

FDD : Floppy Disk Drive ;720KB

*

Devices to be tested

RAM : Random Access Memory

ROM : Read Only Memory

KB : Keyboard

DSP : Plasma Display Unit

FDD : Floppy Disk Drive (720KB/360KB)

PRT : Printer Device or Wraparound connector

RSC : Communications controller + Wraparound connector card, Modem

HDD : Hard Disk Drive

RTM : Real Timer

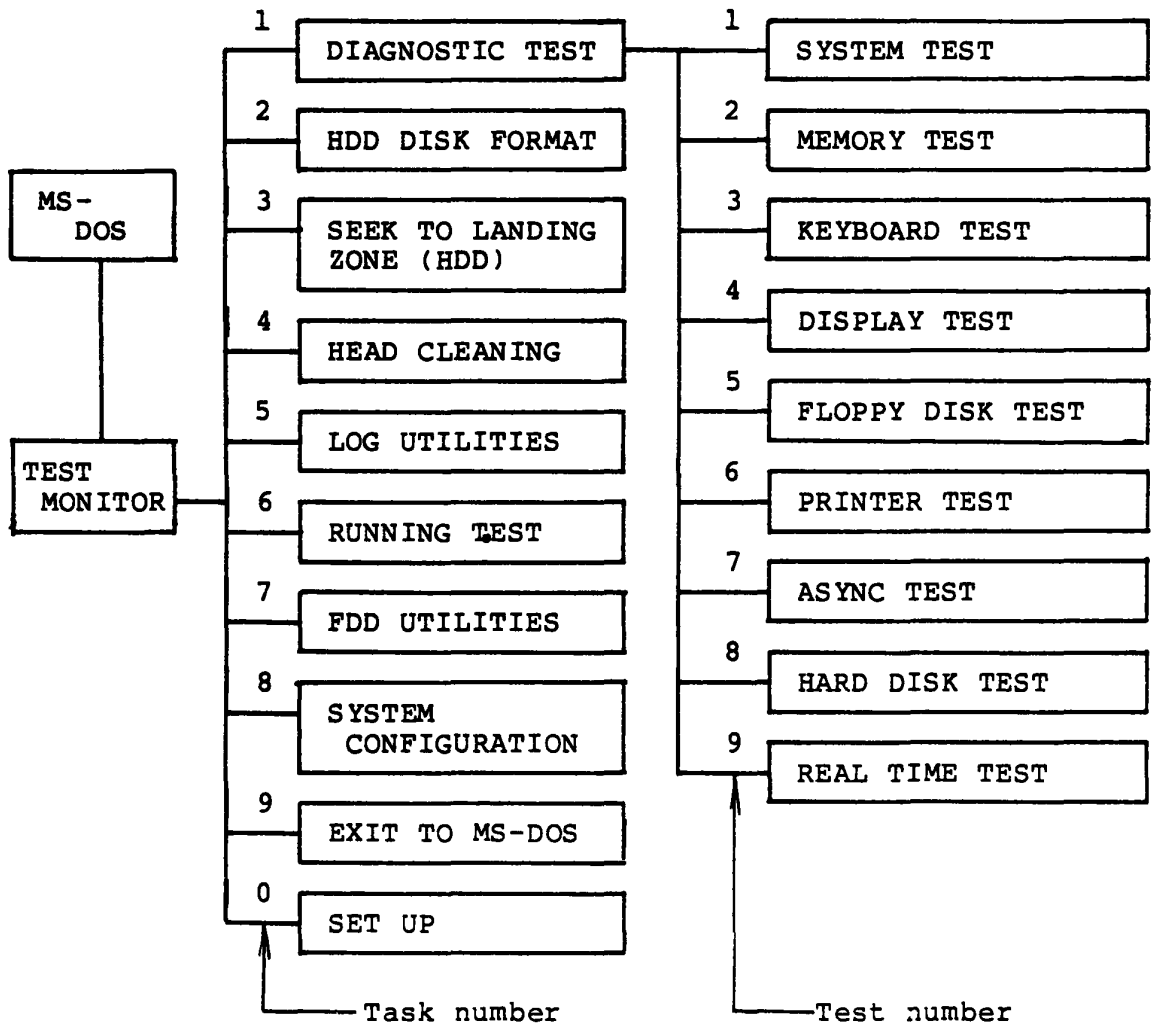
8.1.3 Structure

The T3100 test program system is composed of 17 program modules executed under the Test Monitor.

The 17 program modules can be divided into two groups, the Service Program modules (HDD format, Landing zone seek, Head cleaning, Log utility, Running test, FDD utilities, and System configuration) and the Test Program modules (all other modules). Those are shown in the figure on next page.

Each of the Test Program modules contains some number of subtest programs which are shown in the **ANNEX A:** Test Program List.

TEST PROGRAM STRUCTURE



8.2 OPERATION

This section describes how to operate the T3100 Test and Diagnostics such as **CE Diagnostic Test Program** . These Diagnostic Test Programs are provided in the MS-DOS System Disk. You have to run the MS-DOS before you load the CE Diagnostic Test Program.

5.2.1 CE DIAGNOSTIC

(1) Test program loading

Insert the MS-DOS disk to the internal disk drive, then turn on the power of the T3100. The MS-DOS is loaded after **Power On Self-test** execution. After the loading, following messages appear on the screen.
And press the "ENTER" Key twice, and then file name of **CE Diagnostic** as **testce** to load the diagnostic program.
If **Current date** and **Current time** is mistake, input the **Enter new date** and **Enter new time** then file name of **Diagnostic** as **testce** to load the diagnostic program.

```
Toshiba Personal Computer  (RXXXXUS)      Preliminary version

Copyright 1984,86 Toshiba Corporation

MS-DOS   Ver 2.11
Copyright 1983,84 Microsoft Corp.

Command  Ver 2.11V
Current date is  Wed  1-01-1986
Enter new date :
Current time is   0:36:46.00
Enter new time :

A>testce
```

The underlined portion on the above screen is for the input message.
After the above operation, the test program loading is complete.

(2)Module selection

The following screen (Diagnostic Menu) is displayed after the test program loading.

```
TOSHIBA personal computer T3100 DIAGNOSTICS
version X.XX (c) copyright TOSHIBA Corp 1986

DIAGNOSTICS MENU :

  1 - DIAGNOSTIC TEST
  2 - HARD DISK FORMAT
  3 - SEEK TO LANDING ZONE (HDD)
  4 - HEAD CLEANING
  5 - LOG UTILITIES
  6 - RUNNING  TEST
  7 - FDD UTILITIES
  8 - SYSTEM CONFIGURATION
  9 - EXIT TO MS-DOS
  0 - SETUP




PRESS [0]-[9] KEY
```

Input a module number and then press the "ENTER" key to select the module on DIAGNOSTIC MENU. When you input;

1 : Displays the Diagnostic Test Menu. See page 8-10. (includes pressing "ENTER" key only)
2 : Executes the Hard Disk Format. See page 8-34. (Use the only F/H type.)
3 : Seeks the head of HDD to Landing Zone. See page 8-36. (Use the only F/H type.)
4 : Cleans the head of FDD. See page 8-37.

5 : Displays the error logs. See page 8-38.

6 : Executes the running test. See page 8-40.

7 : Executes the format, copy and dump of FDD. See page 8-42.
8 : Displays the system configuration. See page 8-43.

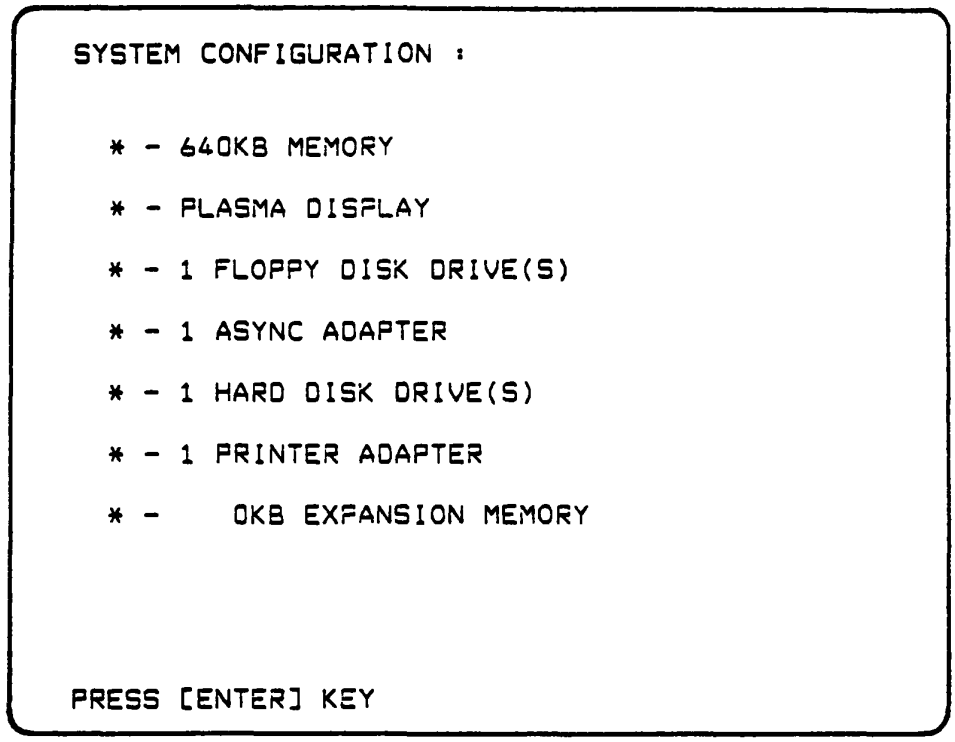
9 : Returns to MS-DOS

0 : Displays the set up of System (Writing of CMOS) See page 8-44.

If you input the except above module number, the screen return to the Diagnostic Menu. (above screen)

(3) Displaying of system configuration

The following system configuration will be displayed on the Plasma Display Unit/CRT Display Unit after pressing "8" and "ENTER" keys at task selection.



Above message is an example of F/H type System .

Compare your System Unit and System Configuration of above message, and then if it is good, press the "ENTER" key.
If it is no good, turn OFF the power switch of the System Unit, and then check the configuration DIP switch. (Refer to page 1-10)
Repeat the operation from step (1) after correcting them.

(4) Test selection

The following screen appears after pressing "1" and "ENTER" keys at task selection.

```
TOSHIBA personal computer T3100 DIAGNOSTICS
version X.XX (c) copyright TOSHIBA Corp 1986

DIAGNOSTIC TEST MENU :

   1 - SYSTEM TEST
   2 - MEMORY TEST
   3 - KEYBOARD TEST
   4 - DISPLAY TEST
   5 - FLOPPY DISK TEST
   6 - PRINTER TEST
   7 - ASYNC TEST
   8 - HARD DISK TEST
   9 - REAL TIMER TEST
  88 - FDD & HDD ERROR RETRY COUNT SET
  99 - EXIT TO DIAGNOSTICS MENU




 PRESS [1]-[9] KEY
```

Input the test number, and then press the "ENTER" key to execute the DIAGNOSTIC TEST MENU.

If you input the above test number (1 - 9), System Unit execute the each test.

If you input the above test number (88), You can set the error retry count of the FDD and HDD.

If you input the above test number (99), the Screen return to the DIAGNOSTIC MENU. (Refer to page 8-8.)

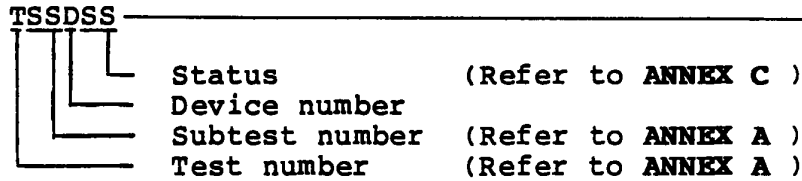
If you input except above test number, the screen return to the Diagnostic Test Menu. (above screen)

(5) Subtest and test mode selection

The subtest menu screen (the following sample is for FDD) will be displayed after selecting any test(1-7) at test selection, so input two digit subtest number.
(Refer to **ANNEX A:** Test Program List)

```
FLOPPY DISK                                  501000


SUB-TEST   : 01
PASS COUNT: 00000       ERROR COUNT: 00000
WRITE DATA: 00          READ  DATA : 00
ADDRESS    : 000000     STATUS     : 000

SUB-TEST MENU :

01 - Sequential read
02 - Sequential read/write
03 - Random address/data
04 - Write specified address
05 - Read specified address
99 - Exit to DIAGNOSTIC TEST MENU



SELECT SUB-TEST NUMBER  ? 01
TEST  LOOP (1:YES/2:NO) ? 2
ERROR STOP (1:YES/2:NO) ? 1
```

where,



Note 1 : Subtest number

Select a subtest by typing two-digit number. The input number "99" make the control return to step (4): Diagnostic Test Menu.

Note 2 : Test mode selection

The test program execution mode can be specified as follows after the test ends or when an error occurs.

TEST LOOP (1:YES/2:NO) ?

1 : At each time a test cycle ends, it increments the pass counter by one and repeats the test cycle. (If you press "RETURN" key, it is assumed to be TEST LOOP 1:YES.)

2 : At the end of test cycle, it terminates the test execution and exits to the subtest selection menu.

ERROR STOP (1:YES/2:NO) ?

1 : When an error occurs, it displays the error status at column 7 (Refer to **ANNEX C**) and stops the execution of test program. The operation guide displays on the right side of the screen as follows.

```
((HALT OPERATION))
  1 : Test End
  2 : Continue
  3 : Retry
```

Input "1" key : It terminates the test program execution and exits to the subtest selection menu.
Input "2" key : It continues the test.
Input "3" key : It retrys the test.

2 : When an error occurs, it displays the error status, then it increments the error counter by one and goes to the next test step.

Note : The Running test will neglect the "TEST LOOP (N)", and "ERROR STOP (Y)".
If you stop the Running test, press "Ctrl + "Break" keys. The screen return to the DIAGNOSTIC MENU.

(6) Termination

When it is needed to terminate the test program execution, press the **"Ctrl" + "Break"** keys. The screen return to the DIAGNOSTIC MENU.

8.3 SYSTEM TEST

Summary of the System Test

This program performs the checksum test of the ROM on the Systems PCB.

Subtest and test mode selection

After pressing "1" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
SYSTEM TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - ROM checksum
99 - Exit to DIAGNOSTIC TEST MENU









SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER". Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS** , and **STATUS** are displayed and updated during execution as shown above.

8.4 MEMORY TEST

Summary of the Memory Test

This test performs the memory read/write test with constant data (Five patterns) and address pattern data and also memory refresh test for RAM.

Subtest and test mode selection

After pressing "2" and "ENTER" keys at test selection on the DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
MEMORY TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - RAM constant data
02 - RAM address pattern data
03 - RAM refresh
99 - Exit to DIAGNOSTIC TEST MENU









SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Subtest 01 Constant data read/write test

Writes constant data to Memory, and then reads and compares it with the original data.
The constant data are "FFFFH", "AAAAH", "5555H", "0101H" and "0000H".

Subtest 02 Address pattern data read/write test

Makes the segment address and offset address by XORing, and then writes the address pattern data it and reads and compares them with a original data.

Subtest 03 Memory refresh test

Writes constant data in 256 byte length to Memory, and then reads and compares it with the original data. The constant data are "AAAAH" and "5555H". A certain interval time will be taken between the write and the read operations.

Subtest 04 Protect mode test

Write the data = AA55H, 55AAH, FFFFH, 0846H for 256 KB - MAX 640 KB, 1 MB - MAX MB to protect mode, then reads and compares it with original data.

8.5 KEYBOARD TEST

Summary of the Keyboard Test

This test performs the function test of keyboard by pressing all the keys according to the keyboard pattern on the screen.

Subtest and test mode selection

After pressing "3" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
KEYBOARD TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX       ERROR COUNT: XXXXX
WRITE DATA: XX          READ  DATA  : XX
ADDRESS    : XXXXXX     STATUS      : XXX

SUB-TEST MENU :

01 - Pressed key display
99 - Exit to DIAGNOSTIC TEST MENU









SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Keyboard layout is drawn on the Display, and when a certain key is pressed, the character "*" will be displayed at the corresponding location of the screen.

If the same key is pressed again, it becomes to be the original state so that it is able to confirm the self-repeat function.

If you stop the Keyboard test, press "Ctrl" + "Break" keys.

8.6 DISPLAY TEST

Summary of the Display Test

This test performs the test of VIDEO RAM read/write, attribute character, character mode display, graphic mode display, and screen page for Plasma Display and its controller function.

Subtest and test mode selection

After pressing "4" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
DISPLAY TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - VRAM read/write
02 - Character attributes
03 - Character set
04 - 80 * 25 Character display
05 - Graphics display (color set 0/1)
06 - 640 * 200 Graphics display
07 - 640 * 400 Graphics display
08 - Display page
09 - "H" pattern display
99 - Exit to DIAGNOSTIC TEST MENU


SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two dights subtest number in **SUBTEST MENU** as show above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Subtest 01 Read/write test of video RAM

In the display-off mode, it writes the constant data such as "FFH", "AAH", "55H", "00H" to the video RAM, then it reads and compares them with the original data.

Subtest 02 Character attribute display test

Normal Display
Intensified Display
Reverse Display
Blinking Display

* Note : If it is a color CRT display unit, you checks background color, foreground color, border color about each of seven colors of blue, green cyan, red magenta, yellow and white.

Subtest 03 Display of character set

Displays in 40 x 25 Test mode character codes "00H" though "FFH"

Subtest 04 Display of 80 x 25 characters

Displays Shift-Characters.

Subtest 05 In the case of Color Display:

Displays three painted blocks with color set 0 in 320 x 200 graphic mode.

Blocks color green, red, and yellow

Displays three painted blocks with color set 0 in 320 x 200 graphic mode.

Blocks color Cyan, magenta, and white.

In the case of Plasma Display:

Screen is lighten in order of RED MAGENTA, GREEN CYAN, YELLOW WHITE.

Subtest 06 Display in 640 x 200 graphic mode

It displays in the screen Black & white.

Subtest 07 Display in 640 x 400 graahic mode

Only Plasma Display.

To be continued.

Subtest description (Continued)

Subtest 08 Screen Page test

Displays the contents of VIDEO RAM to the CRT in 40 x 25 test mode. VIDEO RAM contains a capacity of 8 screen pages and each screen page is displayed as all "0", all "1" .... and all "7" respectively.

Subtest 09 "H" Pattern display test

Display of "H" character on the whole screen.

8.7 FLOPPY DISK TEST

Summary of the FLOPPY DISK Test

This test performs the read/write test with sequencial address, random address, and specified address for FDD and its controller functions.

Subtest and test mode selection

After pressing "5" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following message appear on the screen.

Test drive number select (1: FDD1, 2: FDD2, 0: FDD1&2) ?

1: Executes only FDD1 test.

2: Executes only FDD2 test.

0: Executes FDD1 and FDD2 test.

After press the above the number, following the message on the screen.

Media in drive#n mode (0:720K, 1:360-360K, 2:360K-1.2M/720K, 3:1.2M)?

0: Check the media of FDD (2DD).
(2DD media - 2DD drive)
(2DD media - 2HD drive)

1: Check the media of FDD (2D).
(2D media - 2D drive)

2: Check the media of FDD (2D).
(2D media - 2DD drive)
(2D media - 2HD drive)

3: Check the media of FDD (2HD).
(2HD media - 2HD drive)

To be continued.

After you choose the media in drive#n mode of FDD, the following screen appears for subtest and test mode selection.

```
FLOPPY DISK                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Sequential read
02 - Sequential read/write
03 - Random address/data
04 - Write specified address
05 - Read specified address
99 - Exit to DIAGNOSTIC TEST MENU




SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS** ,and **STATUS** are displayed and updated during execution as shown above.

Refer the following subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Subtest 01 Sequential read test

Reads all tracks sequencially and checks CRC.

Subtest 02 Sequential read/write test

Writes data to all tracks sequencially, and then reads the data back and compares them with the original data.
(The data pattern,"B5ADAD H", is repeated.)

Subtest 03 Random address/data read/write

Writes random data into tracks gelected at random, and then reads the data back and compares them with the original data.

Subtest 04 Specified address write test

Writes the data into a track and a head specified and head address done through the Keyboard.

Subtest 05 Specified address read test

Reads the data from the track and head address specified through the Keyboard.

Note: Use one of the following "Format" programs to format a work disk according to the disk type.
In the case of 2D(FORMAT /4), formatted tracks are 0 thru 39.
In the case of 2DD(FORMAT), formatted tracks are 0 thru 79.

8.8 PRINTER TEST

Summary of the Printer Test

This test performs the test of ripple pattern, functions(six print modes), and wraparound for printer and its controller.

Subtest and test mode selection

After pressing "6" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
PRINTER TEST                          XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Ripple pattern
02 - Function
03 - Wrap around
99 - Exit to DIAGNOSTIC TEST MENU




SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS** ,and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Subtest 01 Ripple pattern test

Prints characters (codes "20H" through "7EH") on a line rotating the line pattern by one character to the down lines.

Subtest 02 Function test

Normal Print
Double Width Print
Compressed Print
Emphasized Print
Double Strike Print
All Characters Print

Subtest 03 Wraparound test

Checks the data, control, and status lines with the Printer Wraparound Connector(Part No.).

Note: Subtest 01 and subtest 02 needs the channel selection.

8.9 ASYNC(RS232C) TEST

Summary of the ASYNC(RS232C) Test

This test performs the data transmission(Send/Receive) with the CCM Wraparound Connector(Part No.).

Subtest and test mode selection

After pressing "7" and "ENTER" at test selection, the following screen appears for subtest and test mode selection.

```
ASYNC TEST                                  XXXXXXX.

.

SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Wrap around (channel-1)
02 - Wrap around (channel-2)
03 - Point to point (send)
04 - Point to point (receive)
05 - Card modem loopback
06 - Card modem on-line test
07 - Dial tester test
99 - Exit to DIAGNOSTIC TEST MENU


SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Note: Communication mode of subtest 01 - 05 is as follows;
Async, 9600 BPS, 8 data bit + parity (even), 1 step bit, data = 20H - 7EH.
From subtest 03 to subtest 07 need the channel selection.

Subtest 01 Wrap around test (channel - 1)

Performs a data send/receive test with the wraparound connector for the channel 1.

Subtest 02 Wrap around test (channel - 2)

Performs the same test as subtest 01 for the channel 2.

Subtest 03 Point to point test (send)

Sends data (codes 20H through 7EH) to another communication device referred to as a receiver, and receive the data from the receiven, then compared them with original data.

Subtest 04 Point to point test (receive)

Receives the data from another communication device (referred to as a transmitter) comparesthem with original data then back the data to the transmitter.
Note: Subtest 03 (send side) and subtest 04 (receive side) is pare.

Subtest 05 Card modem loopback test

Sends data to a card modem, then receives the data looped back in the card modem, then compares them with original data.

Subtest 06 Card modem on-line test

Sends data to a card modem through data a PBX, then receive looped back and compares them with original data.
Communication mode is 110/300/1200 BPS, 8 data bits + no parity, 1 stop bit, data = 20H - 7EH codes.

To be continued.

Subtest 07 Dial tester test

Performs pules dial and tone dial test with a dial tester.
The pulse dial test sends the pulse "1-2-3-4-5-6-7-8-9-0-1-2" twice.
The tone dial send the data "1-2-3-4-5-6-7-8-9-*-0-#" twice.

8.10 HARD DISK TEST

Summary of the HARD DISK Test

WARNING

The data on the HDD will be lost permanenty during the write operations in subtests 2, 3, 4, 6 and 8.

Current disk contents will be completely destroyed. Save the data on Hard Disk before execute this program if you don't want to do so.

If you execute the subtest 2, 3, 4, 6 and 8 must set the partition of HDD. (Refer to 8.20 Set the partition)

This test performs the read/write test with sequential address, randam address, and specified address and so on for HDD and its controller function.

To be continued.

Subtest and test mode selection

After pressing "8" and "ENTER" keys appear the following message on the screen.

Test drive number select (1: HDD1, 2: HDD2, 0: HDD1&2) ?

1: Executes the test of only drive 1.
2: Executes the test of only drive 2.
3: Executes the test of drive 1 and drive 2.

After you choose the above number, then press it.
The following screen appears for subtest selection.

```
HARD DISK TEST                          XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Sequential read
02 - Address uniquence
03 - Random address/data
04 - Cross talk & peek shift
05 - Write/read/compare(CE)
06 - Write specified address
07 - Read  specified address
08 - ECC circuit (CE cylinder)
99 - Exit to DIAGNOSTIC TEST MENU



SELECT SUB-TEST NUMBER  ?
```

Selected desired subtest by pressing two digits subtest number in **SUBTEST MENU** as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer to the **ANNEX C** for error status code.

Subtest description

Subtest 01 Sequential read test(CYL.0-610,CYL.610-0)

Performs the Forword Read(0-610 tracks) and Reverse Read(610-0 tracks).

Subtest 02 Address uniquence test

Writes the address data(sector by sector) track by track, then reads the data and compare them. Following three kind of reads operations are performed.
(Forward sequential, Reverse sequential, Randam)

Subtest 03 Randam address/data test

Write, read and compare the data at randam address (Cyl, Head, and Sec) and randam length.

Subtest 04 Cross talk & peek shift test

Write, read and compare the worst pattern data (8types such as B5ADADH, 4A5252H, EB6DB6H, 149249H, 63B63BH, 9C49C4H, 2DB6DBH, and D24924H) cylinder by cylinder to check the interference between the tracks.

Subtest 05 CE cylinder(611) Write/Read/Compare test

The Worst pattern data (B5ADADH) is used in this test.

Subtest 06 Specified address write test

Writes the data at the specified cylinder and head address.

Subtest 07 Specified address read test

Read the data at the specified cylinder and head address.

Subtest 08 ECC circuit test

Checks the ECC circuit functions at CE cylinder (611 cylinder).

8.11 REAL TIMER TEST

Summary of the REAL TIME test

This test performs the check test of the calender and timer.

Subtest and test mode selection

After pressing "9" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
REAL TIME TEST                          XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Real time test
02 - Backup memory test
03 - Real time carry test
99 - Exit to DIAGNOSTC TEST MENU




SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two dights subtest number in SUBTEST MENU as shown above and "ENTER".

Subtest description

Subtest 01 Real time test

The Current date and time are display, and new date and new time are possible to be entered.

Subtest 02 Backup RAM test

Prepare the data = FFH, AAH, 55H, 00H about reading and writing to 64 bytes.

Subtest 03 Real timer set

WARNING : If this test execute, Current date and Current time return to "12-31-1985" "23:59:55".

Confirm that up date Current date and time are displayed on the screen.
Start the from the menu as follow.

Current date : 12-31-1985

Current time : 23:59:55

8.12 HARD DISK FORMAT

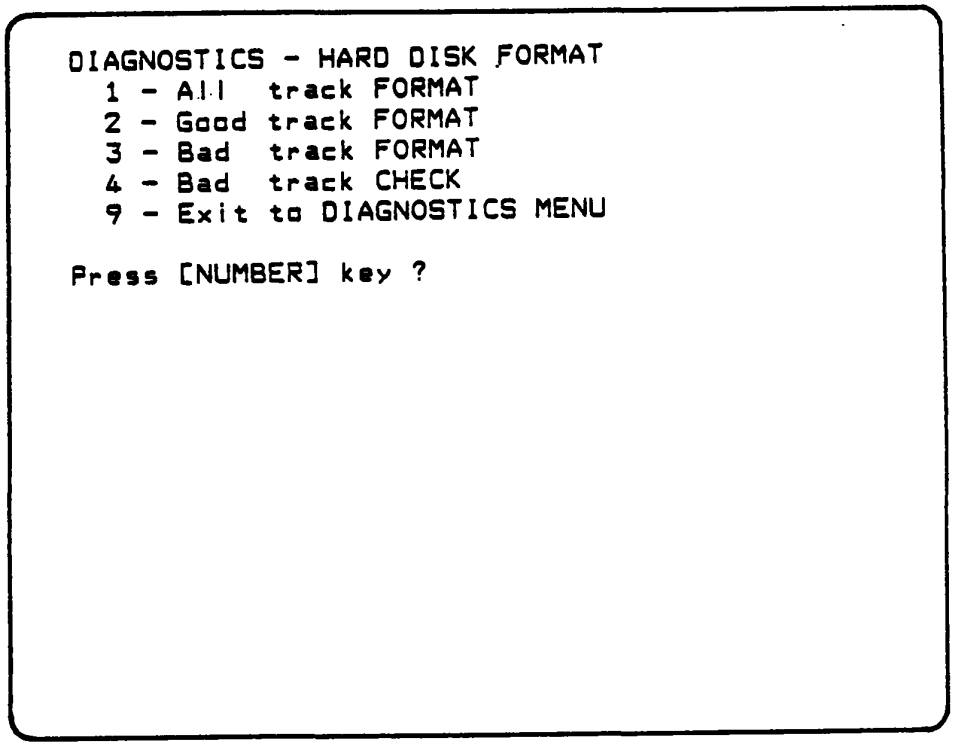
Summary of the program

WARNING : Current disk contents will be completely destroyed. Save the data on Hard Disks before execute this program if you don't want yo do so.

If Formats a Hard Disk Drive with the specified format and 4 types operation described in program description on next page.

Program execution

After pressing "2" and "ENTER" keys at task selection of **DIAGNOSTIC MENU** , the following screen appears before execution.



Program description

(1) All track FORMAT (Execution time 6 minutes)

Executes format of Hard Disk.

Secter sequence	:	3
Cylinder	:	612 (0 - 611)
Head	:	2 (0 - 1)
Sector	:	17 (1 - 17)
Sector length	:	512 Byte/sector
Bad track	:	Up to 12 tracks (If more than track were typed-in, the program is terminated.)

All track format execute as follws.

1. Reads the all track, and then check the Bad track information now.
2. You input the Bad track information.
3. Formats the all track by Good track format.
4. Writes the Bad track by information of 1 and 2.
5. Executes Read test to all track, and error track dicide the Bad track.

(2) Good track FORMAT (Execution time 1 second)

Executes the format of appointed cylinder and track as good-track.

(3) Gad track FORMAT (Execution time 1 second)

Executes the format of appointed cylinder and track as bad-track.

(4) Bad track CHECK (Execution time 1 and half minutes)

Check for the bad-track by read operation about all-track on the Hard Disk, then it display list of bad-track.

8.13 SEEK TO LANDING ZONE

Summarry of the program

This program moves head of the Hard Disk Drive to Landing Zone.

Note: When it does not issues any command to HDD for 5 seconds, heads of the Hard Disk Drive moves to Landing zone antomatically.

8.14 HEAD CLEANING

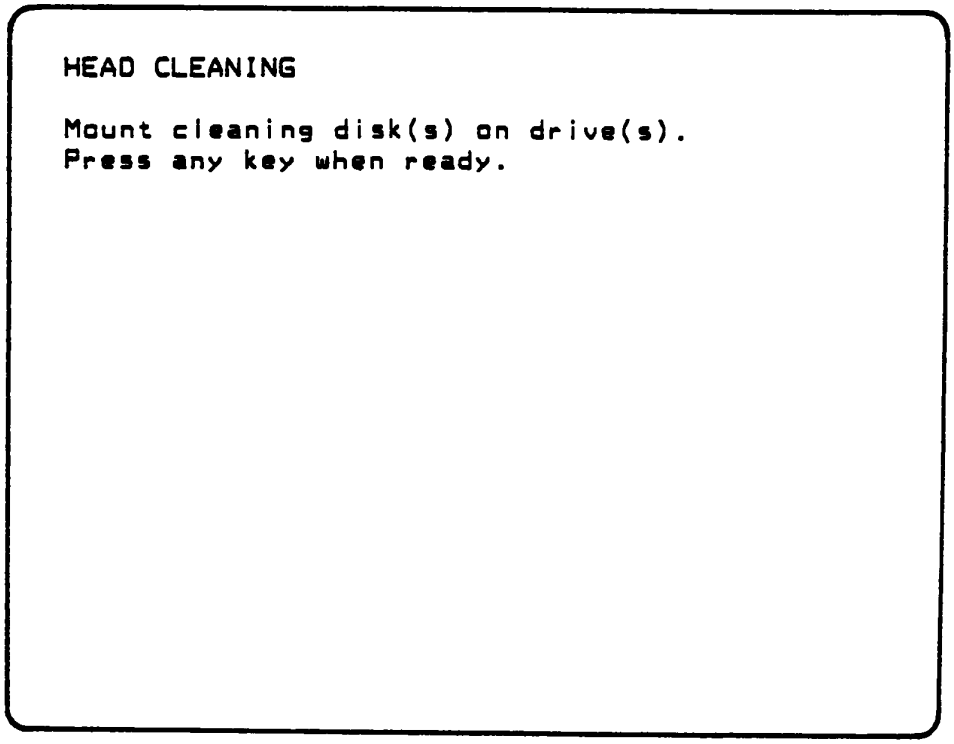
Summary of the program

It executes the head load, seek and read operation for the purpose of head cleaning.

The Cleaning Disk Kit(Part No.) is required to perform the cleaning properly.

Program execution

After pressing "4" and "ENTER" at task selection of **DIAGNOSTIC MENU** , the following screen appears before test execution.



After the above message apper on the screen, then set the Cleaning Disk to FDD and press the any key.

The message of **"Cleaning start"** is displayed on the screen and Head Cleaning is executed.

When it is finished, it return to the **Diagnostic Menu** .

8.15 LOG UTILITY

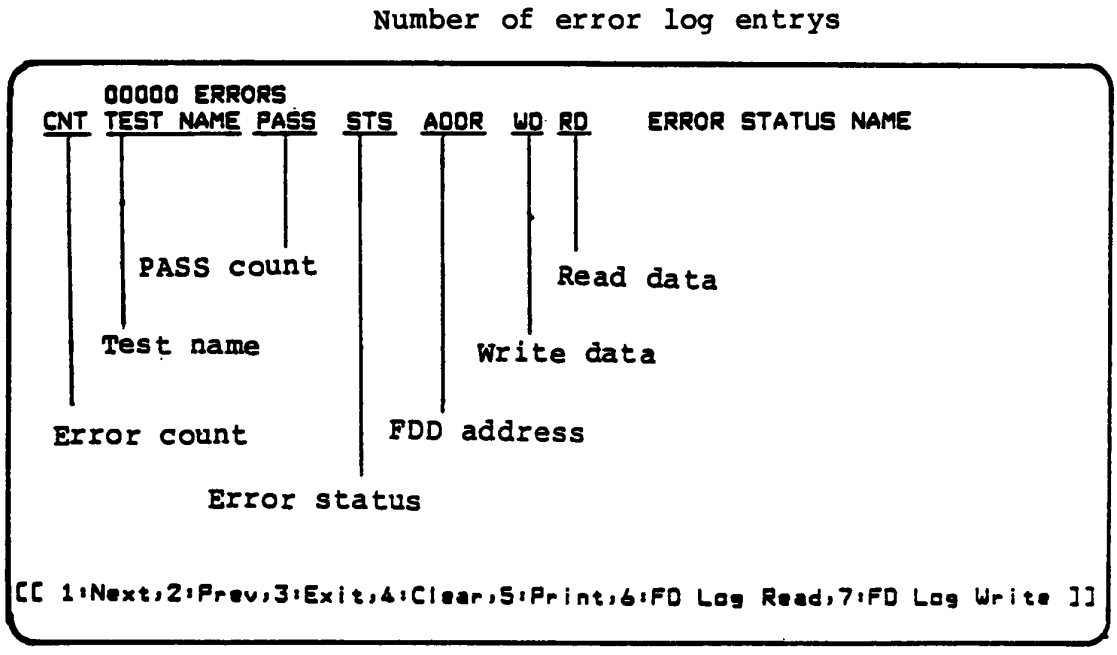
Summary of the program

The error information detected while testing is logged in the memory or the test floppy disk.
The logged error information is able to be displayed on the CRT or be printed out through the printer.

Program execution

The error information logged in the Memory or the floppy disk is displayed as shown below by press "5" key during the task selecting operation.

Error Display



Operation guide is displayed bottom of the screen.
Error status name is displayed right side of the screen.

The following functional keys are available for the error display screen.

"1" key : One page is scrolled upwards.

"2" key : One page is scrolled downwards.

"3" key : It returns to task selection.

"4" key : All error logs in RAM are erased.

To be continued.

"5" key : The error logs are printed out through the printer.

"6" key : The error logs in floppy disk are displayed on the CRT.

"7" key : The error logs in RAM are written to floppy disk.

Note : When the error retry was made successfully, the "R" character is added at the head of error status.
In this case, the error count is not updated.

8.16 RUNNING TEST

Summary of the program

The Running Test makes a sequential and continuous execution of the test programs specified by the test list of system parameter with taking no man's intervention. Under the execution of Running Test, it displays the test name and subtest number being currently executed.

Program execution

Prior to the execution of Running test, the screen shows the following messages asking of execution or non-execution of printer and ASYNC wraparound test, and display selection .

(1) **Printer wraparound test (1:YES/2:NO)?**

1 : It executes the printer wraparound test.

2 : It does not.

(2) **Async wraparound test (1:YES/2:NO)?**

1 : It executes the async wraparound test.

2 : It does not.

(3) **Media in drive mode (0:720, 1:360K-360K, 2:360K-1.2M, 3:1.2M-1.2M) ?**

0 : 720K-720K mode, 720KB-1.2MB mode

1 : 360K-360K mode

2 : 360K-1.2M mode, 360KB-720KB mode

3 : 1.2M-1.2M mode

The Running Test executes the following test programs

	Test name to be tested		Subtest number in sequential execution
	1. System	:	01
	2. Memory	:	01, 02, 03, 04
	3. Display	:	01 - 08
*	4. FDD	:	02
	5. Printer	:	03 (Printer Wraparound Connector Part No. is required.)
	6. RS232C	:	01 (CCM Wraparound Connector Part No. is required.)
	7. HDD	:	01, 05, 08
	8. Realtimer	:	02

Refer to **ANNEX A** , Test Program List, for summary of the subtests or Subtest description in each program module for the details.

(* mark : Automatically select "1"(one FDD) or "0"(two FDD.)

8.17 FDD UTILITES

(1) FORMAT

Formats a Floppy Disk
Two-sided doble density double-track, 48TPI,MFM mode
512 Byte, 9 sectors/track (2D)
Two-sided doble density double-track, 96TPI, MFM mode
512 Byte, 9 sector/track (2DD)

(2) COPY

Copys a Floppy Disk
Copy with one FDD (Drive A)
Copy with two FDDs (from drive A to B)

(3) DUMP

Displays contents of Floppy Disk (each type) or Hard Disk (designated sector).

8.18 SYSTEM CONFIGURATION

Summary of the program

It displays your system's configuration such as Memory size, Display type, Number of FDD(s), Number of HDD, Number of RS232C, Number of Printer and option.

```
SYSTEM CONFIGURATION :

  * - 640KB MEMORY
  * - PLASMA DISPLAY
  * - 1 FLOPPY DISK DRIVE(S)
  * - 1 ASYNC ADAPTER
  * - 1 HARD DISK DRIVE(S)
  * - 1 PRINTER ADAPTER
  * -    0KB EXPANSION MEMORY



PRESS [ENTER] KEY
```

Above message is an example of F/H type System.

8.19 SET UP

Summary of the program

This program displays System setup of T3100 System, then you can change it.

It displays your system's System Setup such as Current date, Current time, Number of FDD(s), Number of HDD(s), System memory size, Expansion memory size and Primary display.

```
[[ System setup ]]

  1.Current date        = 01-01-1986

  2.Current time        = 00:26:13

  3.Floppy disk drives= 1
       drive#1 type     = 0 - No drive
       drive#2 type     = 2 - 720KB/1.2MB

  4.Hard disk drives    = 1
       drive#1 type     = 1 - Cyl=612,h=2
       drive#2 type     = 0 - No drive

  5.System memory size=    640KB

  6.Expansion memory    =     0 KB

  7.Primary display     = 2 - Color(80col)


Select setup change (1:no/2:yes) ?
```

Above message is an example of F/H type System.

To be continued.

Program execution

Select setup change (1:no / 2:yes)

When you press the "1" key, return to the DIAGNOSTIC MENU. When you press the "2" key, appears the following message, then you can change the items of System setup.

Select change type (1:Auto / 2:Manual) ?

When you press the "1" key, set the autmatically system composition.
When You press the "2" key, the partial items are changed.

1: Standard setting

Date = 0 clear

Time = 0 clear

FDD = FDD type check of FDD 1 or 2

System memory size = BIOS call

Expansion memory size = CMOS call

Display = BIOS call

2: Partial setting

Date and time

Floppy Disk Drive type

Hard Disk Drive type

System memory size

Expansion memory size

Display type

Note: It executes partial setting in order of above items to changing it.
In the case of no change, go to the next item to only "RETURN" key.

8.20 Set the partition

Summary of the program

This program set the partition of Hard Disk.

In the case of following items, you need to set the partition of Hard Disk.

1. Replacing the good spare HDD.
   Note: After formating the HDD, executes it.
   (Refer to paragraph 8.12)

2. Breaking the media of HDD.

3. Executing the Hard Disk Test of Test & Diagnostic.

To be continued.

Program execution

Insert the MS-DOS System Disk into the internal disk drive, then turn on the power of the T3100 System.
After MS-DOS loading, press the "ENTER" key twice.
INPUT **"FDISK"** then press "ENTER" keys, then the following screen appears for the partiton setting.

```
Fixed Disk Setup Program                          / Drive #1

 Total  611 cylinders  ( 17kb/cylinder)

 Partition Type Status Start  End  Size

   1       DOS   A          0  610   611

 Max. available space :     -    -     0




Choose one of the following options                    : 1

   1 : Create Partition
   2 : Change Active Partition
   3 : Delete Partition


Press ESC to return to DOS/FDISK option
```

1: Executes partition setting

2: Changes the strat address and end address of the partition.

3: Deletes the partition setting.

Refer to OWNER"S MANUAL.

ANNEX A : TEST PROGRAM LIST

TEST No.	TEST NAME	SUBTEST No.	TEST ITEM
1	SYSTEM	01	ROM Checksum
2	MEMORY	01 02 03 04	Constant Data R/W test Address Pattern R/W test Memory Refresh Test Protect Mode test
3	KEYBOARD	01	
4	DISPLAY	01 02 03 04 05 06 07 08	Video RAM R/W Test Character Attribute display Character Set display 80 x 25 display 320 x 200 Graphic display 640 x 200 Graphic display 640 x 400 Graphic display Screen Page Test
5	FDD	01 02 03 04 05	Sequential Read Test Sequential R/W Test Random Address/Data R/W Test Specified Address Write Test Specified Address Read Test
6	PRINTER	01 02 03	Ripple Pattern Test Function Test Wraparound Test (It needs wraparound connector.)
7	ASYNC/ (RS232C)	01 02 02 03 04 05 06 07	Wraparound (chanel-1)Test (It needs wrapround connector) Wraparound (chanel-2)Test (It needs wrapround connector) Point to point Test (send) ( ) Point to point Test (recive) ( ) Card modem loopback Test Card modem on-line Test Dial tester Test

ANNEX A : TEST PROGRRAM LIST (Continued)

TEST No.	TEST NAME	SUBTEST No.	TEST ITEM
8	HDD	01	Sequential read Test
		02	Address uniquence Test
		03	Random address/data Test
		04	Cross talk & peek shift Test
		05	Write/read/compare(CE) Test
		06	Write specified address Test
		07	Read specified address Test
		08	ECC circuit (CE cylinder) Test
9	Real time	01	Real time Test
		02	Backup memory test
		03	Real time carry test

ANNEX B : AVERAGE EXECUTION TIME

TEST NO.	TEST NAME	SUBTEST NO.	EXECUTION TIME
1	SYSTEM	01	1 Second
2	MEMORY (640 KB)	01	30 Seconds
		02	10 Seconds
		03	20 Seconds
		04	3 Seconds
3	KEYBOARD	01	
4	DISPLAY	01	1 Second
		02	1 Second
		03	1 Second
		04	1 Second
		05	3 Second
		06	3 Second
		07	5 Second
		08	15 Second
5	FDD	01	65 Seconds
		02	130 Seconds
		03	12 Seconds
		04	1 Second
		05	1 Second
6	PRINTER	01	110 Seconds
		02	15 Seconds
		03	1 Second
7	ASYNC/ (RS232C)	01	1 Second
		02	1 Second
		03	1 Second
		04	1 Second
		05	5 Second
		06	10 Second
		07	60 Second

ANNEX B : AVERRAGE EXECUTION TIME (Continued)

TEST NO.	TEST NAME	SUBTEST NO.	EXECUTION TIME
8	HDD	01	6 Second
		02	10 Second
		03	30 Second
		04	13 Second
		05	2 Second
		06	1 Second
		07	1 Second
		08	2 Second
9	Real Time	01	
		02	
		03	

ANNEX C : ERROR STATUS CODE LIST

DEVICE NAME	ERROR CODE	STATUS
SYSTEM	01	ROM Checksum Error
MEMORY	01	Parity Error
	02	PROTECTED MODE NOT CHANGE ERROR
COMMON	FF	Compare error
FDD	01	Bad Command
	02	Address Mark Not Found
	03	Write Protected
	04	Record Not Found
	06	Media removed on dual attach card
	08	DMA Overrun Error
	09	DMA Boundary Error
	10	CRC Error
	20	FDC Error
	40	Seek Error
	60	FDD not drive
	80	Time Out Error
PRINTER	01	Time Out
	08	Fault
	10	Select Line
	20	Out of Paper
	40	Power off
	80	Busy Line
ASYNC/ (RS232C)	01	DSR Off Time Out
	02	CTS Off Time Out
	04	RX EMPTY Time Out
	08	TX BUFFER FULL Time Out
	10	Parity Error
	20	Framing Error
	40	Overrun Error
	80	Line Status Error
	88	Modem Status Error
	33	NO CARRIER (CARD MODEM)
	34	ERROR (CARD MODEM)
	36	NO DIAL TONE (CARD MODEM)

ANNEX C ERROR SRAYUS CODE LIST (Continued)

DEVICE NAME	ERROR CORD	STATUS
HDD	01	Bad command error
	02	Bad address mark
	04	Record not found
	05	HDC NOT RESET
	07	Device not initialize
	09	DMA Boundary error
	0A	Bad secter error
	0B	Bad track error
	10	ECC error
	11	ECC recover enable
	20	HDC error
	40	Seek error
	80	Time out error
	AA	Device not ready
	BB	Undefined
	CC	Write fault
	E0	Status error
	F0	Not sense error (HW.code=FF)

ANNEX D : WRAPAROUND CONNECTOR

1. Wraparound connector for printer (Dsub 25 pin male)

(1)	- STROBE	———	- ACKNOWLEDGE	(10)
(9)	+ DATA BIT 7	———	+ P. END	(12)
(14)	- AUTO FEED	———	- ERROR	(15)
(16)	- INITIALIZE PRINTER	———	+ SELECT	(13)
(17)	- SELECT INPUT	———	+ BUSY	(11)

2. Wraparound connector for RS232C

(3)	TRANSMIT DATA	———	RECEIVE DATA	(2)
(7)	REQUEST TO SEND	———	CLEAR TO SEND	(8)
		———	CARRIER DETECT	(1)
(4)	DATA TERMINAL READY	———	DATA SET READY	(6)
		———	RING INDICATE	(9)

3. Direct connection cable for RS232C

(Dsub 9 pin Fumale)			(Dsub 9 pin Fumale)	
(3)	TD	———	RD	(2)
(4)	DTR	———	DSR	(6)
		———	CTS	(8)
		———	RI	(9)
(7)	RTS	———	CD	(1)
(5)	GND	———	GND	(5)
(2)	RD	———	TD	(3)
(1)	CD	———	RTS	(7)
(6)	DSR	———	DTR	(4)
(8)	CTS			
(9)	RI			

APPENDIX A

Bus Driver GA (Gate Array)

The Bus Driver Gate Array is a x,xxx gate flat package type with 100 lead chip.
The Bus Drive Gate Array has following functions.

- o Input/Output control of the data bus.
- o To generates system address
- o To generates memory refresh Address

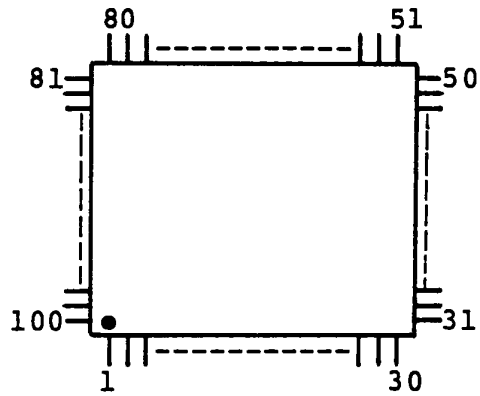
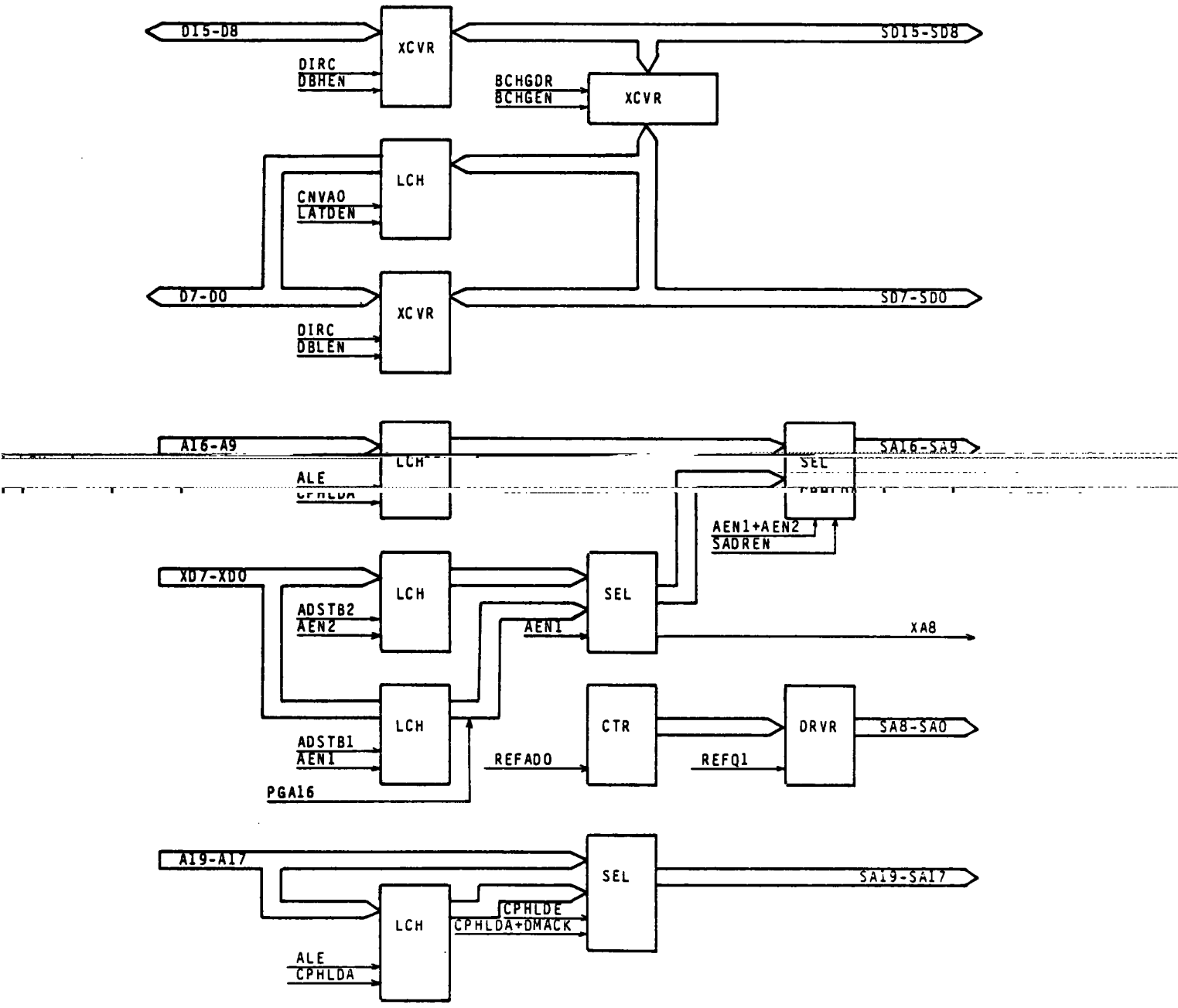


Figure A-1 Bus Driver GA



Where
XCVR: Transceiver
DRVR: Driver
SEL : Selecter
LCH : Latch
CTR : Counter

Bus Driver GA Interface Signal

Pin	I/O	Signal Name	Description
1	I	CPHLDA	CPU hold acknowledge signal. When this signal is high, the system bus is used by the other than the CPU. If it is low, the system bus is used by the CPU.
2	I	ALE	CPU address latch signal. This signal is active high.
3		VCC	+5v
4	I	PGA16	This signal is a part of DMA address from the page register of the Memory Mapper GA.
5	I	DIRC	Data transfer direction signal in CPU access mode. When this signal is low, the data goes to the CPU (read cycle). When this signal is high, the data comes from the CPU (write cycle).
6	I	BUSEN	Data bus enable signal. This signal controls data enable timing during CPU read/write operation. This signal is active high.
7	I	XD0	XD7-XD0 are data bus from I/O controllers. The DMAC outputs DMA address on the data bus in DMA operation. Data bus bit 0.
8	I	XD1	Data bus bit 1.
9	I	XD2	Data bus bit 2.
10	I	XD3	Data bus bit 3.
11	I	XD4	Data bus bit 4.
12	I	XD5	Data bus bit 5.
13	I	XD6	Data bus bit 6.
14	I	XD7	Data bus bit 7.
15		GND	Ground
16	I	AEN1	Address enable signal for slave DMA. This signal is active low.
17	I	AEN2	Address enable signal for master DMA. This signal is active low.
18	I	A9	A19-A9 are CPU address lines. These lines also come from the Memory Mapper GA for DMA address transfer. CPU address line bit 9.
19	I	A10	CPU address line bit 10.
20	I	A11	CPU address line bit 11.
21	I	A15	CPU address line bit 15.

Bus Driver GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
22	I	A12	CPU address line bit 12.
23	I	A13	CPU address line bit 13.
24	I	A17	CPU address line bit 17.
25	I	A19	CPU address line bit 19.
26	I	A14	CPU address line bit 14.
27	I	A16	CPU address line bit 16.
28		Vcc	+5v
29	I	A18	CPU address line bit 18.
30	I	DMACK	This signal is generated by CPHLDA signal. When this signal is low, it is CPU mode. When this signal is high, it is DMA mode.
31	O	XA8	DMA address.
32	I/O	SD15	SD15-SD0 are system data bus. SD15-SD8 are a high bank and SD7-SD0 are a low bank. System data bus bit 15.
33	I/O	SD14	System data bus bit 14.
34	I/O	SD13	System data bus bit 13.
35	I/O	SD12	System data bus bit 12.
36	I/O	SD11	System data bus bit 11.
37	I/O	SD10	System data bus bit 10.
38	I/O	SD9	System data bus bit 9.
39	I/O	SD8	System data bus bit 8.
40		GND	Ground
41	I/O	SD7	System data bus bit 7.
42	I/O	SD6	System data bus bit 6.
43	I/O	SD5	System data bus bit 5.
44	I/O	SD4	System data bus bit 4.
45	I/O	SD3	System data bus bit 3.
46	I/O	SD2	System data bus bit 2.
47	I/O	SD1	System data bus bit 1.
48	I/O	SD0	System data bus bit 0.
49	I	BCHGEN	This is an enable signal to transfer the 2nd byte while 16/8 bit conversion. It is also enabled while DMA byte is transferred. This signal is active low.
50	I	BCHGDR	This signal controls the direction of 2nd byte transfer in 16/8 bit conversion or DMA byte transfer. When this signal is low: High bank → Low bank. When this signal is high: High bank ← Low bank.

Bus Driver GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
51	O	SA6	System address lines. SA8-SA0 are used in memory refresh cycle, and SA15-SA9 are used in CPU/DMA mode as a part of system address. System address line bit 6.
52		NO USE	
53		VCC	+5v
54	O	SA9	System address line bit 9.
55	O	SA7	System address line bit 7.
56	O	SA8	System address line bit 8.
57	O	SA10	System address line bit 10.
58	O	SA13	System address line bit 13.
59	O	SA11	System address line bit 11.
60	O	SA12	System address line bit 12.
61	O	SA5	System address line bit 5.
62	O	SA3	System address line bit 3.
63	O	SA4	System address line bit 4.
64	O	SA2	System address line bit 2.
65		GND	Ground
66	O	SA1	System address line bit 1.
67	O	SA14	System address line bit 14.
68	O	SA15	System address line bit 15.
69	O	SA16	System address line bit 16.
70	O	SA17	System address line bit 17.
71	O	SA18	System address line bit 18.
72	O	SA0	System address line bit 0.
73	O	SA19	System address line bit 19.
74	I	DBHEN	High bank data bus (SD15-SD8) enable signal. This signal is active high.
75	I	DBLEN	Low bank data bus (SD7-SD0) enable signal. This signal is active high.
76	I	LATDEN	This signal is to read the 1st byte latched to the internal buffer during 16/8 bit conversion. 1st byte is read out while 2nd byte read timing if this signal is active. This signal is active low.
77	I	CNVA0	This signal is dummy address for 2nd byte in 16/8 bit conversion. This signal stores the 1st byte to the internal buffer while read operation. This signal is active high.
78		Vcc	+5v

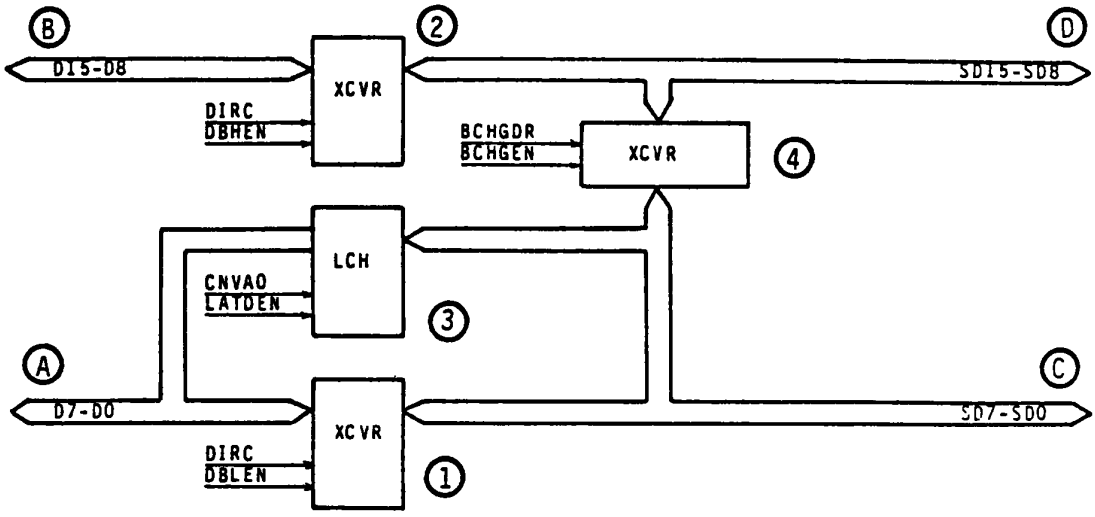
Bus Driver GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
79	I	REFAD0	This signal is a refresh address (least significant bit). It is output as SA0. This signal is also used as a clock signal of the internal refresh address counter.
80	I	REFQ1	This signal is to output the refresh address to the system bus. This signal outputs the content of the refresh address counter.
81	I	ADSTB1	Slave DMAC address strobe signal. This signal is used to latch the DMA address which has been on the data bus.
82	I/O	D15	CPU data bus from/to the CPU. (D15-D8 is high bank, D7-D0 is low bank) CPU data bus bit 15.
83	I/O	D14	CPU data bus bit 14.
84	I/O	D13	CPU data bus bit 13.
85	I/O	D12	CPU data bus bit 12.
86	I/O	D11	CPU data bus bit 11.
87	I/O	D10	CPU data bus bit 10.
88	I/O	D9	CPU data bus bit 9.
89	I/O	D8	CPU data bus bit 8.
90		GND	Ground
91	I	ADSTB2	Master DMAC address strobe signal. This signal generates DMA address. It is active high.
92	I/O	D7	CPU data bus bit 7.
93	I/O	D6	CPU data bus bit 6.
94	I/O	D5	CPU data bus bit 5.
95	I/O	D4	CPU data bus bit 4.
96	I/O	D3	CPU data bus bit 3.
97	I/O	D2	CPU data bus bit 2.
98	I/O	D1	CPU data bus bit 1.
99	I/O	D0	CPU data bus bit 0.
100		NO USE	

1. Data Bus Control

This circuit controls the data bus between the CPU and I/O port or memory. 8/16 bit conversion is performed with this circuit.

Figure A-2



1) Word Access

When the I/O port connected to the data bus is word oriented, no data conversion is performed.

Low bank : (A) ⟷ (C)

High bank: (B) ⟷ (D)

(refer to Fig. A-2)

In this case, read/write cycle is complete in three CPU cycle. (no wait cycle request is included.)

2) Byte Access

Followings are for the case of byte access.
The I/O port is connected to the low bank of the data bus.

o Word Read Operation

The 1st data byte (even address data) transferred from Ⓒ is latched to the buffer ③ temporarily.
The consequent 2nd byte data (odd address data) is transferred to the D15-D8 (Ⓑ) through the transceiver ④.
At this time, the 1st data byte in the buffer ③ is enabled to be output to the data bus D7-D0 (Ⓐ), thus 16 bit data is transferred to the CPU. The transceiver ① is disabled while 2nd data byte transfer time.

1st data byte : Ⓐ ⟶ ③ ⟶ Ⓒ
2nd data byte : Ⓑ ⟶ ④ ⟶ Ⓒ

(refer to Fig. A-2)

o Word Write Operation

16 bit write data from the CPU is output to Ⓐ and Ⓑ through the data bus D15-D0.
The low bank data D8-D0 is transferred to Ⓒ through the transceiver ① as 1st data byte.
The high bank data D15-D9 is transferred to Ⓒ through the transceiver ② and transceiver ④ as 2nd byte.

1st data byte : Ⓐ ⟶ ① ⟶ Ⓒ
2nd data byte : Ⓑ ⟶ ② ⟶ ④ ⟶ Ⓒ

(refer to Fig. A-2)

The transceiver ① is disabled while 2nd byte transfer.
The buffer ③ is disabled while write operation.
This word/byte conversion occupys 12 system clock cycle time.

3) DMA Operation

o Byte DMA Operation

DMA data transfer between I/O port connected to low bank data bus and memory location of odd address is as follows.

Case of I/O to Memory : Ⓒ ⟶ ④ ⟶ Ⓓ

Case of Memory to I/O : Ⓓ ⟶ ④ ⟶ Ⓒ

(refer to Fig. A-2)

o Word DMA Operation

The GA is not concerned in the DMA operation.

2. Address Generation

System address SA19-SA0 is generated in this GA. And it is used as following purposes.

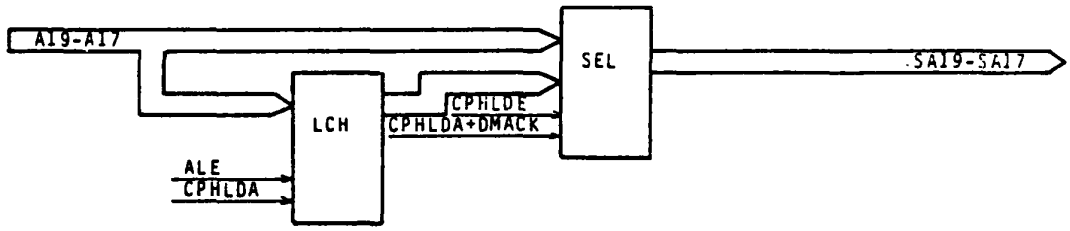
- o CPU address output: SA19-SA9
- o DMA address output: SA19-SA9,XA8
- o Refresh address output: SA8-SA0

To generate the system address, following three functional blocks are applied.

SA19-SA17

A19-A17 comes from the CPU and from the Memory Mapper GA. They are wired ORed.

Figure A-3

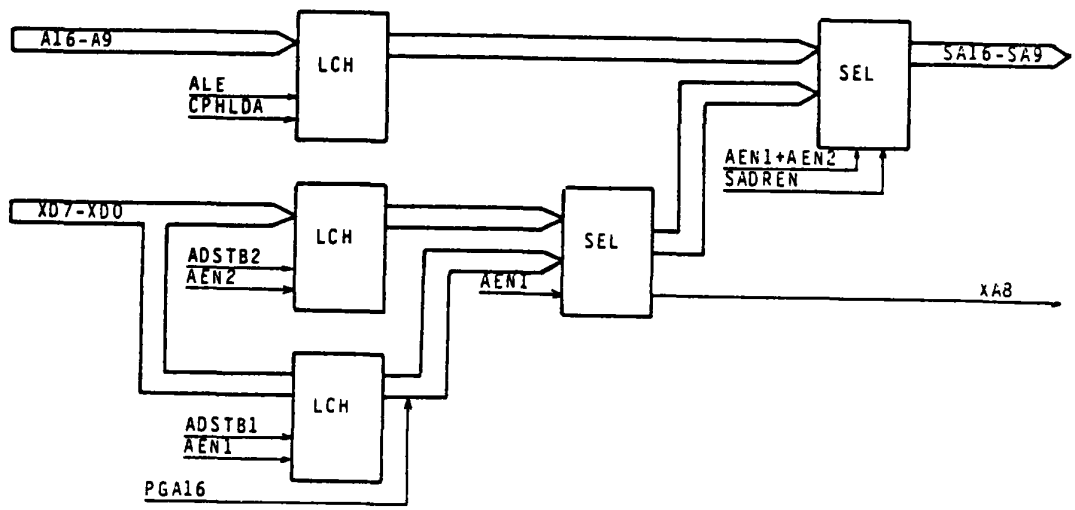


The CPU address (A19-A17) is output to SA19-SA17 while CPU mode.
The DMA address (A19-A17) is output to SA19-SA17 while DMA mode.

SA16-SA9,XA8

These lines are use to output the CPU address A16-A9 to SA16-SA9 or output the DMA address PGA16, XD7-XD0 to SA16-SA9, XA8.

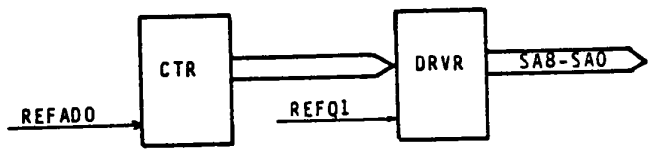
Figure A-3



SA8-SA0

These address lines are used to output the memory refresh address. The address is generated by refresh address counter and it is output at every 15 μ seconds.

Figure A-4



APPENDIX B

Memory Mapper GA (Gate Array)

The Memory Mapper Gate Array is a x,xxx gate flat package type with 100 lead chip.
The Memory Mapper Gate Array has following functions.

- o To generate DMA memory address.
- o To decode I/O address.
- o Miscellaneous functions.

  ROM control signal
  Timer clock
  Parity error detection control
  NMI (Non Maskable Interrupt) signal

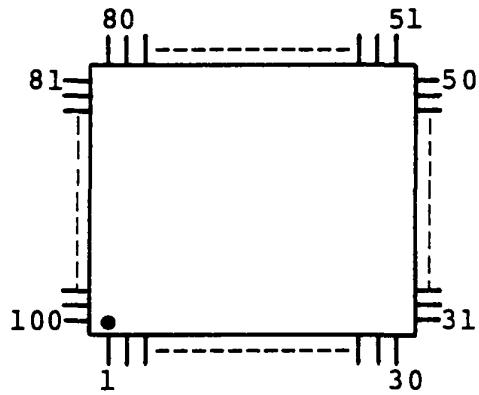
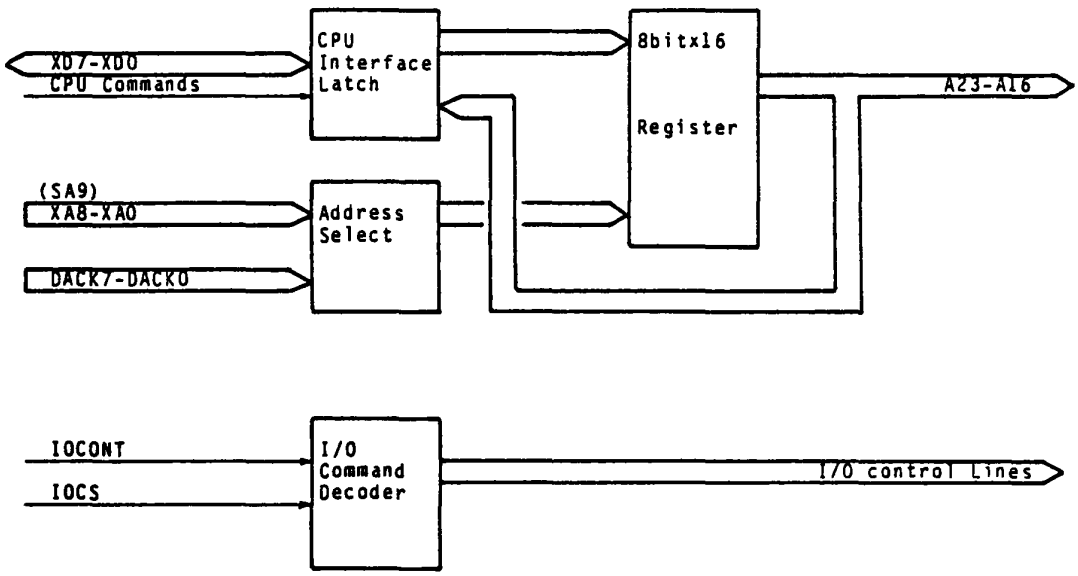


Figure B-1 Memory Mapper GA



Memory Mapper GA Interface Signal

Pin	I/O	Signal Name	Description
1	I	CPHLDA	CPU hold acknowledge signal. When this signal is high, the system bus is used by the other than the CPU. If this signal is low, the system bus is used by the CPU.
2	I	MIO	Memory I/O select signal. When this signal is high, it is memory cycle. When this signal is low, it is I/O cycle.
3		VCC	+5v
4	O	SPK	Buzzer signal from the external circuit.
5	O	KBCCS	Keyboard controller select signal. This signal becomes low when the I/O port address is 062h-068h(even).
6	O	LROMCS	Chip select signal to the BIOS ROM. This signal is active low. The address ranges are: 0E0000h-0FFFFFh FE0000h-FFFFFFh
7	O	ROMOE	Output enable signal to the BIOS ROM. This signal is generated by the ROM chip select signal and the memory read command. This signal is active high.
8	I	SBHE	System bus high enable signal. This signal generates the data bus high enable signal. This signal is active low.
9	I	MEMR	Memory read command.
10	I	LATA0	This signal comes from the DMA controller GA and it is generated from SA0. When this signal is high, the low bank of the data bus is selected.
11	I	CNVALE	Dummy address latch enable signal for the 2nd byte transfer in 16/8 bit conversion. This signal also generates output enable signal of the 1st byte which has been latched.
12	O	PGA16	Address line from the Memory Mapper register in DMA cycle or memory refresh cycle. This signal is used as SA16 while slave DMA operation.
13	O	NDPCS	This signal defines that the NDP (80287) has been selected. If this signal is low, it disable the system data bus. When 0F8h*SMIO*INTAi is made, this signal becomes active.

Memory Mapper GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
14	I	DIRC	Direction signal for CPU data transfer. When this signal is low, read data is on the data bus. When this signal is high, write data is on the data bus.
15		GND	Ground
16	I	DEC16M	This signal becomes high when the memory access is in word mode.
17	O	DBLEN	Data bus (low bank) enable signal. This signal is generated form LATA0 signal. This signal is active high.
18	O	DBHEN	Data bus (high bank) enable signal. This signal is generated from SBHE signal. This signal is active high.
19	O	LATDEN	This signal is read enable signal for the 1st byte transfer in 16/8 bit conversion. The 1st byte has been stored in a buffer of the Bus Controller GA during the 1st read cycle.
20	O	NMI	NMI interrupt signal. It is active high. This signal is output when memory parity error or any error from expansion unit occurs.
21	O	BSYCPU	CPU busy signal to NDP. This signal is active low.
22	O	CMDLY	Time delay control signal to memory command or I/O command. When this signal is low, command delay is not made. When this signal is high, 1 CPU clock delay is made.
23	O	ROMCS	ROM chip select signal. This signal is active low. The address ranges are: 0F0000h-0FFFFFh FE0000h-FFFFFFh
24	I	RAM16	This signal becomes low when the system memory is accessed. This signal enables internal parity error detection flag.
25	O	PPICS	Peripheral I/O select signal. This signal becomes active when the I/O port address is 06*h-07*h. This signal is active low.
26	I	PUCLR	Power on reset signal. This signal is active low. This signal inhibits real timer write command during the reset period.

Memory Mapper GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
27	I	IOCHK	Error signal from an external expansion unit. If this signal is low, the NMI flag becomes to be on.
28		Vcc	+5v
29	I	INTA	This signal is to read the interrupt vector address. This signal comes from the interrupt controller (U8259A).
30	I	REFRESH	DRAM refresh enable signal. This signal is active high. The Memory Mapper address A23-A17 and PGA16 are output while memory refresh operation.
31	I	TM2OUT	Buzzer sound signal. This signal comes from the timer (U8254).
32	I	RESET	System reset signal. This signal is active high.
33	I	IOR	I/O read command. This signal is active low. It is used to read memory address register in the GA, system status or to generate commands.
34	I	IOW	I/O write command. This signal is active low. It is used to write memory address register in the GA or to generate commands.
35	I	ALE	Address latch enable signal from the CPU. This signal is active high.
36	O	TMCLK	Clock signal to the timer (U8254). 1.19 MHz.
37	O	TMGATE	Count control signal to the timer (U8254). When this signal is low, it disables to count. When this signal is high, it enables to count.
38	O	PITCS	Timer (U8254) chip select signal. This signal is active low. This signal becomes active when the I/O port address is 04*h-05*h.
39	O	PIC1CS	Chip select signal to the master interrupt controller (U8259A). This signal is active low. This signal becomes active when I/O port address is 02*h-03*h.
40		GND	Ground
41	O	DSTRB	Data read strobe signal to the real timer. This signal becomes active when read operation to the I/O port address 071h is executed. This signal is active low.

Memory Mapper GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
42	O	RETIMW	Data write command to the real timer. This signal becomes active when write operation to the I/O port address 071h is executed. This signal is active low.
43	O	DMA1CS	Chip select signal to the DMAC (U8237A). This signal become active when the I/O port address is 00*h. This signal is active low.
44	I	DACK6	DMA acknowledge signal from channel 6.
45	I	DACK2	DMA acknowledge signal fron channel 2.
46	I	DACK4	DMA acknowledge signal from channel 4.
47	I	DACK0	DMA acknowledge signal fron channel 0.
48	I	DACK7	DMA acknowledge signal from channel 7.
49	I	DACK3	DMA acknowledge signal fron channel 3.
50	O	IRQ13	Interrupt request signal of NDP error.
51	I	MASTER	System operation request signal from the external processer. This signal is active low.
52		GND	Ground
53		Vcc	+5v
54	I	NDPER	NDP error signal. Not used in T3100
55	I	NDPBS	NDP busy signal. Not used in T3100.
56	O	BALE	This signal is ORed signal of ALE and CPHLDA. This signal functions as address latch enable signal. This signal is active high.
57	I	SA9	System address. This signal is used to decode I/O port address.
58	O	DMACK	This signal is ORed signal of CPHLDA and MASTER signals. This signal is low except in DMA mode.
59	O	NDPRST	Reset command to the NDP. This signal is active high.
60	O	PIC2CS	Chip select signal to the slave interrupt controller (U8259A). This signal is active when the I/O port address is 0A*h-0B*h. This signal is active low.
61	O	DMA2CS	Chip select signal to the master DMAC (U8237). This signal is active when the I/O port address is 0C*h-0Dh. This signal is active low.
62	O	CS287	I/O reset signal to the NDP. This signal is not used in T3100.

Memory Mapper GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
63	I	MDSPK	Buzzer sound signal from the MODEM card.
64	I	PDINL	Parity error signal from the system memory (low bank). This signal is not used in T3100.
65		GND	Ground
66	I	PDINH	Parity error signal from the system memory (high bank). This signal is active low. It makes a NMI interrupt signal at the beginning of memory read if error occurs.
67		NO USE	Ground
68	O	STEP	Step signal to the FDD. This signal is active high.
69	I	RWSEK	Seek enable signal to the FDD. When this signal is low, it enables FDD seek operation. When this signal is high, it is FDD read/write operation.
70	I	FDSTEP	Step signal from the FDC. This signal is active high.
71		NO USE	Ground
72	O	A23	A23-A17 are used as page address in DMA operation. The page address from the internal register is output when the DMA acknowledge signal is low. Address line bit 23.
73	O	A22	Address line bit 22.
74	O	A21	Address line bit 21.
75	O	A20	Address line bit 20.
76	O	A19	Address line bit 19.
77	O	A18	Address line bit 18.
78		Vcc	+5v
79	O	A17	Address line bit 17.
80	I	$14MHZ	Clock signal to the timer (U8254). 14.31818 MHz
81	I	XA0	XA9-XA0 are X address which are same to the system address. They are used to decode the I/O port address or specify the DMA page register for read/write operation to page address register. X address line bit 0.
82	I	XA7	X address line bit 7.
83	I	XA6	X address line bit 6.
84	I	XA5	X address line bit 5.
85	I	XA4	X address line bit 4.

Memory Mapper GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
86	I	XA3	X address line bit 3.
87	I	XA2	X address line bit 2.
88	I	XA1	X address line bit 1.
89	I	XA8	X address line bit 8.
90		GND	Ground
91	O	XDREAD	Read enable signal to the peripheral I/O which is connected to the X data bus. This signal is active low. This signal is active when $\overline{INTA}$+NDPCS*SA9*XA8*$\overline{IOR}$ is made.
92	I/O	XD0	XD7-XD0 is X data bus. Read/Write operation of DMA page register and read operation of system status are done through this bus. X data bus bit 0.
93	I/O	XD1	X data bus bit 1.
94	I/O	XD2	X data bus bit 2.
95	I/O	XD3	X data bus bit 3.
96	I/O	XD4	X data bus bit 4.
97	I/O	XD5	X data bus bit 5.
98	I/O	XD6	X data bus bit 6.
99	I/O	XD7	X data bus bit 7.
100		GND	Ground

1. DMA Memory Address

DMA page address is stored to the DMA page address register in the Memory Mapper GA before it is used in the DMA cycle. The DMA pageaddress register has 8 bit length and it is output to the address lines A23-A17 and PGA16 during the DMA cycle. The every DMA channel has a DMA page address register and address is assigned as follows.

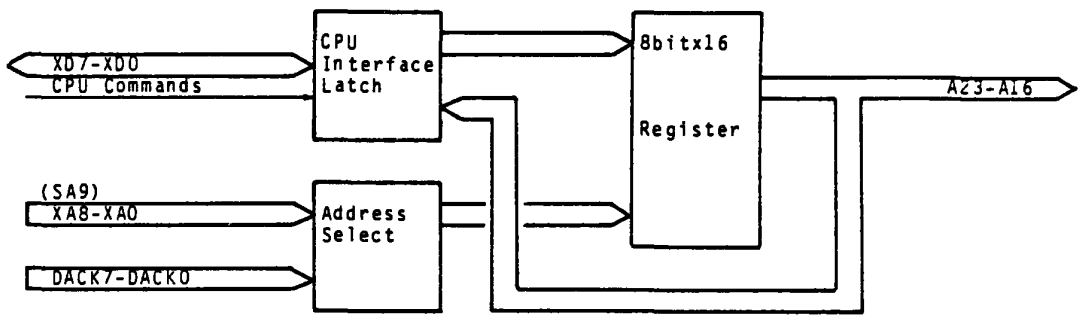
Table B-1 Address Asignment of DMA Address Register

Address	Channel	
081h	Channel 2	Slave DMA
082h	Channel 3	
087h	Channel 0	
089h	Channel 6	Master DMA
08Ah	Channel 7	
08Fh	* Refresh	

* It is used in memory refresh cycle.

To store the DMA page address, the address lines XA are decoded and the data on the XD lines is stored to the selected register.

Figure B-2 DMA Page Address Register



2. I/O Decode Control

Address lines SA9 and SA8-SA5 are used to generate the I/O port select signal.
Address on the XA lines are decoded for I/O port chip select if it is not DMA cycle.
Following Table B-2 shows the address assignment to each I/O port chip.

Table B-2 Address Assignment to The I/O port

Address	Signal Name	Description
00*h-01*h	DMA1CS	Slave DMAC select
02*h-03*h	PIC1CS	Master Interrupt Controller select
04*h-05*h	PITCS	Timer chip select
06*h-07*h	PPICS	Peripheral I/O select
08*h-09*h	PREGCS	Register select in the GA
0A*h-0B*h	PIC2CS	Slave Interrupt Controller select
0C*h-0D*h	DMA2CS	Master DMAC select
0E*h-0F*h	C287	NDP reset

APPENDIX C

DMA Controller GA (Gate Array)

The DMA Controller Gate Array is a x,xxx gate flat package type with 100 lead chip.
The DMA Controller Gate Array has following functions.

- o Clock generator.
  - CPU clock
  - DMA clock
  - Keyboard clock
- o System timing control.
  - Memory control (ROM, RAM)
- o DMA control.
- o Memory refresh control
- o DMA ready control.

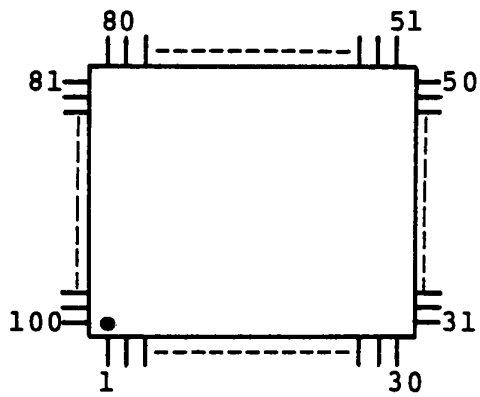
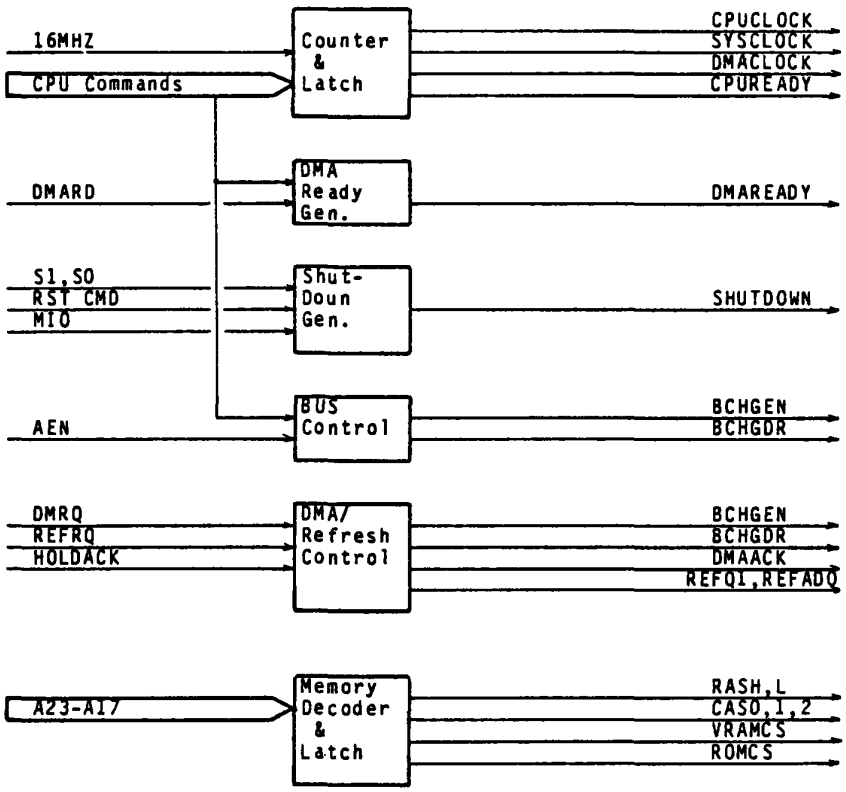


Figure C-1 DMA Controller GA



DMA Controller GA Interface Signal

Pin	I/O	Signal Name	Description
1	I	CPHLDA	CPU hold acknowledge signal. When this signal is high, the system bus is used by the other than the CPU. If this signal is low, the system bus is used by the CPU.
2	I	ALE	CPU address latch signal. The address data is latched at falling edge of the signal.
3		VCC	+5v
4	I	AEN1	Address enable signal in slave DMA operation. It enables the DMA address when this signal is low.
5	I	IOR	I/O read command. (output from U82288) I/O read operation is done when this signal is low.
6	I	IOW	I/O write command. (output from U82288) I/O wite operation is done when this signal is low. This signal is output from the DMAC (U8237) while DMA operation.
7	I	MIO	Memory I/O select signal. When this signal is high, it is memory cycle. When this signal is low, it is I/O cycle.
8	O	XBHE	Bus enable signal to X address bus. When this signal is low, it enables high bank of the X bus. This signal is generated within the GA in DMA operation. This signal is same to SBHE.
9	I/O	MEMR	Memory read command. This signal is output if it is memory refresh operation. Memory read operation is done when this signal is low.
10	I	MEMW	Memory write command. The write operation is done when this signal is low.
11	I	SEL4M	Clock rate select signal. This signal selects CPU clock rate. When this signal is low, the CPU clock rate is 8 MHz. When this signal is high, the CPU clock rate is 4 MHz.
12	I	CPUA20	Address line from the CPU. This signal is controlled within the GA. It depend on the CPU mode (Real mode / Protect mode). When it is real mode, A20 is fixed to low. When it is protect mode, CPUA2 is output to A20.

DMA Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
13	I	RSTCMD	CPU reset command. This signal is active low.
14	I	A0	CPU address line bit 0. This signal generates SA0 within the GA.
15		GND	Ground
16	O	RAMLSL	This signal becomes active when low bank of system memory (0-640 KB) is accessed or memory refresh cycle is executed. This signal is active high. This signal becomes RAS signal in external circuit.
17	O	RAMHSL	This signal becomes active when high bank of system memory (0-640 KB) is accessed or memory refresh cycle is executed. This signal is active high. This signal becomes RAS signal in external circuit.
18	O	CASCS0	This signal becomes high when the system memory (0-512 KB) is accessed. This signal is low when memory refresh cycle is executed. This signal becomes CAS signal in external circuit.
19	O	CASCS1	This signal becomes high when the system memory (512-640 KB) is accessed. This signal is low when memory refresh cycle is executed. This signal becomes CAS signal in external circuit.
20	I	A1	Shut down detection signal. This signal is low when S0/S1 are low and MIO is high.
21	I	A17	CPU/Memory Mapper address. Memory Mapper address is input while DMA operation. CPU/Memory Mapper address line bit 17.
22	I	A18	CPU/Memory Mapper address line bit 19.
23	I	A19	CPU/Memory Mapper address line bit 20.
24	I	A20	This signal used as follows. When it is real mode, this signal is fixed to low. When it is protect mode, CPU A2 signal is output.
25	I	A21	CPU/Memory Mapper address line bit 21.
26	I	A22	CPU/Memory Mapper address line bit 22.
27	I	A23	CPU/Memory Mapper address line bit 23.
28		Vcc	+5v
29		NO USE	

DMA Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
30	I	REAL	Real/Protect mode select signal. When this signal is low, the CPU is real mode. When this signal is high, the CPU is protect mode.
31	O	CLK42	Keyboard controller clock signal. The clock rate is a half of CPU clock.
32	O	AS18	Address strobe signal to the real timer (MC146818). This signal is active low.
33	I	$16MHZ	System clock signal. (16 MHz)
34	O	CPRDY	CPU ready signal. This signal is active low.
35	O	CPUCLK	CPU clock signal. It is 16 MHz/8 MHz.
36	I	S1	CPU bus status bit 1.
37	I	S0	CPU bus status bit 0.
38	I	NDPCS	NDP(80287) chip select signal.
39	I	TMIOUT	Memory refresh request signal. This signal is input at every 15 µs.
40		GND	Ground
41	I	GA3TS	Test signal for the GA.
42	I	PPICS	Peripheral I/O select signal. This signal generates real timer address strobe signal. When I/O address is 06*h/07*h, this signal becomes low.
43	I	PUCLR	Power on reset signal. This signal is active low.
44	O	DMACLK	DMA clock signal. It is a half of the system clock rate.
45	O	DMARDY	Ready signal to the DMAC. One wait cycle is given in a DMA operation. When this signal is low, it gives the wait cycle. When this signal is high, it is ready.
46	O	DMHLDA	Ack hold signal to the external DMAC. When this signal is high, it allows DMA operation.
47	I	DMHRQ	CPU hold request signal from the external DMAC. This signal is active high.
48	I	DMAMRD	Memory read command from the DMAC. This signal is active low.
49	I	DACK4	Slave DMAC cycle signal. This signal is active low. The master DMAC can not output address/command signal while this signal is active.

DMA Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
50	I	SA4	CPU/DMA address bit 4.
51	I/O	XA0	Address signal. This signal is from SA0 It is input while slave DMAC operation.
52		GND	Ground
53		Vcc	+5v
54	I	MSELC	Memory type select signal. When the system memory type is 64KBx4bit type, this signal is low. When the system memory type is 256KBx1bit type, this signal is high.
55	O	SMEMR	Memory read command. This signal is output to 8 bit expansion bus. It is not output to more than 1 MB address. This signal is active low.
56	O	SMEMW	Memory write command. The output condition of this signal is same to the SMEMR signal.
57	I	IORDY	CPU ready control signal from the external. When this signal is low, it is able to give a wait cycle.
58	O	DMAAEN	Address enable signal in a DMA operation. This signal is active low.
59	I/O	SBHE	System bus high enable signal. This signal enables the high bank of the data bus when this signal is active. This signal is generated within the GA in a DMA operation. When it is master mode, this signal is fixed to low. When it is slave mode, the signal is inverted of XA0.
60	I	IO16	This signal defines that 16 bit type of I/O device is serviced in I/O command execution.
61	I	MEM16	16 bit memory access signal. This signal comes from expansion memory board.
62	O	SYSCLK	System clock. It is a half of CPU clock rate.
63	O	DM1HLD	This signal is output when DMA request comes from the slave DMAC. When DACK4 is low, this signal becomes active (high).
64	I	ROM16	This signal is to connect the data from BIOS ROM to 16/8 bit data bus. When this signal is low, it connects the data to 16 bit data bus. When this signal is high, it connects the data to 8 bit data bus. (T3100 has only 16 bit data bus.)

DMA Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
65		GND	Ground
66	O	MEG1	This signal becomes low, when the memory address is more than 1 MB during the memory access. (Not used in T3100)
67	O	XMEMR	This signal is a memory command in a DMA cycle. This signal is generated from DMMRD signal.
68	I	REFRSH	Refresh enable signal. When this signal is high, it enables internal memory refresh circuit.
69	I	INTA	Interrupt vecter read signal. When this signal is low, it forces system address (SA0) to be low.
70	O	FREQ2	This signal is output signal from memory refresh control ccunter. This signal is active low. It makes memory read signal to be active.
71	I/O	SA0	System address. (least significant bit)
72		NO USE	Ground
73		NO USE	Ground
74	I	SA16	System address line bit 16. SA16 and SA15 are used to select the video memory chips.
75	I	SA15	System address line bit 15.
76	O	YME16	Color graphic video memory select signal. This signal is not used in T3100 system.
77	I	OWAIT	It gives 0 wait to the CPU cycle. When this signal is low, it enables to give two system cycle.
78		Vcc	+5v
79	O	CPURST	CPU reset signal. This signal is active high. When it is power on timing or shut down, this signal becomes active.
80	I	AEN2	Address enable signal in master DMAC operation. This signal is active low.
81	I	WAITIM	This signal is to give one wait cycle when it accesses the memory address more than 1 MB.
82	I	RAMOP	System memory (512KB-640KB) read/write enable signal. It enables to use the external memory card if this signal is high.(disable)

DMA Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
83	O	CRTMCS	Color graphic video memory select signal. (0B8000h-0BBFFFh)
84	O	RST	System reset. This signal becomes active when it is power on timing.
85	O	REFIN	Memory refresh enable signal. This signal is active high.
86	O	REFQ1	This signal is from memory refresh control counter. When this signal is low, the refresh signal is output.
87	O	REFAD0	Memory refresh address. (least significant bit)
88	O	CNVA0	This signal is dummy address for 2nd byte transfer in 16/8 bit conversion. The 1st byte is latched at raising point of this signal while read operation.
89	O	BCHGDR	This signal specifys the direction of 2nd byte transfer in 16/8 bit conversion. When this signal is low: high bank → low bank. When this signal is high: low bank → high bank.
90		GND	Ground
91	O	BCHGEN	This signal is an enable signal for the 2nd byte transfer in 16/8 bit conversion. This signal is active low.
92	O	CPUHRQ	CPU hold request signal. This signal is active high. This signal is generated when the DMHRQ signal is high.
93	O	CMDDIS	This signal is to terminate 1st byte read/ write operation in 16/8 bit conversion. When this signal is low, it forces the U82288 command to be inactive. This signal becomes high and makes the command to be active while the 2nd byte transfer timing.
94	O	RAM16	System memory (0-640KB) access signal. This signal is active low. It allows to detect the parity error.
95	O	CNVALE	This signal is to latch the dummy address of 2nd byte transfer in 16/8 bit conversion. This signal is active high.
96	O	DEC16M	This signal becomes high while the CPU word access to the memory.

DMA Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
97	O	ROMCS	BIOS ROM chip select signal. This signal is active low. The decode ranges of the address are: 0E0000h -- 0FFFFFh FE0000h -- FFFFFFh
98	O	LATA0	System address inverted signal in CPU cycle. When This signal is high (SA0 is low), low data bus enable signal is generated.
99	I	BHE	High data bus enable signal. When this signal is low, high bank of data bus is accessed.
100		Vcc	+5v

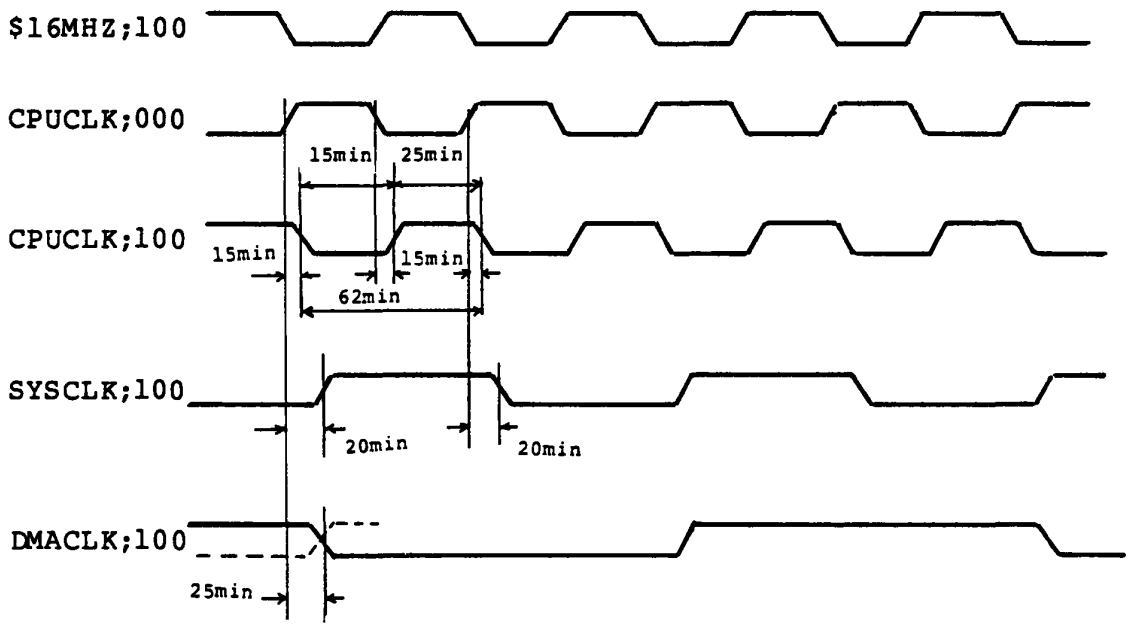
1. Clock Generater

This circuitry is to generate following clocks.
The original clock signal is a 16 MHz clock which is generated from dividing 32 MHz by 2.

	fast	slow
CPU clock :	16 MHz	8 MHz
System clock :	8 MHz	4 MHz
DMA clock :	4 MHz	2 MHz

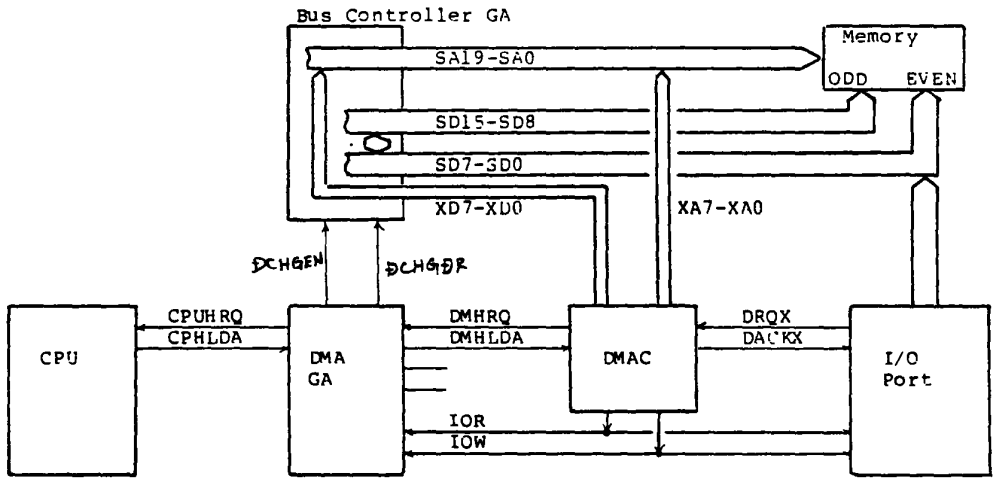
Figure C-2 Clock Generater

Followings are timing chart of the clocks.



2. DMA Control

Figure C-3 DMA Controller



This circuitry controls DMA operation.
The DMA GA receives DMHRQ signal from the DMAC, then the GA responds to the CPU with CPUHRQ signal.
After receiving CPHLDA signal from the CPU, the GA responds to the DMAC with the DMHLDA signal.
The DMAC starts DMA operation when it receives the DMHLDA.
The DMAC prepare the DMA address on the system address bus and IOR/IOW signal to the DMA GA for the bus control. If the I/O port is byte oriented device, the Bus Controller GA is used for data bus switching (low bank to high bank or high bank to low bank).

APPENDIX D

I/O Controller GA (Gate Array)

The I/O Controller Gate Array is a x,xxx gate flat package type with 100 lead chip.
The I/O Controller Gate Array has following functions.

- o FDD control.
- o Printer control.

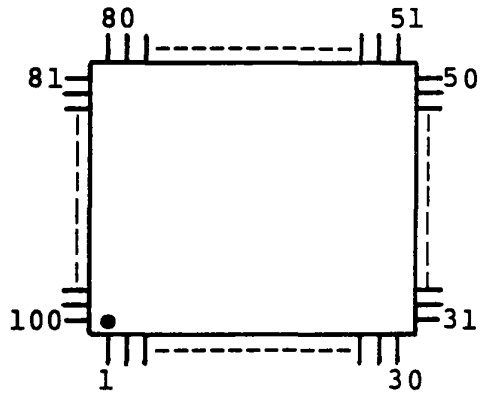
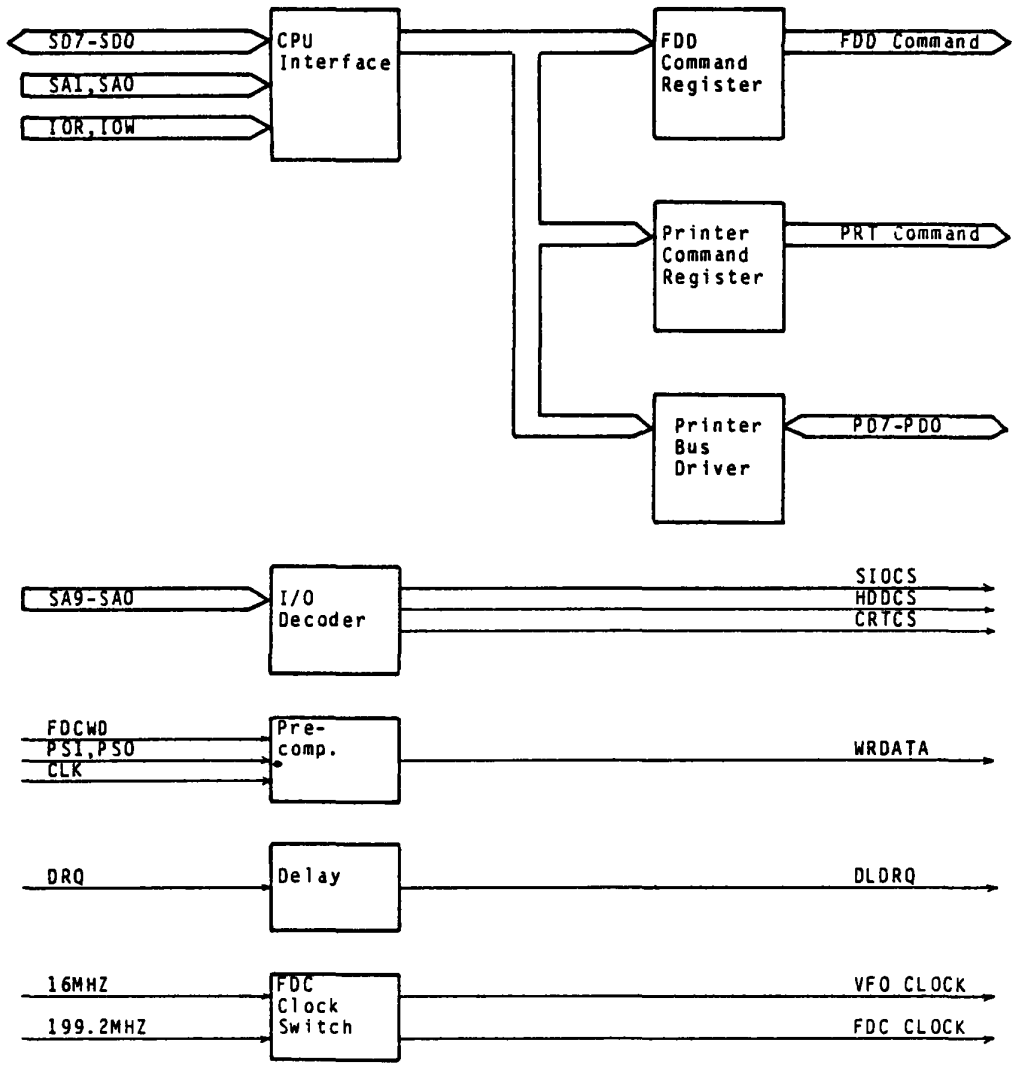


Figure D-1 I/O Controller GA



I/O Controller GA Interface Signal

Pin	I/O	Signal Name	Description
1	I/O	SD0	SD7-SD0 is system data bus. For printer control, This signal is used. - to output print data. - to read printer status. - to decode printer command. For FDD control, it is used; - to decode FDD control command. System data bus bit 0.
2	I/O	SD1	System data bus bit 1.
3		VCC	+5v
4	I/O	SD2	System data bus bit 2.
5	I/O	SD3	System data bus bit 3.
6	I/O	SD4	System data bus bit 4.
7	I/O	SD5	System data bus bit 5.
8	I/O	SD6	System data bus bit 6.
9	I/O	SD7	System data bus bit 7.
10	O	CRTCS	I/O port select signal to the color graphics controller. This signal is active (low) when the I/O port address is 3D*h.
11	I	SA2	SA9-SA0 is system address. They are used to decode the I/O port address. Printer/FDD/Color Graphics port/ HDD port/RS232C System address line bit 2.
12	I	SA3	System address line bit 3.
13	I	SA4	System address line bit 4.
14	I	SA5	System address line bit 5.
15		GND	Ground
16	I	SA6	System address line bit 6.
17	I	SA7	System address line bit 7.
18	I	SA8	System address line bit 8.
19	I	SA9	System address line bit 9.
20	I	SA1	System address line bit 1.
21	I	RDS00	Write precompensation control This signal is fixed to low in T3100.
22	O	DRQ2	DMA cycle request signal from the FDC. This signal is active high.
23	I	TC	This signal is a terminal count signal which indicates the end of DMA data transfer. This signal is active high. It comes from the DMAC (U8237).

I/O Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
24	O	FDAKTC	Terminal count signal to the FDC. This signal is active high. It is is generated from the TC signal.
25	O	FDACK	DMA acknowledge signal to the FDC. This signal is active low.
26	I	DRQFDC	DMA cycle request signal from the FDC. This signal generates DRQ2 and it is sent to the DMAC. This signal is active high.
27	I	PDS01	Write precompensation ON/OFF signal. This signal is fixed to high in T3100.
28		Vcc	+5v
29	O	IRQ6	Interrupt request signal which the FDC outputs at the end of command execution. This signal is active high. This signal goes to the input gate of the U8259A.
30	I	DMACK	This signal inhibits to output the I/O port address while DMA operation. When this signal is low, it enables to decode the address. When this signal is high, it disables to decode the address.
31	I	DACK2	This is acknowledge signal to DRQ2 which is DMA data transfer request signal. This signal is active low.
32	I	EXTFDD	This signal is to switch the printer port connector to the external FDD. When this signal is low, the connector is for printer port. When this signal is high, the connector is for FDD port.
33	I	$16MHZ	Basic clock to the FDC and VFO. 16 MHz (cycle time is 62.5 ns)
34	I	$19MHZ	Basic clock to the FDC and VFO. 19.2 MHz (cycle time is 52.08 ns)
35	O	$CKFDC	FDC clock. The frequency of the clock is depend on the rate of data transfer speed. 250 Kbps; 8 MHz, 16 MHz 300 Kbps; 4.8 MHz, 19.2 MHz 500 Kbps; 4 MHz, 16 MHz
36	O	$HIFRQ	VFO clock. The frequency of the clock is depend on the rate of data transfer speed. 250 Kbps; 8 MHz 300 Kbps; 9.6 MHz 500 Kbps; 8 MHz
37	O	WINDOW	Window signal. This signal is active high.

I/O Controller GA Interface Signal (continued)

<table>
<tr><th>Pin</th><th>I/O</th><th>Signal Name</th><th>Description</th></tr>
<tr><td>38</td><td>O</td><td>WCLK</td><td>FDD data write clock to the FDC.
The cycle time of this signal is one eighth of CKFDC.</td></tr>
<tr><td>39</td><td>O</td><td>FDCCS</td><td>Chip select signal to the FDC (U765).
This signal is active (low) when the I/O port address is 3F4h/3F5h.</td></tr>
<tr><td>40</td><td></td><td>GND</td><td>Ground</td></tr>
<tr><td>41</td><td>I</td><td>IOR</td><td>I/O read command.
This signal is active low.</td></tr>
<tr><td>42</td><td>I</td><td>IOW</td><td>I/O write command.
This signal is active low.</td></tr>
<tr><td>43</td><td>O</td><td>FDCRST</td><td>FDC reset command. This signal is active high. This signal is issued by the command to 3F2h(data is D2).</td></tr>
<tr><td>44</td><td>I</td><td>FDCWD</td><td>Write data from the FDC.
This signal is active high.</td></tr>
<tr><td>45</td><td>I</td><td>FDCINT</td><td>Interrupt signal from the FDC.
This signal is active high. This signal generates IRQ6 signal.</td></tr>
<tr><td>46</td><td>O</td><td>XF7RD</td><td>This signal is to read the status of FDD disk change. This signal is active (low) when read address is 3F7h.</td></tr>
<tr><td>47</td><td>I</td><td>PS1</td><td>PS1 and PS0 are precompensation control signals. These signals are output from the FDC.
<table>
<tr><th>PS0</th><th>PS1</th><th>Time</th></tr>
<tr><td>Low</td><td>Low</td><td>No delay</td></tr>
<tr><td>Low</td><td>High</td><td>225-250 ns delay</td></tr>
<tr><td>High</td><td>Low</td><td>225-250 ns early</td></tr>
</table></td></tr>
<tr><td>48</td><td>I</td><td>PS0</td><td>Precompensation control signal.</td></tr>
<tr><td>49</td><td>I</td><td>SYNC</td><td>This signal is to control the VFO operation mode. When this signal is low, it inhibits to read. When this signal is high, it allows to read.</td></tr>
<tr><td>50</td><td>I</td><td>FDCWE</td><td>Data write enable signal to the FDD.
This signal is active high.</td></tr>
<tr><td>51</td><td>O</td><td>IRQEN</td><td>Printer interrupt enable signal.
This signal is active low. This signal is issued by the command to 372h.</td></tr>
<tr><td>52</td><td>O</td><td>CCMICS</td><td>RS232C (Primary) select signal.
This signal is active (low) when the I/O port address is 3F8h-3ffh.</td></tr>
<tr><td>53</td><td></td><td>Vcc</td><td>+5v</td></tr>
</table>

I/O Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
54	O	SWMONA	FDD motor on signal to the 1st FDD. This signal is active high. ON/OFF is controlled by the command to 3F2h.
55	O	SWMONB	FDD motor on signal to the 2nd FDD. This signal is active high. ON/OFF is controlled by the command to 3F2h.
56	O	INDRVB	Internal FDD (2nd FDD) select signal. This signal is active high.
57	O	SWFDA	Internal FDD (1st FDD) select signal. This signal is active high.
58	O	XRATE0	This signal defines the rate of FDD data transfer speed. When this signal is low: 500 Kbps - 250 Kbps When this signal is high: 300 Kbps This signal is issued by the command to to 3F7h.
59	I	SELECT	Printer select command. This signal is active low. It can be read from address 3F7h. This signal becomes write gate signal when it is external FDD mode.
60	I	BUSY	Printer busy status. This signal is active high. It can be read from address 371h. This signal becomes motor ON/OFF signal when it is external FDD mode.
61	O	CBDIR	Read enable signal to the I/O peripheral which is connected to external bus. T3100 has not such bus.
62	I	STROBE	Printer strobe signal. This signal is active high. It can be read from address 371h.
63	I	AUTFD	Printer auto-feed command. This signal is active high. It can be read from address 371h. This signal becomes low density signal when it is in external FDD mode.
64	I	PDS10	FDD precompensation ON/OFF signal. This signal is not used in T3100.
65		GND	Ground
66	O	CCM2CS	RS232C (Secondary) select signal. This signal is active (low) when the I/O port address is 2F7h-2FFh.

I/O Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
67	I	PE	Paper end status from the printer. This signal is active high. It can be read from address 371h. This signal becomes write data signal when it is external FDD mode.
68	I	PINIT	Printer initial command. This signal is active high. It can be read from the address 372h. This signal becomes direction signal when it is in external FDD mode.
69	I	SLIN	Printer select command. This signal is active high. It can be read from address 372h. This signal becomes step signal when it is in external FDD mode.
70	I	ACK	Printer ACK status. This signal is active high. It can be read from address 371h. Select signal is input when it is in external FDD mode.
71	I	ERROR	Printer error status. This signal is active high. It can be read from address 371h. This signal becomes SIDE signal when it is external FDD mode.
72	O	EXFDWE	Write gate signal in external FDD mode. This signal is active high.
73	O	SWFDB	System FDD (2nd FDD) select signal. This signal is active high.
74	O	DTAREA	Read control signal to the VFO. When this signal is low, it inhibits to read. When this signal is high, it allows to read.
75	O	EN96M	This signal is to change the value of register in the VFO circuit when the rate of data transfer speed is 300 Kbps. This signal is active high.
76	O	WN	Window signal from the VFO. This signal is active high.
77	O	MINI	This signal defines the type of the format on disk. When this signal is low: 9 sectors/track. When this signal is high: 15 sectors/track.
78		Vcc	+5v

I/O Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
79	O	WRDATA	Write data to the FDC. This signal is active high. The precompensation is given to this write data.
80	O	HDDCS	Select signal to the external HDC. This signal is active (low) when the I/O address is 170h-177h.
81	O	PRTDIR	This signal controls the direction of printer data port. When this signal is low: External → Internal. When this signal is high: Internal → External. The above function is neglected when it is in external FDD mode.
82	I/O	PD7	PD7-PD0 is an printer or parallel data IN bus. When it is in external FDD mode, they are high impedance. When printer is connected, they are output mode. Printer data bus bit 7.
83	I/O	PD6	Printer data bus bit 6.
84	I/O	PD5	Printer data bus bit 5.
85	I/O	PD4	Printer data bus bit 4.
86	I/O	PD3	Printer data bus bit 3.
87	I/O	PD2	Printer data bus bit 2.
88	I/O	PD1	Printer data bus bit 1.
89	I/O	PD0	Printer data bus bit 0.
90		GND	Ground
91	O	SLCTIN	Printer select command. This signal is active high. This signal issued by the command to address 372h.
92	O	AUTFD	Printer auto-feed command. This signal is active high. This signal is issued by the command to address 372h.
93	O	INIT	Printer initial command. This signal is active high. This signal is issued by the command to address 372h.
94	O	STROBE	Printer strobe command. This signal is active high. This signal is issued by the command to address 372h.
95	I	DIREN	This signal is to control the direction of the printer data bus. When this signal is low, it is parallel in mode. When this signal is high, it is printer output mode.

I/O Controller GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
96	O	FDSLEN	This signal is to read the FDD interface signal when it is in external FDD mode. This signal is active low. INDEX/TRACK 0/WRITE PROTECT/ READ DATA/DISK CHANGE/READY
97	I	SA0	Address line. This signal is used to generates printer/FDD command.
98	I	RST	Initial reset signal. This signal is active low. Internal counters and F/Fs are reset by this signal.
99	I	FSELSW	This signal is to change the drive number of internal FDD. When this signal is low, the drive number is changed to B. When this signal is high, the drive number is changed to A (Normal).
100		GND	Ground

APPENDIX E

Display Controller GA (Gate Array)

The Display Controller Gate Array is a 5,000 gates, CMOS, 100-pin flat package type chip.
It contains Color Graphics Adaptor which is able to control external CRT disply as well as internal plasma display.
The Display Controller Subsystem can control following three types of displays.
The signal name and it's meaning of each pin are described in this section.

A). 640 x 400 dot Plasma Display.
B). 640 x 200 dot LCD (Liquid Crystal Display).
C). 640 x 200 dot CRT (Cathode Ray Tube) Display.

Note: External CRT display unit and internal plasma display unit could not display a screen at same time.
You can select current display unit from them by keyboard operation.

Ctrl + Alt + Home ---- Internal display unit is selected.
Ctrl + Alt + End ---- External display unit is selected.

The Display Controller GA is composed of following functions.

1) Plasma/LCD/CRT control function.
   This function is compatible with the MC6845 (CRTC) on software operation.
2) Attribute handling function.
3) Interface to CPU (I/O bus).
4) Interface to V-RAM, CG-ROM (Character Generator ROM).

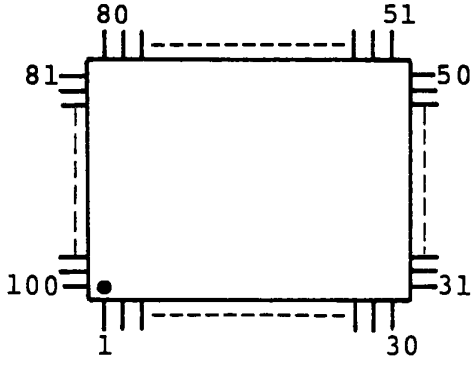
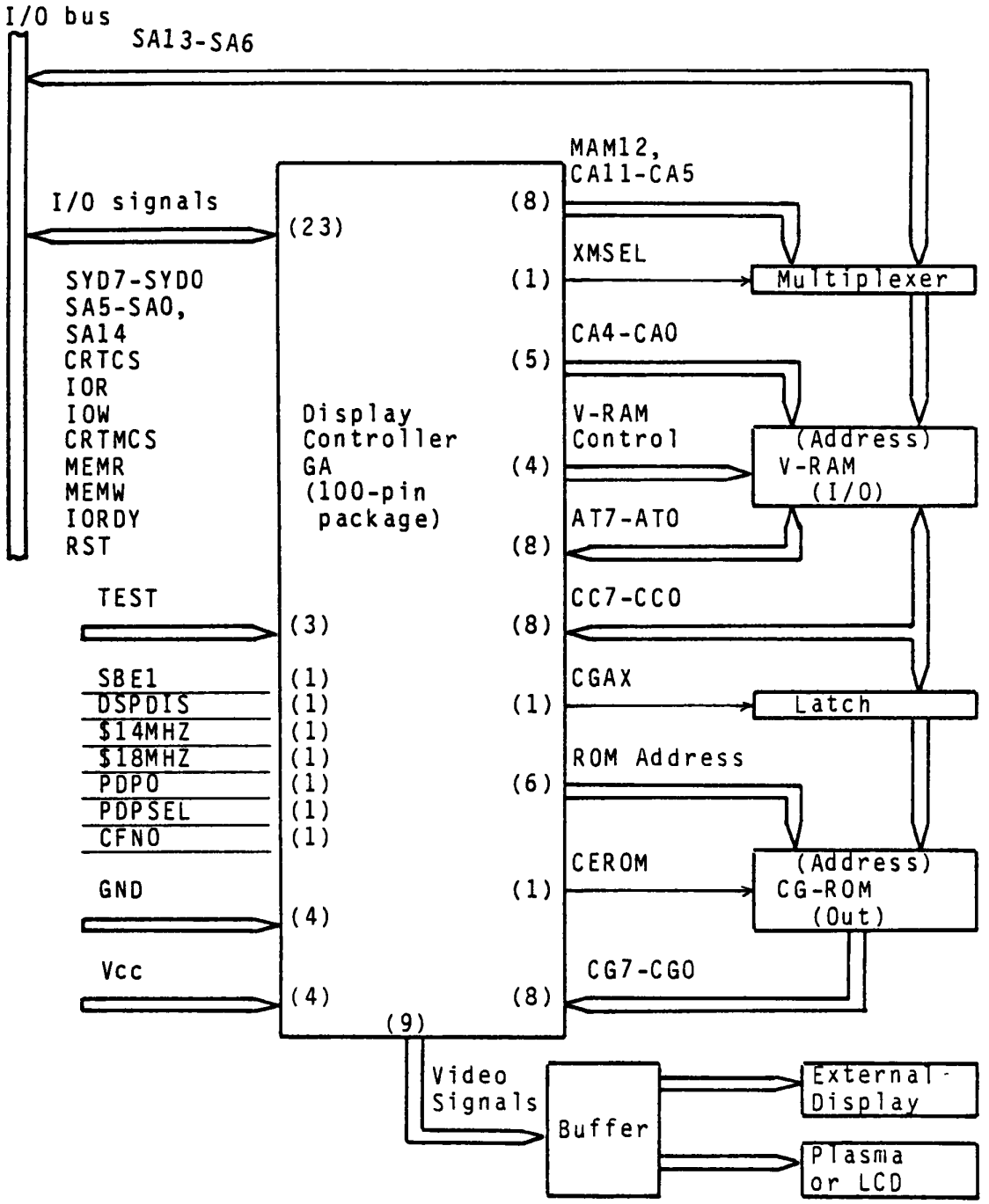


Figure E-1 Display Controller Subsystem (DCS)



Interface Signal

Pin	I/O	Signal Name	Description
1	I	CG3	Character generator output signal bit 3.
2	I	CG4	Character generator output signal bit 4.
3	I	VCC	+5V
4	I	CG5	Character generator output signal bit 5.
5	I	CG6	Character generator output signal bit 6.
6	I	CG7	Character generator output signal bit 7.
7	O	CEROM	Chip enable signal to CG-ROM (Character Generator - ROM).
8	I	CG2	Character generator output signal bit 2.
9	I	CG1	Character generator output signal bit 1.
10	I	CG0	Character generator output signal bit 0.
11	O	RA0	Raster scan address bit 0.
12	O	RA1	Raster scan address bit 1.
13	O	RA2	Raster scan address bit 2.
14	O	RA3	Raster scan address bit 3.
15		GND	Ground
16	I	SBE1	Reserved for LCD.(Ground)
17	O	INTE	Single dot select signal. (single dot/double dots character)
18	O	CGM0	Plasma font select signal. (8x8/8x16)
19	O	CGAX	CG address latch.
20	O	XMSEL	Refresh address select signal.
21	O	MAM12	Refresh address bit 12.
22	O	CA11	Refresh address bit 11.
23	O	CA10	Refresh address bit 10.
24	O	CA9	Refresh address bit 09.
25	O	CA8	Refresh address bit 08.
26	O	CA7	Refresh address bit 07.
27	O	CA6	Refresh address bit 06.
28	I	VCC	+5V
29	O	CA5	Refresh address bit 05.
30	I	$14MHZ	Clock 14.31818 MHz for the video signal of CRT display.
31	I	CRTCS	Display I/O select signal. This is access signal to the I/O port of the GA.
32	I	CRTMCS	V-RAM access signal from CPU or DMAC.
33	I/O	SYD7	Data bus bit 7.
34	I/O	SYD6	Data bus bit 6.
35	I/O	SYD5	Data bus bit 5.
36	I/O	SYD4	Data bus bit 4.
37	I/O	SYD3	Data bus bit 3.
38	I/O	SYD2	Data bus bit 2.
39	I/O	SYD1	Data bus bit 1.

Interface Signal (Continued)

Pin	I/O	Signal Name	Description
40		GND	Ground.
41	I/O	SYD0	Data bus signal bit 0.
42	O	IORDY	I/O ready signal.
43	I	RST	GA reset signal.
44	I	SA5	CPU address bit 5.
45	I	SA4	CPU address bit 4.
46	I	SA3	CPU address bit 3.
47	I	SA2	CPU address bit 2.
48	I	SA1	CPU address bit 1.
49	I	SA14	CPU address bit 14.
50	I	MEMW	Memory write signal. (for V-RAM write)
51	I	MEMR	Memory read signal. (for V-RAM read)
52	I	IOR	I/O read signal. This signal reads out I/O port data to the data bus SYD71-SYD01.
53	I	VCC	+5v
54	I	IOW	I/O write signal. This signal writes data on the data bus to the I/O port.
55	I	SA0	CPU address bit 0.
56	I	PDP0	Plasma display panel select signal.
57	I	DSPDIS	GA off. If this signal is high, the GA becomes to be disable.
58		TSTB	Ground
59		TST0	Ground
60		TST1	Ground
61	O	BFR0	Video signal.
62	O	FRHV	Vertical sync signal for composite CRT display.
63	O	WSYNC	Vertical sync signal for plasma/Color CRT display.
64	O	SCK	Video signal.
65	O	GND	Ground.
66	O	HSYNC	Horizontal sync signal for plasma/Color CRT display.
67	O	DRPD1	Red signal for Color CRT display.
68	O	DGPD2	Green signal for Color CRT display.
69	O	DBPD3	Blue signal for Color CRT display. .
70	O	DIPD4	Intensity signal
71	I	FONT	Character font change signal.
72	I	PDPSEL	Flat display select signal. This signal changes internal/external display.
73	I	$18MHZ	Clock 17.5 MHz.
74	O	CEH	Chip enable high. Chip select signal for the V-RAM (BC000-BFFF).

Interface Signal (Continued)

Pin	I/O	Signal Name	Description
75	O	WRCC	Character code write signal. This signal is used with chip enable signal to write the V-RAM (even).
76	O	WRAT	Attribute code write signal. This signal is used with chip enable signal to write the V-RAM (odd).
77	O	CEL	Chip enable low. This signal is V-RAM select signal.
78		Vcc	+5v
79	O	CA0	CPU/Refresh address bit 0.
80	O	CA1	CPU/Refresh address bit 1.
81	O	CA2	CPU/Refresh address bit 2.
82	O	CA3	CPU/Refresh address bit 3.
83	O	CA4	CPU/Refresh address bit 4.
84	I/O	AT0	Attribute data bit 0.
85	I/O	AT1	Attribute data bit 1.
86	I/O	AT2	Attribute data bit 2.
87	I/O	AT3	Attribute data bit 3
88	I/O	AT4	Attribute data bit 4.
89	I/O	AT5	Attribute data bit 5.
90	I/O	GND	Ground
91	I/O	AT6	Attribute data bit 6.
92	I/O	AT7	Attribute data bit 7.
93	I/O	CC0	Character code data bit 0.
94	I/O	CC1	Character code data bit 1.
95	I/O	CC2	Character code data bit 2.
96	I/O	CC3	Character code data bit 3.
97	I/O	CC4	Character code data bit 4.
98	I/O	CC5	Character code data bit 5.
99	I/O	CC6	Character code data bit 6.
100	I/O	CC7	Character code data bit 7.

Display Controller Subsystem

Display Controller Subsystem (DCS) is composed of following components.

Table E-1

Display Controller GA		CMOS 6 KG 100-pin flat Package
Video-RAM		32 KB 64 KBSRAMx4
CG-ROM		32 KB 256 KB ROMx1
OSC	CPU-CLK	14.31818 MHz
	Other	17.5 MHz
Others	Multiplexer Latch Display Buffer	74HC157x2 74HC273x1

Table E-2 is the operation mode of the DCS of internal plasma display and external CRT display.

Table E-2

Operation Mode		Plasma (Pixels)		External CRT(Pixels)	
		Resolution	Character Box	Resolusion	Character Box
40x25	TEXT	320x400	8x16	320x200	8x8
80x25	TEXT	640x400	8x16	640x200	8x8
320x200	GRAPH	320x200	8x8	320x200	8x8
640x200	GRAPH	640x200	8x8	640x200	8x8
40x50	TEXT	320x400	8x8	not supported	
80x50	TEXT	640x400	8x8	not supported	
640x400	GRAPH	640x400	8x16	not supported	

Signals

The DCS has follwing groups of signals.

- o I/O Interface Signals (23 lines)
- o V-RAM Signals (34 lines)
- o Character Generator (CG) Signals (16 lines)
- o Video Signals (9 lines)
- o Display Mode Select Signals (3 lines)
- o Clock Input (2 lines)
- o Miscellaneous Signals (5 lines)

1) I/O Interface Signals (23 lines)

CRTCS : Display I/O Select (Input)
This signal allows the CPU to read or write I/O port within the GA when this signal is low.
IOR or IOW should be low as well as CRTCS for read or write operation to I/O port within the GA.

IOR : I/O Read (Input)
I/O port data within the GA is transferred to the CPU through the SYD7-SYD0 when this signal is low and CRTCS is low too.

IOW : I/O Write (Input)
Data from the CPU is transferred and writed to the selected I/O port within the GA through the SYD7-SYD0 when this signal is low and CRTCS is low too.

CRTMCS : Display Memory Selected (Input)
This signal allows the CPU to read or write the DMAC or Video RAM when this signal is low.
MEMR or MEMW should be low as well as CRTMCS for read or write operation to V-RAM.

MEMR : Memory Read (Input)
Read operation to the V-RAM is executed and read data is transferred to the SYD7-SYD0 when this signal is low and CRTMCS is low too.

MEMW : Memory Write (Input)
Data from the SYD7-SYD0 is written to the V-RAM when this signal is low and CRTMCS is low too.

SA5-SA0,SA14 : CPU Address (Input)
These are address data lines from the CPU or DMAC and high level is logical true.
SA3-SA0 are used for selecting one of I/O ports within the GA during read or write operation to the I/O port within the GA.
For memory read or memory write operation to the V-RAM, SA5-SA0 and SA14 go through the GA then they are used to selecting memory location of the V-RAM with SA13-SA6.

SYD7-SYD0 : 8-bit Data Bus (Input/Output)
These are 8-bit data lines and high level is logical true.
The data goes through these lines while read/write operation to the I/O port within the GA or read/write operation to the V-RAM.

IORDY : I/O Ready (Output)
It is ready when this line is high level. If CRTMCS is low (the CPU or DMAC requests V-RAM access), the GA holds this line low level to make the CPU or DMAC to waite until the end of the access. This signal line is held high level usually and it is also high when the CPU reads or writes the I/O port within the GA.

RST : Reset (Input)
The GA is reset when this signal line is low level.

2) V-RAM Signals (34 lines)

CA4-CA0 : CPU/Refresh Address 4 - 0 (Output)
These lines are used to send a part of CPU address and a part of refresh address to the V-RAM.
The CPU address comes from CPU address lines SA5-SA1.

MAM12,CA11-CA5 : Refresh Address 12 - 5 (Output)
These lines are address lines for the V-RAM refresh.
MAM12,CA11-CA5 as high-order bits of address lines are input to the D-RAM through the multiplexer which has another input of I/O bus address (SA13-SA6), while CA4-CA0 are directly connected input pins of the V-RAM. (see Fig. E-1)
There are two ways to read or write the V-RAM. One way is that the CPU reads or writes the D-RAM through the I/O bus. The other is Display refresh (read only) by the GA.
The addressing of the each case is shown on the Table E-3.

CEL,CEH : Chip Enable Low/High (Output)
These signals are chip-enable signals of the V-RAM, and they are active when low. The block diagram of the V-RAM control signals and logical operation of the signals are shown respecively on the Fig. E-2 and Table E-4. The V-RAM is composed of four 8KB*8bit SRAM (TC565). CEL address 16KB of two S-RAMs starting from B8000h, and CEH0 addresses 16KB of two S-RAMs starting from BC000h respectively.
The RAMs connected to the data bus of CC7-CC0 are assigned to even address and the RAMs connected to the data bus of AT7-AT0 are assigned to odd address respectively. For V-RAM refresh, two byte read operation is done always. It makes two RAM chips (two bytes) enable to read but only one of two bytes are put on the data lines (SYD7-SYD0) of the I/O bus when the CPU or DMAC reads the V-RAM. CC7-CC0 are read out to the I/O bus SYD7-SYD0 if SA0 is low, and AT7-AT0 are read out to the I/O bus SYD7-SYD0 if SA0 is high. Two RAMs (CC7-CC0 and AT7-AT0) become to be enabled but only one RAM is written when the CPU or DMAC executes write operation.

WRCC : Write Character Code (Output)
WRAT : Write Attribute Data (Output)
They are write enable signal to the V-RAM.
It selects the RAM chip which chip enable signal and one of WRCC/WRAT is low for write operation to the RAM. The write operation to the V-RAM is executed only when the CPU or DMAC request to write (CRTMCS=low and MEMW=low). At this point, one of WRCC and WRAT becomes low according to the SA0 state. WRCC becomes low when SA0 is low, and write data on the I/O bus SYD7-SYD0 is transferred to CC7-CC0. WRAT becomes low when SA0 is high, and write data on the I/O bus SYD7-SYD0 is transferred to AT7-AT0.

Table E-3

V-RAM		CPU Address	Memory Refresh	
Pin Name	Signal Name		TEXT Mode	GRAPH Mode
$\overline{CE}$	CEH0/CEL0	SA14	MA13	RA1
AD12	MAM12	SA13	MA12	RA0
AD11	CA11	SA12	MA11	MA11
AD10	CA10	SA11	MA10	MA10
AD09	CA9	SA10	MA09	MA09
AD08	CA8	SA9	MA08	MA08
AD07	CA7	SA8	MA07	MA07
AD06	CA6	SA7	MA06	MA06
AD05	CA5	SA6	MA05	MA05
AD04	CA4	SA5	MA04	MA04
AD03	CA3	SA4	MA03	MA03
AD02	CA2	SA3	MA02	MA02
AD01	CA1	SA2	MA01	MA01
AD00	CA0	SA1	MA00	MA00
$\overline{WE}$	WRCC/WRAT	SA0	--	--

Note:

* SA14-SA0 are I/O bus address lines from the CPU.
  SA5-SA0 and SA14 are input to CPU address input gates of the GA.

* MA13-MA00 are Refresh Memory Address.
  They are generated by the 6845 compatible circuit within the GA.

* RA1-RA0 are Raster Scan Address.
  There are four Raster Scan Address lines ((RA3(MSB) - RA0(LSB)), but only two lower-bits are used in graphics mode.

Figure E-2 V-RAM Control Signals

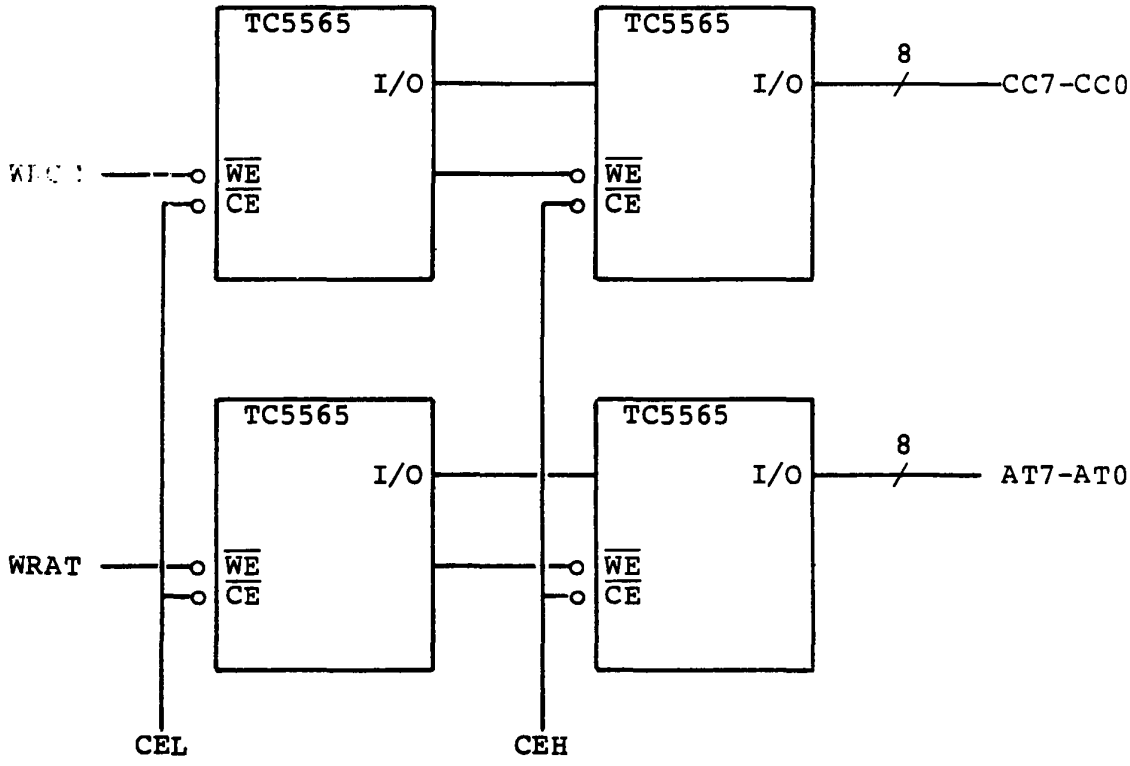


Table E-4 V-RAM Control Signals

V-RAM Control Signal	CPU Address		Display Refresh
	Read	Write	
CEL	if SA14=low, Low	if SA14=low, Low	if MA13 or RA1 =Low, Low
CEH	if SA14=high, Low	if SA14=high, Low	if MA13 or RA1 =High, Low
WRCC	High	if SA0=Low, Low	High
WRAT	High	if SA0=High, Low	High

XMSEL : Refresh Address Select (Output)
This signal is an input select signal to the V-RAM address multiplexer. If this signal is low, the display refresh address lines (MAM12,CA11-CA5) are selected as V-RAM address. If it is high, the I/O bus address lines are selected as V-RAM address.

CC7-CC0 : Character Code Data Bus (Input/Output)
These lines are data bus from/to the even address V-RAM. The even address V-RAM is used to store the character codes in TEXT mode.

AT7-AT0 : Attribute Data Bus (Input/Output)
These lines are data bus from/to the odd address V-RAM. The even address V-RAM is used to store the attribute codes in TEXT mode.

3) Character Generator (CG) Signals (16 lines)

CGAX : CG Address Latch (Output)
The character code from the V-RAM (CC7-CC0) is set to the external latch circuit by this signal. The set timing of the external latch circuit is at the rising edge of this signal. The output from the external latch circuit is used for the address of CG-ROM. The character code is 8-bit code, and it can selects one of 256 characters.

ROM Address (Output)
Following 6 signals are also used as CG-ROM address as well as the character code mentioned above.

CGM0 : Plasma Font Select.
INTE : Single Dot Font Select.
RSA3-RSA0 : Raster Scan Address.

Table E-5 and Fig. E-3 shows ROM address assignment.
CG-ROM (32 KB) has following character fonts.

8x8 single dot character set
8x8 double dot character set
8x16 single dot character set
8x16 double dot character set

The plasma display can not display intensified character like CRT display, thus double dot character is used for distinction between normal character and intensified character.
INTEN1 signal is used to select single or double dot character.
INTE=Low --- Single dot character select.
INTE=High -- Double dot character select.

CGM0 signal is used to select 8x16 or 8x8 character font.
CGM0=Low --- 8x16 character select.
CGM0=High -- 8x8 character select.

RA21-RA01 and RA31 are Raster Scan Address. The RA0 is the Least Significant Bit (LSB).

CEROM : Chip Enable for ROM (Output)
This signal enables to access the CG-ROM.

CG7-CG0 : Character Generator Output Signals (Input)
These lines are output signals of the CG-ROM.
The data addressed by ROM address is read out to the CG7-CG0 lines, when CEROM=0.

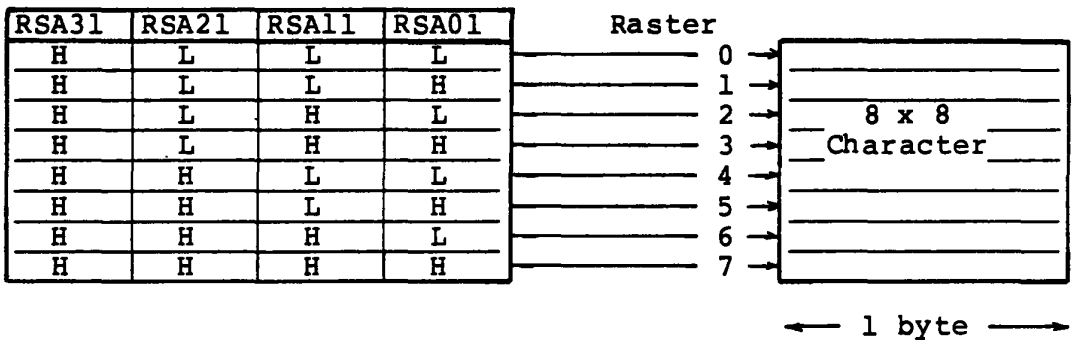


Figure E-3 ROM Address Assignment

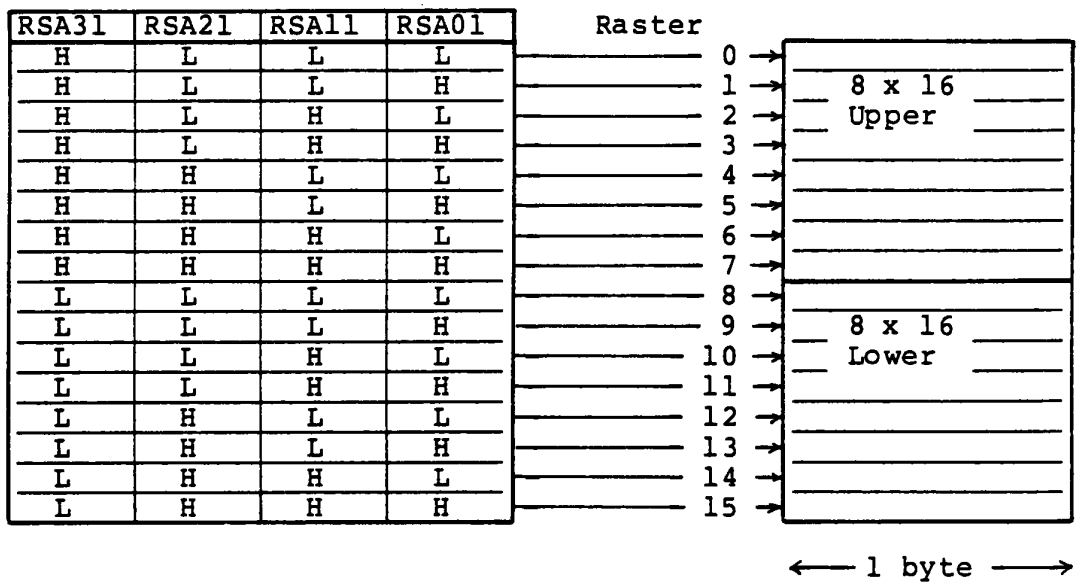


Table E-5 ROM Address Assignment

ROM Add.Pin	GA Signal
AD14	+VCC
AD13	CGM01
AD12	RSA31
AD11	INTEN1
AD10	CC71
AD09	CC61
AD08	CC51
AD07	CC41
AD06	CC31
AD05	CC21
AD04	CC11
AD03	CC01
AD02	RSA21
AD01	RSA11
AD00	RSA01

32 KB - ROM

4000h	8x16 Single Dot Lower Half
4800h	8x16 Double Dot Lower Half
5000h	8x16 Single Dot Upper Half
5800h	8x16 Double Dot Upper Half
6000h	———
6800h	———
7000h	8x8 Single Dot
7800h	8x8 Double Dot
7FFFh	

Note: Addresses 0h-3FFFh of CG-ROM are not used.

4) Video Signals (9 lines)

There are 9 video signals which are output from the GA. They are sent to the plasma display or external CRT display. The signals are used in the each unit as shown Table E-6.

Table E-6 Video Signals

GA Signal	Plasma Display	CRT Display
HSYNC	PHSY0	CHSY1
WSYNC	PVSY0	CVSY1
DRPD1	PD10	CRV1
DGPD2	PD20	CGV1
DBPD3	PD30	CBV1
DIPD4	PD40	CIV1
SCK	PSCK0	

5) Display Mode Selection Signals (3 lines)

FONT : Character Font Change (Input)
This signal is to change the font desplayed on the screen.
The function of this signal is shown on the Table E-7.

PDPSEL : Flat Display Selected (Input)
This signal is to select one of internal and external display unit.
If this signal is high level, the internal plasma display is selected.
If this signal is low level, the external CRT display (RGB, Composite) is selected.

PDP0 : Plasma Display Panel (Input)
This signal is to specify the type of internal display unit.
If this signal is high level, a plasma display unit (640x400 pixels) is used as internal display unit.
If this signal is low level, a LCD display unit (640x200 pixels) is used as internal display unit.

Note: Relation between signals of FONT,PDPSEL,PDP0 and character fonts on the screen are shown on the Table E-7.

Table E-7

Mode	Attribute Bit	GA Input			GA Output		Selected Display	Selected Display
		FONT	PDPSEL	PDP0	INTE	CGM0	Display	Display
80x25 or 40x25	0	H	H	H	H	H	LCD	8x8 Double
	1	H	H	H	L	H	LCD	8x8 Single
	0	L	H	H	L	H	LCD	8x8 Single
	1	L	H	H	H	H	LCD	8x8 Double
80x25 or 40x25	0	H	H	L	L	L	Plasma	8x16 Single
	1	H	H	L	H	L	Plasma	8x16 Double
	0	L	H	L	H	L	Plasma	8x16 Double
	1	L	H	L	L	L	Plasma	8x16 Single
80x50 or 40x50	0	H	H	L	L	H	Plasma	8x8 Single
	1	H	H	L	H	H	Plasma	8x8 Double
	0	L	H	L	L	H	Plasma	8x8 Single
	1	L	H	L	H	H	Plasma	8x8 Double
80x25 or 40x25	0	H	L	x	H	H	CRT	8x8 Double
	1	H	L	x	H	H	CRT	8x8 Double (High Light)
	0	L	L	x	L	H	CRT	8x8 Single
	1	L	L	x	L	H	CRT	8x8 Single (High Light)

6) Clock Input (2 lines)

$14MHZ : Oscillator 14 MHz (Input)
This clock is the input signal to generate a video signal for the CRT display. The frequency of the clock must be 14.31818 MHz.

$18MHZ : Oscillator 18 MHz (Input)
This clock is the input signal to generate a video signal for the plasma display. The frequency of the clock must be 17.5 MHz (60 Hz).

7) Miscellaneous Signals (5 lines)

DSPDIS : GA Off (Input)
It forces the GA to be disable if this signal is high. It forces the GA to be disable when the other display adaptor is installed in the I/O expansion box and the external display adaptor is used.

SBEl : SBE-LCD (Input)
This signal is reserved for LCD display.