1.1 GENERAL

Toshiba Personal Computer T3200 (hereinafter referred to as T3200) is a portable personal computer which is compatible with IBM PC/AT situated at higher rank of portable computer than Toshiba T3100. Hardware of the T3200, a lot of IC chips are C-MOS type so that the power consumption is very little and Gate Array chips are applied so that it is very compact and light weight.

The T3200 is composed of as follows:

System PCB (Printed curcuit board)
Hard disk control PCB
3.5-inch floppy disk drive
3.5-inch hard disk drive
Plasma display
Keyboard
Power supply unit

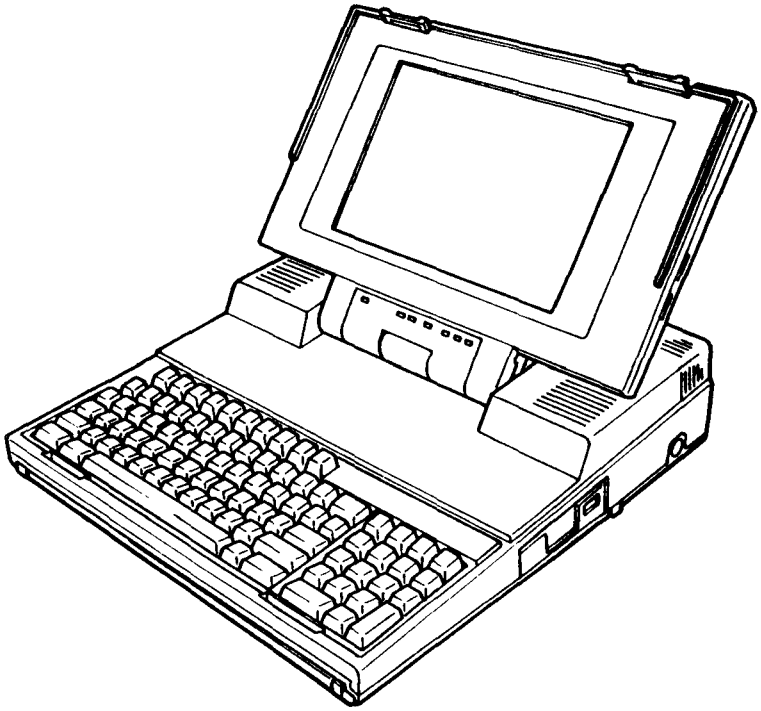


FIGURE 1-1 T3200 Personal Computer

A 3.5-inch Floppy disk drive (FDD) is double-sided, double-density, double-track with storage capacity of 720 kilobytes (formatted). A 3.5-inch hard disk drive (HDD) with storage capacity of 40 megabytes (formatted) is the second external storage device. The plasma display with pixels of 720 in columns and 400 in rows.
The keyboard has 85 keys. For most applications it can be used exactly like a standard typewriter keyboard.
The power supply unit provides +5 Vdc and ±12 Vdc power to every component in the system unit, including the option cards. For the plasma display, this unit regulates +205 Vdc power. This unit has a ventilation fan, driven by +12 Vdc. The fan enhances the reliability and durability of the T3200 system unit.

The T3200 provided connecting to the optional devices at the rear panel of the system. There are three connectors such as a parallel printer (or an external floppy disk drive), an RGB direct drive CRT display and an RS-232C device.
The connector for a parallel printer can be used to connect an external FDD unit by changing the A-B-PRT switch setting.

1.2 SYSTEM PCB

System PCB is composed of the following devices:

- Central processor: CPU (80286-12) (12 MHz/6 MHz))
- Numeric data processor: NPU (80287, optional)
- Memory

RAM	.....	1 Mbyte standard
		3 Mbytes (option card)
		--- "LIM" standard
ROM (Main BIOS)	.....	64 Kbytes (16 bits)
(AGS BIOS)	.....	32 Kbytes (8 bits)
Video RAM	.....	256 Kbytes

- System support elements
  - Direct memory access: DMA (82C37)
  - Programmable interrupt controller: PIC (82C59)
  - Programmable interval timer: PIT (82C54)
  - Real time clock: RTC (MC146818)
- Floppy disk controller: FDC (TC8565F)
- Keyboard controller: KBC (u8042) x 2
- Display controller: PEGA2, AGS G.A.
- Gate array
  - Bus driver
  - Memory mapper
  - DMA driver
  - I/O controller
  - LIM
  - AGS (Advanced graphics subsystem)

1.2.1 DIP switches

The system has DIP switches which are located at the rear panel. The following table shows function of the DIP switches.

TABLE 1-1 DIP Switch Functions

DIP Switch	Setting	Description
1	ON	Auto-Switched display mode
	OFF	IBM EGA full compatible
2	ON	PRT port used both for input and output
	OFF	PRT port only for output
3	ON	Communications port as CH2
	OFF	Communications port as CH1
4	ON	Double font in plasma for TEXT
	OFF	Single font in plasma for TEXT
5	ON	Disable CRTC for EXT.CRTC
	OFF	Enable internal CRTC (normal)
6	ON	North European Font to display
	OFF	Other Fonts (Normal)
7 to 10	(Defined as follows)	

Monitor in use	7	8	9	10
Monochrome	OFF	OFF	OFF	OFF
Standard RGB (40 column mode is default)	ON	OFF	OFF	ON
Standard RGB (80 column mode is default)	OFF	OFF	OFF	ON
Enhanced RGB (200 line or emulation of standard RGB is default)	ON	ON	ON	OFF
Enhanced RGB (350 line, true enhanced operation is default)	OFF	ON	ON	OFF

1.2.2 Jumper straps

The system has six jumper straps (PJ 2) which are located on the keyboard control PCB.
Usually the six jumper straps are all open.
The following figure shows location of the jumper straps.

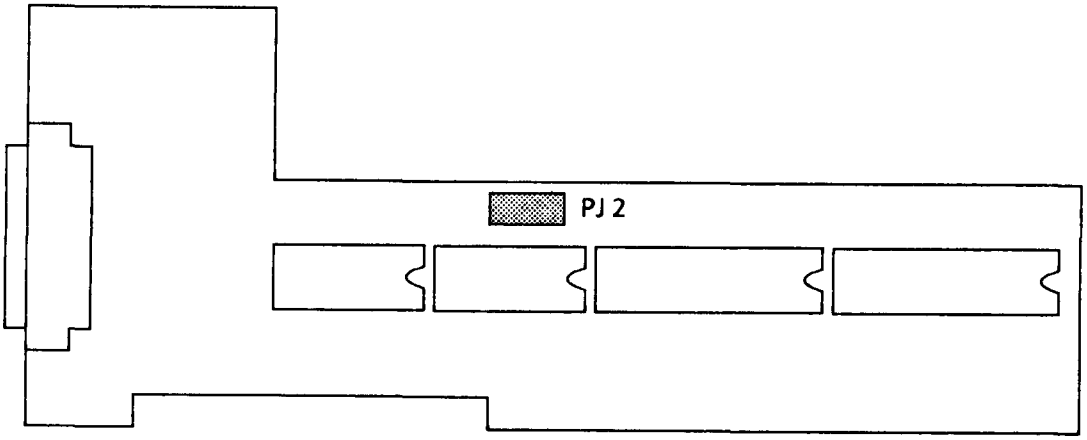


FIGURE 1-2 Jumper Strap Locations

The following table shows function of the jumper straps.

TABLE 1-2 Jumper Strap Functions

	Name	Function
1-2	Not used	
3-4	2HD FDD type	Open ... 1.6 Mbytes Short ... 2.0 Mbytes
5-6	Internal FDD numbers	Open ... One FDD Short ... Two FDD's
7-8	FDD type	Open ... 2DD Short ... 2HD (1.6 Mbytes/2.0 Mbytes)
9-10	Standard memory size	Open ... 640 kbytes Short ... 512 kbytes
11-12	Used 3MB memory card mode (Option)	Open ... Used as the extended memory and the expanded memory. Short ... Used as the only expanded memory.

1.3 3.5-INCH FLOPPY DISK DRIVE

The floppy disk drive (FDD) used in the T3200 is high performance, high reliable, slim sized FDD for 3.5-inch floppy disks with recording capacity of 720 kbytes (formatted) in double-sided, double density and 135 tracks per inch operation. The specifications are as following table.

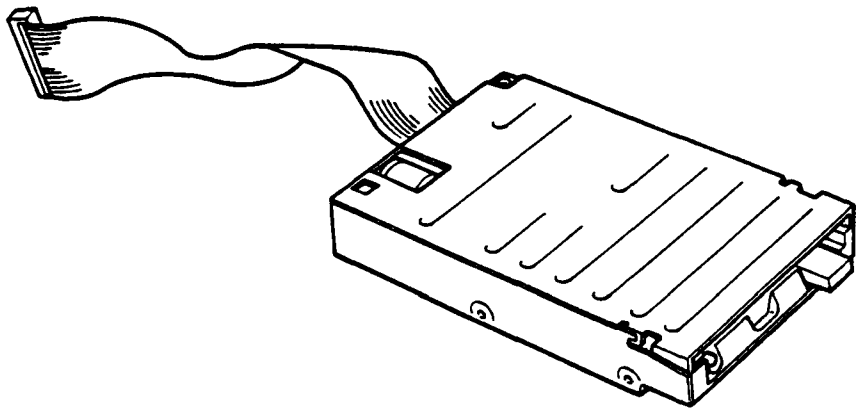


FIGURE 1-3 3.5-inch FDD

TABLE 1-3 3.5-inch Floppy Disk Drive Specifications

Item	Specifications
Storage Capacity (kilobytes)	1000 (unformatted) 720 (formatted)
Number of Heads	2
Number of Track per Side	80
Track to Track Access (milliseconds)	3
Head Settling Time (milliseconds)	15
Track Density (tracks per inch)	135
Motor Start-up Time (milliseconds)	500
Data Transfer Rate (kilobits per second)	250
Rotational Speed (revolutions per minute)	300
Recording Method	MFM (Modified frequency modulation)

1.4 3.5-INCH HARD DISK DRIVE

The hard disk drive (HDD) is random access storage, having recording capacity of 40 Mbytes (formatted). This is equipped with the storage media of non-removable 3.5-inch magnetic disks and mini-winchester type magnetic heads.
The specifications are as following table.

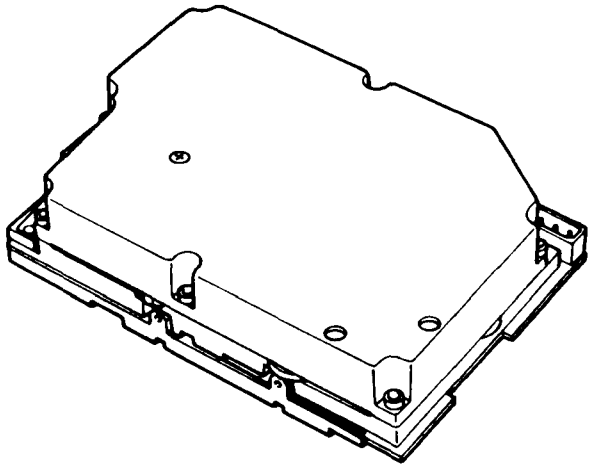


FIGURE 1-4 3.5-inch Hard Disk Drive

TABLE 1-4 3.5-inch Hard Disk Drive Specifications

Item		Specifications
Storage Capacity (megabytes)		51.24 (unformatted) 40.30 (formatted)
Number of Heads		8
Number of Cylinders		615
Number of Tracks (tracks per cylinder)		8
Access Time (milliseconds)	(minimum) (average) (maximum)	8 38 85
Recording Density (bits per inch)		14845
Track Density (tracks per inch)		834
Rotational Speed (revolutions per minute)		3600
Recording Method		MFM (Modefied Frequency Modulation)

1.5 HARD DISK CONTROL PCB

Hard disk control PCB (HDC) is accompanied by hard disk drive (HDD) and connects to the system PCB through a cable. This HDC can interface the HDD to the system PCB.
The specifications are as following table.

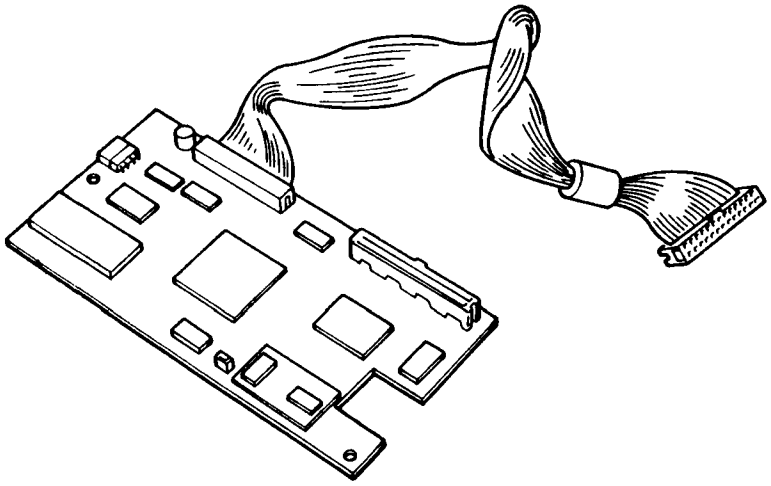


FIGURE 1-5 Hard Disk Control PCB

TABLE 1-5 Hard Disk Control PCB Specifications

Item	Specifications
Encoding method	MFM (Modefied Frequency Modulation)
Data Transfer Rate (megabits per second) maximum	5
Write Precompensation time (nanoseconds)	12
Sectoring	Soft

1.5.1 Jumper straps

The Hard disk control PCB has jumper straps which are PJ 3, PJ 4 and PJ 5.
Functions of the jumper straps are as follows.

(1) PJ 3
Not used.

(2) PJ 4
This jumper straps select recording method of the hard disk control PCB.
The following table shows function.

TABLE 1-6 PJ 4 Jumper Strap Functions

No.	Status	Function
1-2	Short	MFM method
3-4	Open	

(3) PJ 5
This jumper straps select the delay time of the hard disk control PCB.
Usually delay time is selected as 20 ns.
The following table shows function of the jumper straps.

TABLE 1-7 PJ 5 Jumper Strap Functions

No.	Delay time select
1-2	10 ns
3-4	15 ns
5-6	20 ns
7-8	25 ns
9-10	30 ns

1.6 KEYBOARD

The keyboard is mounted on the system and has 85 keys. These consist of 54 standard keys, 10 function keys, 17 cursor keys, 14 functional keypads, and Fn key.
The keyboard is just a key matrix built up by the above keys. The keyboard is connected to the keyboard controller on the system PCB through a 22-pin flat cable.

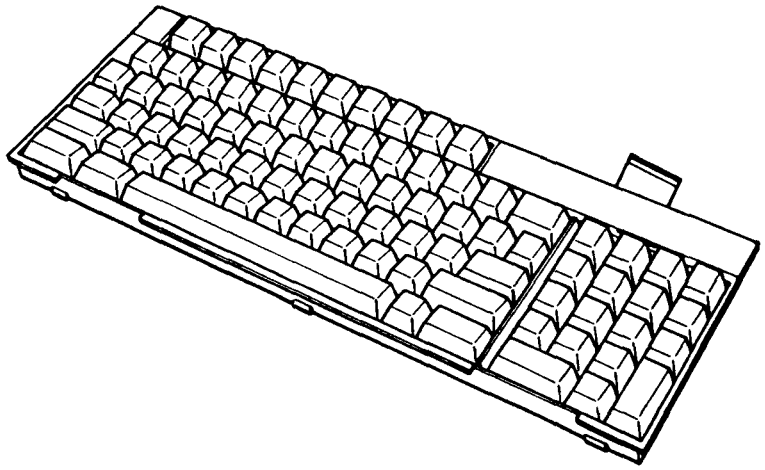


FIGURE 1-6 Keyboard

1.7 PLASMA DISPLAY

The plasma display is a graphics type display unit composed of the display panel and driver circuits. This receives vertical and horizontal sync signals, four bit data signals, and shift clock for data transmission. All these signals are TTL level compatible. The specifications are as following table.

The plasma display has 4-level of gray display.
The plasma display be adjusted by contrast/brightness control volume.

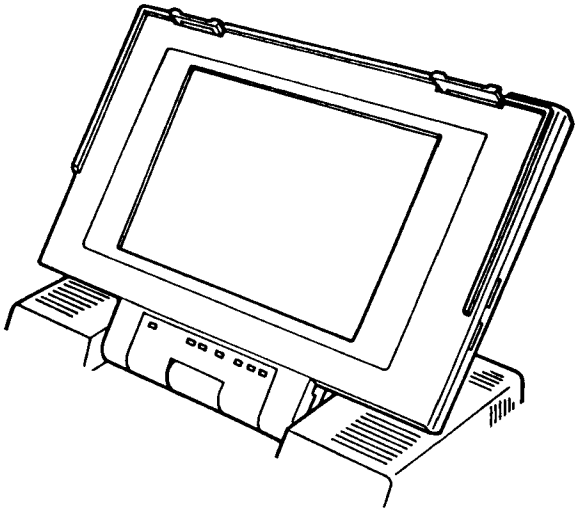


FIGURE 1-7 Plasma Display

TABLE 1-8 Plasma Display Specifications

Item	Specification
Dot Number (dots)	720 x 400
Dot Dimension (mm)	0.18 (V) x 0.16 (H)
Dot Pitch (mm)	0.36 (V) x 0.30 (H)
Display Area (mm)	144 (V) x 216 (H)
Contrast	1 : 10
Color	Neon - orange
Power Requirement	+ 5V ± 0.5V, 0.6A + 205 ± 5V, 170mA + 5V ± 0.5V, 60mA
MTBF	20000 hours

1.8 POWER SUPPLY UNIT

The power supply unit supplies dc 5, 12, -12 and 205 volts to all the components in the system.
The power supply unit is housed in the system and is designed to support the following:

1) System PCB
2) 3.5-inch Floppy disk drive
3) 3.5-inch Hard disk drive
4) Hard disk control PCB
5) Keyboard unit
6) Plasma display
7) Option PCB's

The power supply unit includes the input line filter, line fuse, cooling fan, power conversion circuitry and connectors.
Input rating is as follows.

AC 100, 115/220, 240 Volts, 60W (100W max.)

Output rating is as following table.

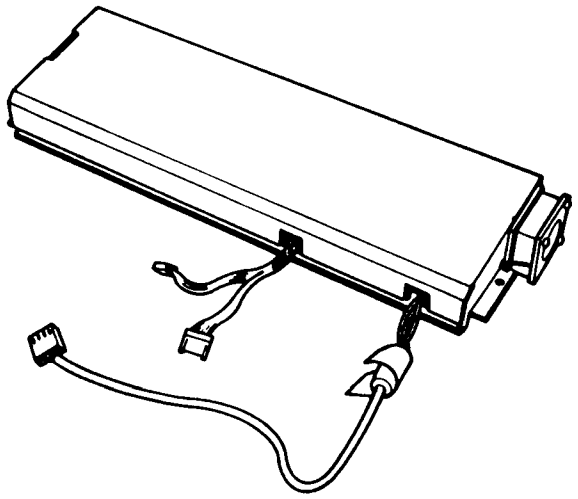


FIGURE 1-8 Power Supply Unit

TABLE 1-9 Power Supply Unit Output Rating

FUNCTION	DC VOLTAGE	REGULATION TOLERANCE	MAX. CURRENT
SYSTEM PCB	5 V	± 5 %	6.5 A
SYSTEM PCB	12 V	± 5 %	2.6 A
SYSTEM PCB	-12 V	+ 10 %, - 20 %	0.3 A
PLASMA DISPLAY	205 V	200 to 210 V	170 mA
PLASMA DISPLAY	5 V	± 10 %	60 mA

2.1 GENERAL

These problem isolation procedures are used to isolate defective FRUs (field replaceable units) to be replaced. FRUs consist of the following:

1. Power supply unit
2. System PCB
3. FDD
4. HDD and HDC
5. Keyboard
6. Plasma display

See PART 4 for detailed replacement procedures instructions. Test program operations are described in PART 3.

The following items are necessary for carrying out the problem isolation procedures.

1. T3200 Diagnostics disk
2. Flatbladed screwdriver
3. Work disk (for FDD testing)
4. Cleaning disk kit (for FDD testing)
5. Multimeter
6. Printer port LED

The problem isolation flowchart described in part 2.2 can be used to determine the necessary isolation procedures to be followed when there is a problem with the T3200.

2.2 PROBLEM ISOLATION FLOWCHART

This flowchart is used as a guide for determining which FRU is defective. Please confirm the following before performing the flowchart procedures.

1. No disk is in the FDD.
2. All optional equipment is disconnected.

See next page.

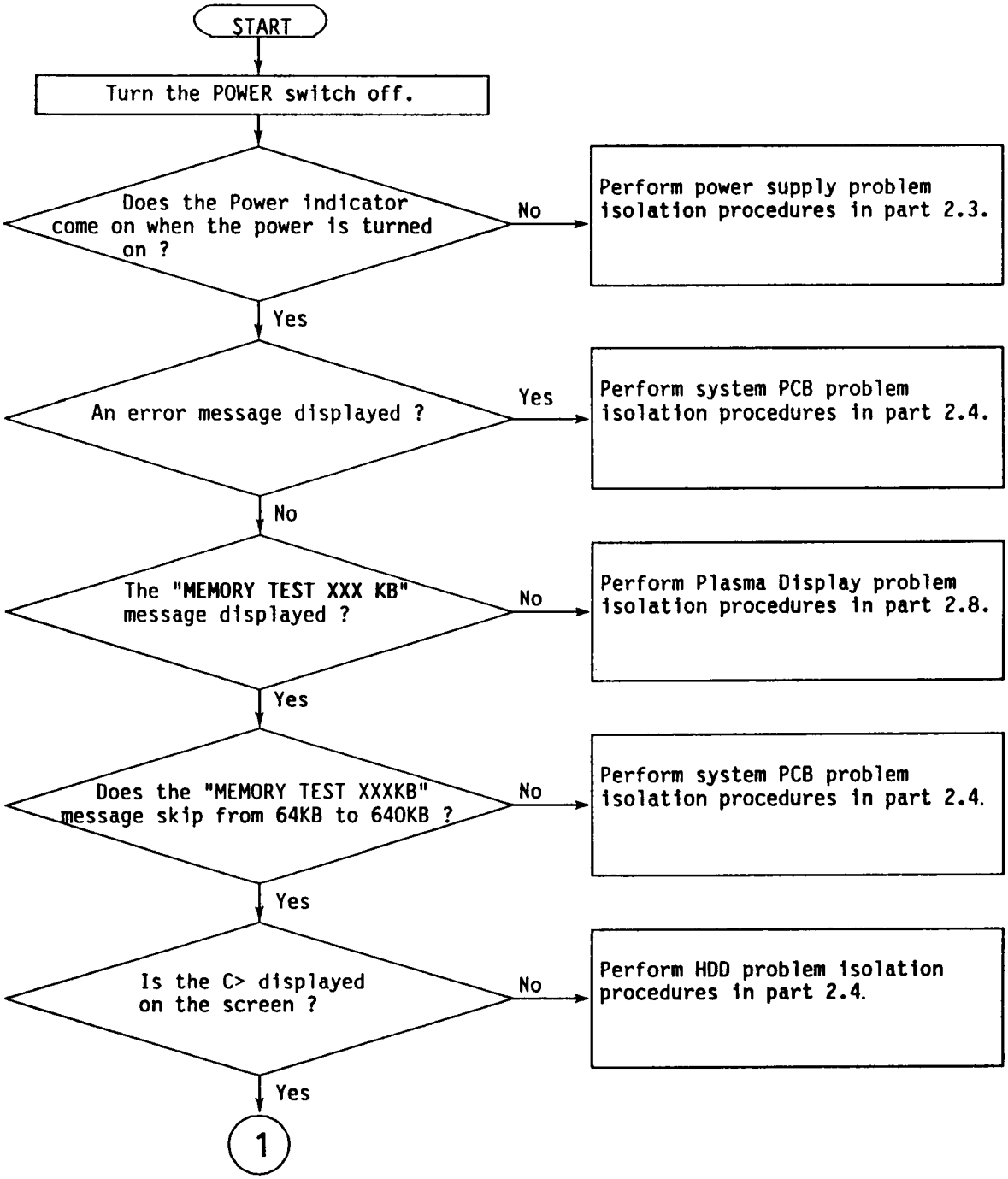
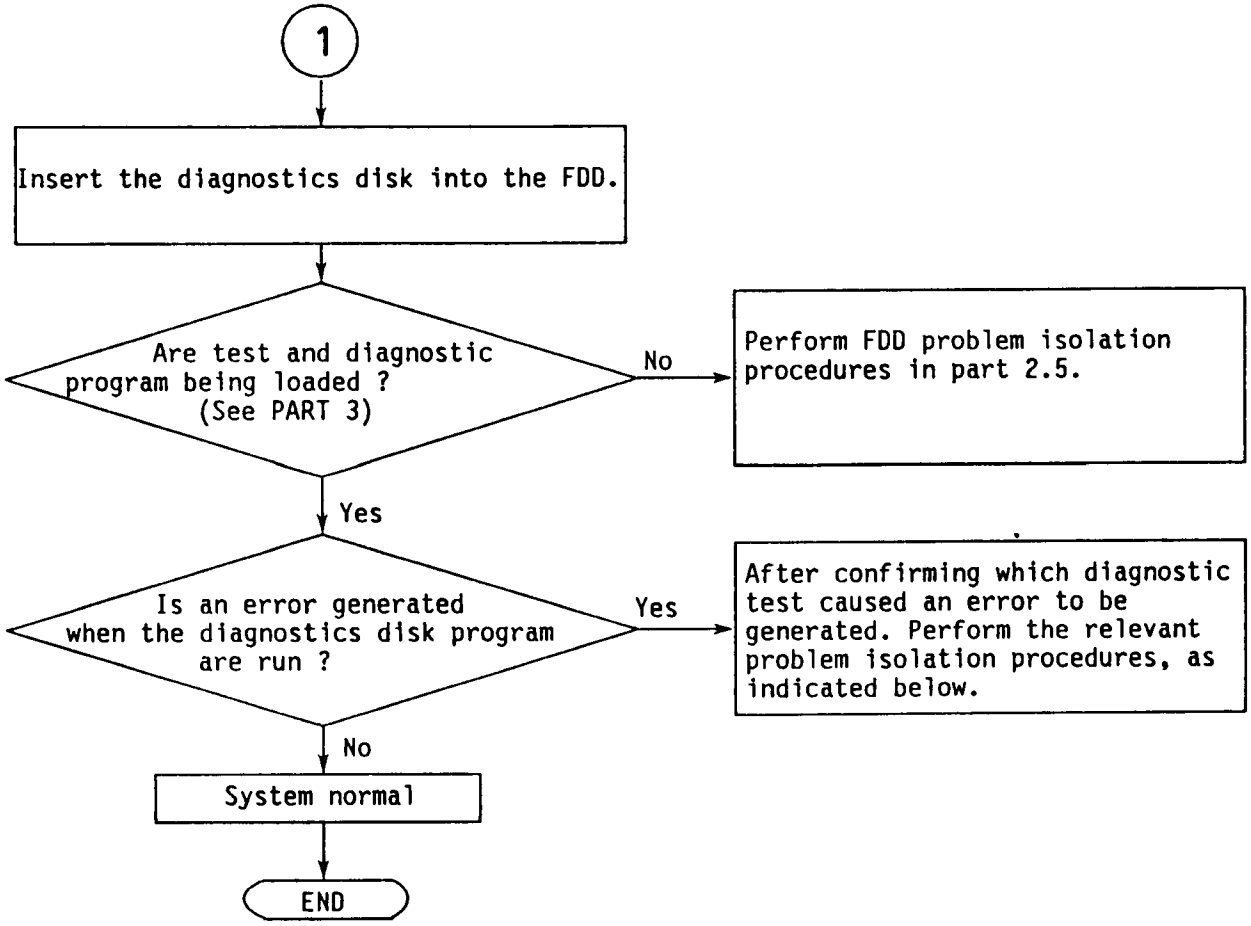


FIGURE 2-1 Problem Isolation Flowchart



1. If an error is generated on the system test, memory test, display test and real timer test, go to system PCB isolation procedures in part 2.4.

2. If an error is generated on the hard disk test, go to HDD isolation procedures in part 2.6.

3. If an error is generated on the keyboard test, go to keyboard isolation procedures in part 2.8.

4. If an error is generated on the floppy disk test, go to FDD isolation procedures in part 2.5.

2.3 POWER SUPPLY UNIT ISOLATION PROCEDURES

This section describes how to determine whether the power supply PCB is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Power Indicator Check

PROCEDURE 2: Connector Check

PROCEDURE 3: Output Voltage Check

PROCEDURE 4: Power Supply Unit Voltage Adjustment

PROCEDURE 5: Power Supply Unit Replacement

PROCEDURE 1

Power Indicator Check

1. Turn the POWER switch on.

2. If the POWER indicator lights, go to PROCEDURE 3.
   If the indicator doesn't light, replace the ac cord; if it lights, the previous ac cord was defective. If the indicator doesn't light yet, go to PROCEDURE 2.

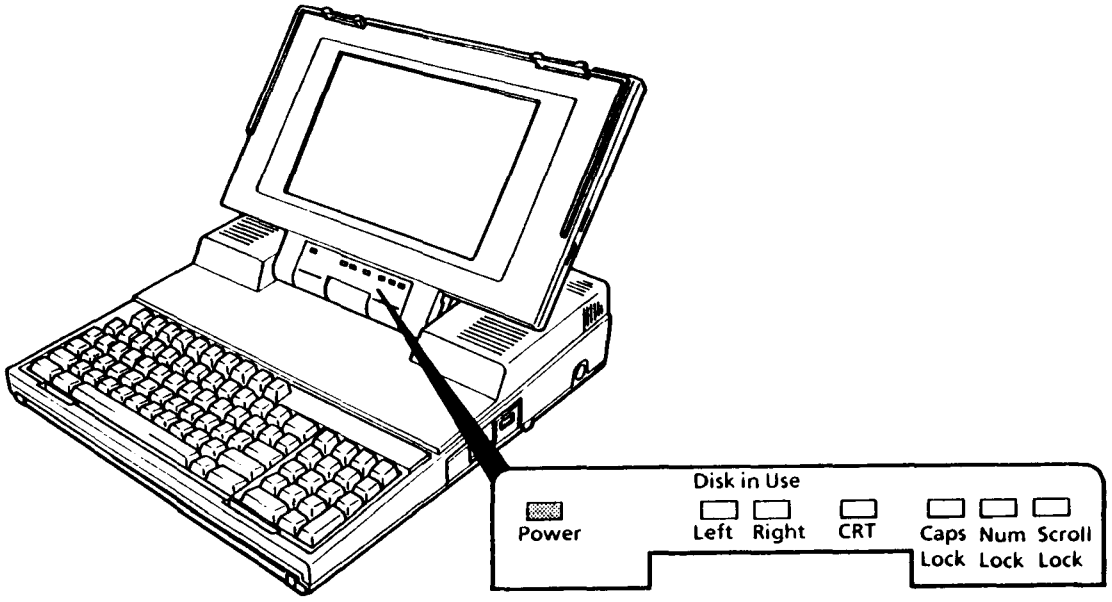


FIGURE 2-2 POWER Indicator Check

PROCEDURE 2

Connector Check

1. Turn the POWER switch off and unplug the ac cord.

2. Remove the top cover. (Refer to part 4.2.)

3. If the two system PCB connectors (PJ 7 and 8) are connected properly, go to PROCEDURE 3; if they are not connected properly, reconnect them.

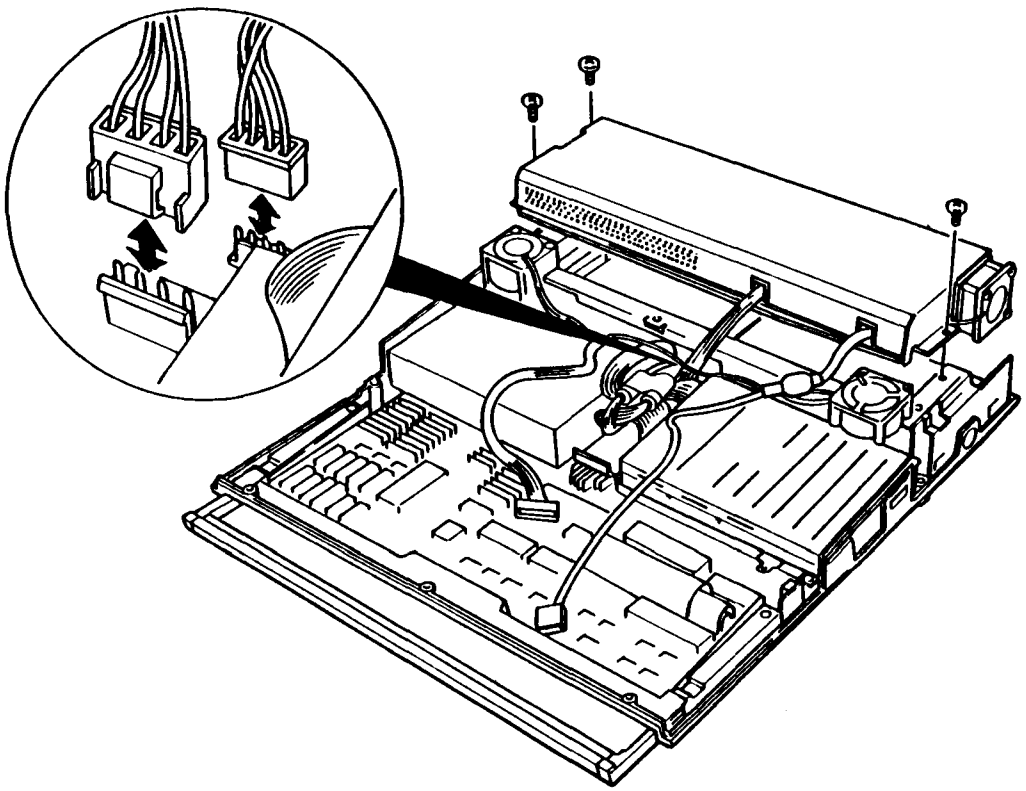


FIGURE 2-3 Power Supply Unit Connectors

PROCEDURE 3

Output Voltage Check

1. Disconnect the three power cables (for plasma display and system PCB) from the system PCB.

2. Plug the ac cord, then turn the POWER switch on.

3. Use a multimeter to confirm that the output voltages for the three power supply PCB connectors conform to the values given in the following table.

4. If the voltages conform to the values given in the table, the power supply PCB is normal. System PCB is probably defective, go to system PCB isolation procedures in part 2.4.

5. If the voltages do not conform to those given in the table, go to PROCEDURE 4.

TABLE 2-1 Power Supply Unit Output Voltages

CONNECTOR	PIN NUMBER		VOLTAGE (Vdc)		
	+ lead	- lead	Normal	Min	Max
PJ 003	1	3, 4	+ 5	+ 4.75	+ 5.25
	2	3, 4	+ 5	+ 4.75	+ 5.25
PJ 004	1	2, 4	+ 12	+ 11.4	+ 12.6
	3	2, 4	- 12	- 13.2	- 9.6
PJ 005	1	2	+ 205	+ 200	+ 210
	3	2	+ 5	+ 4.5	+ 5.5

PROCEDURE 4

Power Supply Unit Voltage Adjustment

1. Turn the POWER switch off and unplug the ac cord.
2. Remove the power supply unit. (Refer to part 4.9.)
3. Remove the power supply unit cover from the power supply unit.
4. Set the dummy load resister (1.3 kiloohm, 35 W) to the plasma display power connector (1-pin to 2-pin).
5. Plug the ac cord to the power supply unit, then turn the POWER switch on.
6. Use a multimeter to confirm that the output voltages for the plasma display power connector conform to the volues given in the following table.

TABLE 2-2 VR1 Adjustment

CONNECTOR	PIN NUMBER		VOLTAGE (Vdc)	
	+ lead	- lead	Min	Max
PJ 005	1	2	+ 201	+ 202

7. If the voltage does not conform to that given in the table, after turn the VR2 to the right, then adjust the VR1 on the power supply PCB by Phillips screwdriver.
8. Turn the POWER switch off, then remove the dummy load resister (1.3 kiloohm, 35 W).
9. Set the dummy load resister (21 kiloohm, 2.5 W) to the prasma display power connector (1-pin to 2-pin).
10. Adjust the VR2 on the systen PCB that the output voltages for the plasma display power connector conform to the values given in the following table.

TABLE 2-3 VR2 Adjustment

CONNECTOR	PIN NUMBER		VOLTAGE (Vdc)	
	+ lead	- lead	Min	Max
PJ 005	1	2	+ 208	+ 209

PROCEDURE 5

Power Supply Unit Replacement

1. Turn the POWER switch off and unplug the ac cord.
2. Replace the power supply unit. (Refer to part 4.9.)
3. If normal operation is restored after replacing the power supply unit, the previous power supply unit was defective.
4. If normal operation is not restored, another FRU is probably defective. The defective unit must be isolated and replaced.

2.4 SYSTEM PCB ISOLATION PROCEDURES

This section describes how to determine whether the system PCB is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Message Check

PROCEDURE 2: Printer Port LED Check

PROCEDURE 3: Test Program Execution

PROCEDURE 4: System PCB Replacement

NOTE: Before carrying out any of these procedures, make sure that there is not a floppy disk in the FDD.

PROCEDURE 1

Message Check

1. Turn the POWER switch on.

2. If the system is loaded, go to PROCEDURE 3.

3. If the following message is displayed on the screen, press the F1 key. Execute the setup. (Refer to OWNER'S MANUAL in PART 6.)

```
*** Error in CMOS. Bad battery ***
Check system Then. press [F1] key ......
```

```
*** Error in CMOS. Bad check sum ***
Check system Then. press [F1] key ......
```

```
**  Error in CMOS. Bad configuration **
Check system Then. press [F1] key ......
```

```
*** Error in CMOS. Bad memory size ***
Check system Then. press [F1] key ......
```

```
**  Error in CMOS. Bad time function **
Check system Then. press [F1] key ......
```

4. If the following message is displayed on the screen, go to HDD isolation procedures in part 2.6.

```
**  HDD Load error or Bad system disk **
Insert system disk in drive
Press any key when ready .....
```

5. If none of the messages are displayed and you have a printer port LED, go to PROCEDURE 3.
   If none the messages are displayed and you don't have a printer port LED, go to PROCEDURE 2.

PROCEDURE 2

Beep Sound Check

1. Turn the POWER switch off.

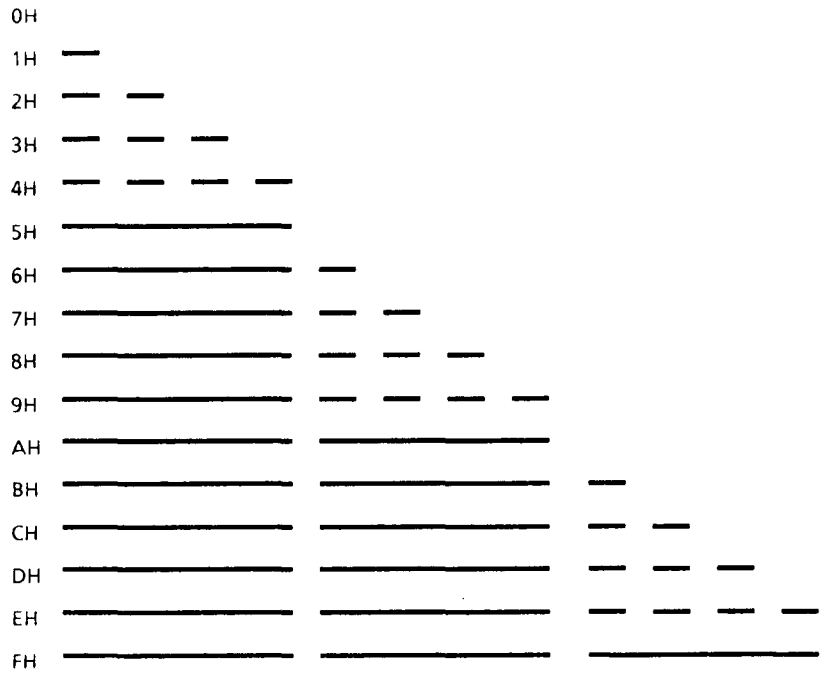
2. Turn the POWER switch on.

3. If the system occurs an error, the system informs you of an error code with the beep sound. (That is the bit information of DL register.)
   The system repeats the buzzer message three times. A hexadecimal number is configured by the combination of two groups of the beep sounds, each of which is composed of either short sounds or long sounds.
   The status of an error code is as following table.

4. If the error code conforms to the values given in the table, go to PROCEDURE 5.

5. If the error code doesn't conform to the values given in the table, another FRU is probably defective.

TABLE 2-4 Beep Sound Error Code



PROCEDURE 3

Printer Port LED Check

1. Turn the POWER switch off.

2. Plug the printer port LED into the PRT/FDD connector on the back of the unit.

3. Turn the POWER switch on while watching the printer port LED.
   The printer port LED will light at the same time that the POWER switch is turned on.

4. Read the final LED status as a hexadecimal value from left to right.

5. If the final LED status matches any of the error code values in the table 2-6 (See the next page.), go to PROCEDURE 5.

6. If the final LED status is **19H,** go to PROCEDURE 4 and continue.

TABLE 2-5 Printer Port LED Normal Status

Status	Messages
01 (H)	Initial setup of LSI start
02 (H)	Initial setup of RTC end
03 (H)	Initial setup of PIT end
04 (H)	Initial setup of DMAC(#1) end
05 (H)	Initial setup of DMAC(#2) end
06 (H)	Initial setup of PIC (#1) end
07 (H)	Initial setup of PIC (#2) end
08 (H)	Initial setup of DMA page register end
09 (H)	Initial setup of KB controller end
0A (H)	Initial setup of memory (0 - 64 KB) end
0B (H)	Initial setup of memory (64 - 640 KB) end
0C (H)	Initial setup of memory (more than 1 MB) Protect mode end
0D (H)	Initial setup of memory (more than 1 MB) Real mode end
0E (H)	Check a checksum of CMOS end
0F (H)	Check classfication of CRT end
10 (H)	Check item of CMOS end
11 (H)	Initial setup of CRT end
12 (H)	Initial setup of keyboard end
13 (H)	Initial setup of Timer end
14 (H)	Initial setup of FDD end
15 (H)	Initial setup of HDD end
16 (H)	Initial setup of option ROM end
17 (H)	Initial setup of printer end
18 (H)	Initial setup of RS232C end
19 (H)	Prepare the boot end

TABLE 2-6 Printer Port LED Error Status

Status	Error Messages	Process
81 (H)	Exception (size proc)	HALT
82 (H)	Failed PM (size proc)	HALT
83 (H)	ADR 20 failed (size proc)	HALT
84 (H)	KBC Self test error	HALT
85 (H)	KBC not ready_I (KBC init)	HALT
86 (H)	KBC not ready_O (KBC init)	HALT
87 (H)	KBC not ready_I (size ret)	HALT
88 (H)	KBC not ready_I (ex. ret size)	HALT
89 (H)	KBC not ready_I (mono set)	HALT
8A (H)	KBC not ready_I (KB init)	HALT
8B (H)	KBC not ready_I (PRT init)	HALT
8C (H)	KBC not ready_O (PRT init)	HALT
91 (H)	PE = 1 (start)	HALT
92 (H)	PE = 0 (size proc)	HALT
93 (H)	PE = 0 (mem test)	HALT
94 (H)	ROM check sum error	HALT
A1 (H)	RTC data bus error	HALT
A2 (H)	RTC int. error	HALT
A3 (H)	RTC clock error	HALT
A4 (H)	PIT data bus error	HALT
A5 (H)	PIT ch.2 output error	HALT
A6 (H)	PIT clock error	HALT
A7 (H)	PIT ch.1 output error	HALT
A8 (H)	PIT ch.0 output error	HALT
A9 (H)	DMAC #1 data bus error	HALT
AA (H)	DMAC #2 data bus error	HALT
AB (H)	PIC #1 data bus error	HALT
AC (H)	PIC #1 data bus error	HALT
AD (H)	PIC #2 data bus error	HALT
AE (H)	PIC #2 data bus error	HALT
AF (H)	MAPPER data bus error	HALT
B1 (H)	MAPPER address error	HALT
B2 (H)	Word/byte error (I/O)	HALT
B3 (H)	Exception (mem test)	HALT
B4 (H)	Failed PM (mem test)	HALT
B5 (H)	KBC not ready_I (ex. ret mem test)	HALT
B6 (H)	ADR 20 failed (mem test)	HALT
B7 (H)	KBC NOT ready_I (mem test)	HALT

Status	Error Messages	Process
B8 (H)	KBC not ready O (FDD int)	HALT
C1 (H)	Mem (base 64KB) data bus error	HALT
C2 (H)	Mem (base 64KB) word/byte error	HALT
C3 (H)	Mem (base 64KB) fixed data error	HALT
C4 (H)	Mem (base 64KB) address error	HALT
C8 (H)	Mem (base 64KB) parity circuit error	HALT
C9 (H)	Mem (base 64KB) parity circuit error	HALT
CA (H)	Mem (base 64KB) parity circuit error	HALT
CB (H)	Mem (base 64KB) parity circuit error	HALT
CC (H)	Mem (base 64KB) parity circuit error	HALT
D0 (H)		
D1 (H)	Mem (64 KB -) data bus error	HALT
D2 (H)	Mem (64 KB -) word/byte error	HALT
D3 (H)	Mem (64 KB -) fixed error	HALT
D4 (H)	Mem (64 KB -) address error	HALT
D5 (H)	Mem address error	HALT
D8 (H)	Mem (64 KB -) parity circuit error	HALT
D9 (H)	Mem (64 KB -) parity circuit error	HALT
DA (H)	Mem (64 KB -) parity circuit error	HALT
DB (H)	Mem (64 KB -) parity circuit error	HALT
DC (H)	Mem (64 KB -) parity circuit error	HALT
E1 (H)	Video RAM error (mono)	HALT
E2 (H)	Video RAM error (plasma/color)	HALT
E3 (H)	Video RAM error (plasma)	HALT
E4 (H)	CRTC error (mono)	HALT
E5 (H)	CRTC error (plasma/color)	HALT
E6 (H)	FDC error	HALT

PROCEDURE 4

Test Program Execution

1. Execute the following test program. (See PART 3 TEST AND DIAGNOSTICS.)

    1. System test
    2. Memory test
    3. Keyboard test
    4. Display test
    5. Floppy disk test
    6. Hard disk test
    7. Real timer test

2. If an error is generated on the system test, memory test, display test and real timer test, go to PROCEDURE 5.

3. If an error is generated on the floppy disk test, go to FDD isolation procedures in part 2.5.

4. If an error is generated on the hard disk test, go to HDD isolation procedures in part 2.6.

5. If an error is generated on the keyboard test, go to keyboard isolation procedures in part 2.7.

PROCEDURE 5

System PCB Replacement

1. Replace the system PCB. (Refer to part 4.14)

2. If normal operation is restored after replacing the PCB, the previous PCB was defective.

3. If normal operation is not restored, another FRU is probably defective. The defective unit must be isolated and replaced.

2.5 FLOPPY DISK DRIVE ISOLATION PROCEDURES

This section describes how to determine whether the floppy disk drive is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Test and Diagnostic Program Loading Check

PROCEDURE 2: Message Check

PROCEDURE 3: Head Cleaning

PROCEDURE 4: FDD Test Execution

PROCEDURE 5: FDD Connector Check

PROCEDURE 6: New FDD connection

PROCEDURE 1

Test and Diagnostic Programs Loading Check

1. Turn the POWER switch off.
2. Insert the diagnostics disk into the FDD.
3. Turn the POWER switch on.
4. If loading occurs normally, go to PROCEDURE 3. (See PART 3 to determine if loading has occurred normally.)
5. If loading has not occurred normally, go to PROCEDURE 2.

PROCEDURE 2

Message Check

1. When the diagnostics disk is inserted into the FDD and the POWER switch is turned on, message (a), message (b), message (c) or message (d) should appear.

(a)
```
**** FDD A in not installed ****
```

(b)
```
Non-System disk or disk error
Replace and press any key when ready
```

(c)
```
** FDD load error or Bad system disk **
Insert system disk in drive
Press any key when ready .....
```

(d)
```
** HDD Load error or Bad system disk **
Insert system disk in drive
Press any key when ready .....
```

2. If (a) of the above message is displayed, confirm that the A-B-PRT switch is set to the PRT side. If it is not seted to the PRT side, set the PRT side; if it is seted to the PRT side, go to PROCEDURE 5.

3. If (b), (c) or (d) of the above messages is displayed, the contents of the floppy disk are damaged, or some other disk than the diagnostics disk has been inserted into the FDD. Change the diagnostics disk. If loading then occurs, go to PROCEDURE 4; if loading does not occur, go to PROCEDURE 3.

4. If none of the above messages appears, go to PROCEDURE 5.

PROCEDURE 3

Head Cleaning

1. Turn the POWER switch off.
2. Insert the cleaning disk to the FDD.
3. Turn the POWER switch on.
4. If normal operation is restored after cleaning the head, go to PROCEDURE 4.
5. If normal operation is not restored, go to PROCEDURE 5.

PROCEDURE 4

FDD Test Execution

1. Run the floppy disk test which is indicated in the Diagnostic Test Menu.

2. If an error is generated during the floppy disk test, an error code and status will be displayed as indicated in the following table. Follow the directions provided in the table.

3. If no error is generated, the FDD is normal.

TABLE 2-7 FDD Error Status

CODE	STATUS
01	Bad Command
02	Address Mark Not Found
03	Write Protected
04	Recod Not Found
06	Media removed on dual attach card
08	DMA Overrun Error
09	DMA Boundary Error
10	CRC Error
20	FDC Error
40	SEEK ERROR
60	FDD not drive
80	Time Out Error (Not Ready)
EE	Write buffer error

PROCEDURE 5

FDD Connector Check

1. Turn the POWER switch off and disconnect the ac cord.
2. Remove the top cover. (Refer to part 4.2.)
3. If the FDD cable is connected to the system PCB securely, go to PROCEDURE 6.
4. If the above connections are not secure, reconnect them.

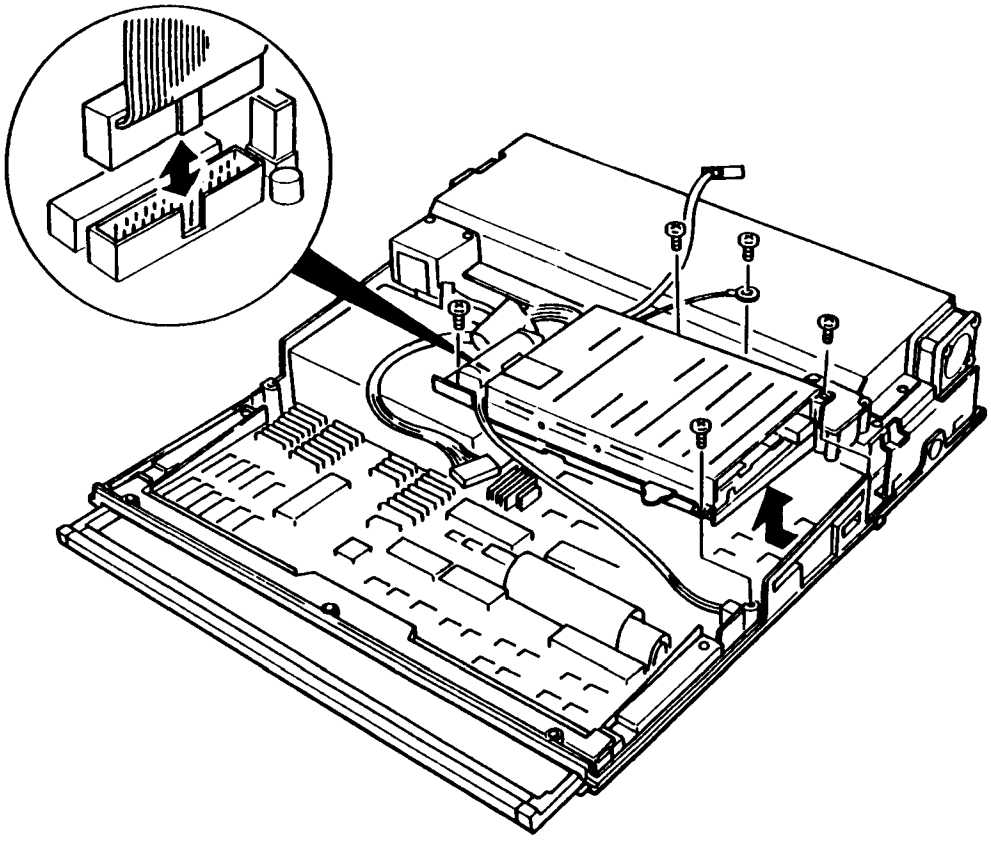


FIGURE 2-4 FDD Connector Check

PROCEDURE 6

New FDD Connection

1. Turn the POWER switch off.
2. Remove the FDD. (Refer to part 4.10.)
3. Connect the new FDD to the FDD connector, then other connectors too.
4. Turn the POWER switch on.
5. If normal operation is restored after connect the new FDD, the previous FDD was defective. Assemble the system.
6. If normal operation is not restored, system PCB is probably defective. Refer to part 2.4.

2.6 HARD DISK DRIVE ISOLATION PROCEDURES

This section describes how to determine whether the Hard Disk Drive is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: HDD Indicator Check

PROCEDURE 2: Message Check

PROCEDURE 3: Format Execution

PROCEDURE 4: Hard Disk Test Execution

PROCEDURE 5: Connector Check

PROCEDURE 6: New HDC Connection

PROCEDURE 7: New HDD Connection

PROCEDURE 1

HDD Indicator Check

1. Turn the POWER switch off.
2. If there is a floppy disk in the FDD, take it out.
3. Turn the POWER switch on.
4. If the HDD indicator (Disk In Use - Left) blinks briefly and goes out, go to PROCEDURE 2; if it continues blinking, go to PROCEDURE 4.
5. If the indicator does not light at all, go to PROCEDURE 5.

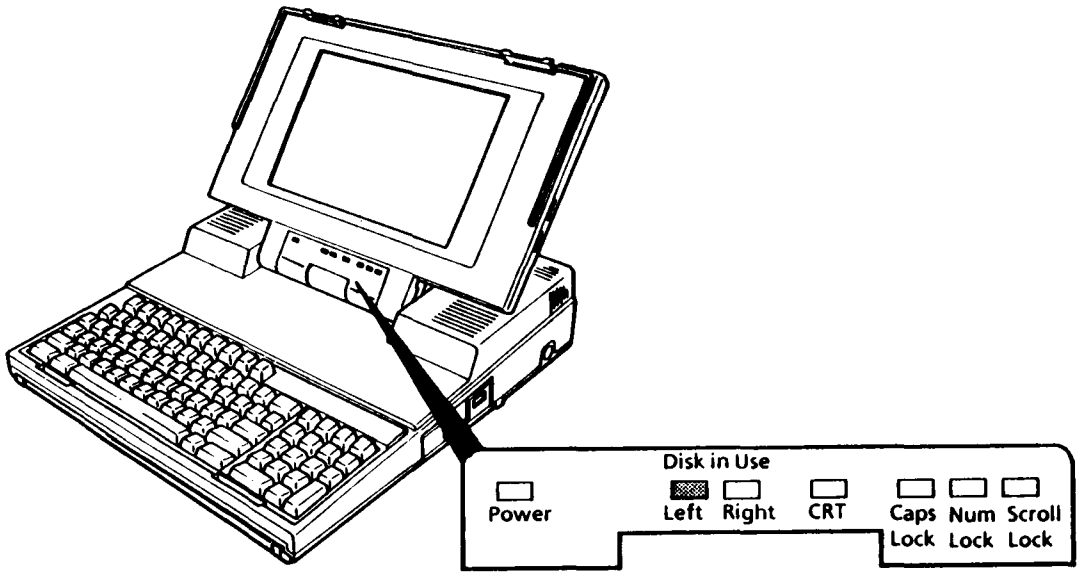


FIGURE 2-5 HDD Indicator Check

PROCEDURE 2

Message Check

1. If the system is loaded, go to PROCEDURE 4.

2. If the following message is displayed on the screen, go to PROCEDURE 3.

```
** HDD Load error or Bad system disk **
Insert system disk in drive
Press any key when ready .....
```

PROCEDURE 3

Format Execution

CAUTION: The contents of the hard disk will be erased when the FORMAT command is run. Before running the test, transfer the contents of the hard disk on the floppy disk. This can be done with the MS-DOS BACKUP command. (See the MS-DOS manual for details.)

1. Remove the diagnostics disk, and then insert the MS-DOS system disk to the FDD.
2. To set the partition of the hard disk, enter the FDISK command. (See the MS-DOS manual for details.)
3. To format the hard disk, enter the FORMAT command. (See the MS-DOS manual for details.)
4. If normal operation is restored, the HDD is normal.
5. If normal operation is not restored, go to PROCEDURE 6.

PROCEDURE 4

Hard Disk Test Execution

CAUTION: The contents of the hard disk will be erased when the test program is run. Before running the test, transfer the contents of the hard disk on the floppy disk. This can be done with the MS-DOS BACKUP command. (See the MS-DOS manual for details.)

1. Insert the diagnostics disk into the FDD and load the test and diagnostic programs.

2. Run the hard disk test which is indicated in the diagnostics test menu.

3. If an error is generated during the hard disk test, an error code and status will be displayed as indicated in the following table. Go to PROCEDURE 6.

4. If no error is generated, the HDD is normal. Enter the MS-DOS FDISK command which will set the partition. Then enter the MS-DOS FORMAT command. (See the MS-DOS manual for details.)

TABLE 2-8 HDD Error Status

CODE	STATUS
01	Bad command error
02	Bad address mark
04	Record not found
05	HDC NOT RESET
07	Drive not initialize
09	DMA Boundary error
0A	Bad sector error
0B	Bad track error
10	ECC error
11	ECC recover enable
20	HDC error
40	Seek error
80	Time out error
AA	Drive not ready
BB	Undefined
CC	Write fault
E0	Status error
F0	Not sense error (HW.code = FF)

PROCEDURE 5

Connector Check

1. Turn the POWER switch off and disconnect the ac cord.
2. Remove the top cover. (Refer to part 4.2)
3. If the HDD, HDC, and system PCB are connected securely, go to PROCEDURE 6.
4. If they are not connected securely, reconnect them.

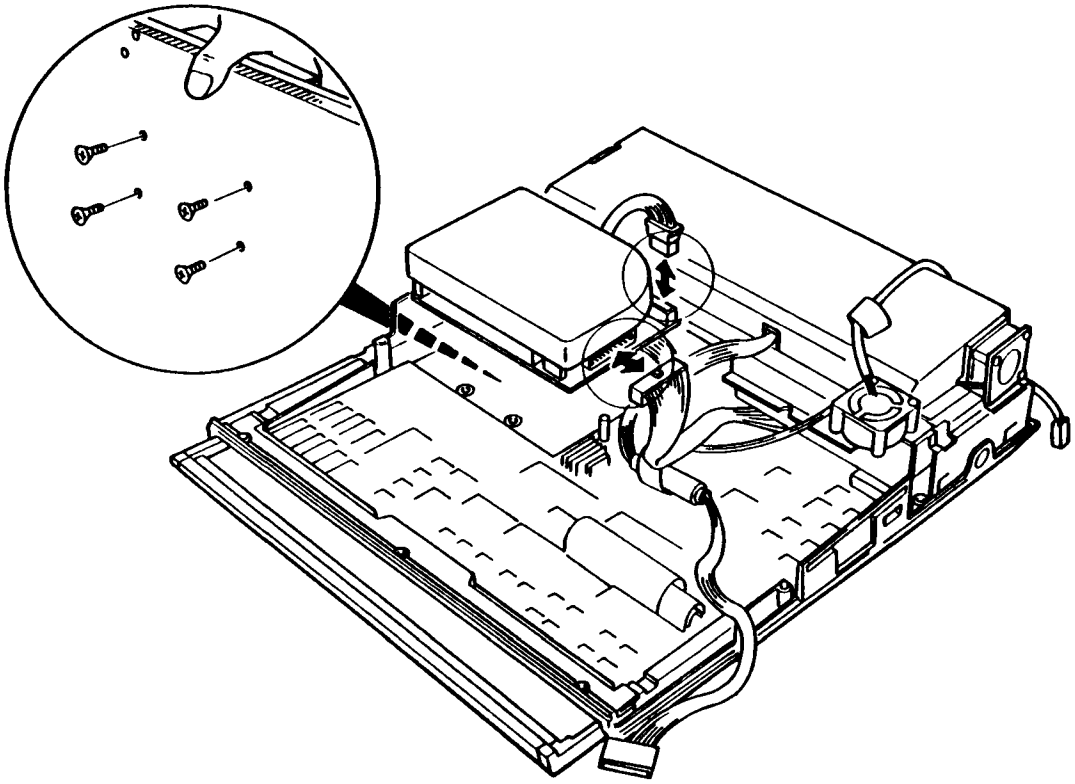


FIGURE 2-6 HDC and HDD Connector Check

PROCEDURE 6

New HDC Connection

1. Turn the POWER switch off and disconnect the ac cord.
2. Remove the HDC. (Refer to part 4.13.)
3. Connect the new HDC to the system PCB and HDD, then other connectors too.
4. If normal operation is restored, the previous HDC was defective. Assemble the system.
5. If normal operation is not restored, HDD is probably defective. Go to PROCEDURE 7.

PROCEDURE 7

New HDD Connection

1. Turn the POWER switch off.
2. Remove the HDD. (Refer to part 4.11.)
3. Connect the new HDD to the HDC, then other connectors too.
4. If normal operation is restored, the previous HDD was defective. Assemble the system.
5. If normal operation is not restored, system PCB is probably defective. System PCB is probably defective. Refer to part 2.4.

2.7 KEYBOARD ISOLATION PROCEDURES

This section describes how to determine whether the keyboard is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Input Check

PROCEDURE 2: Keyboard Test Execution

PROCEDURE 3: Connector Check

PROCEDURE 4: New Keyboared Connection

PROCEDURE 1

Input Check

1. Load either the diagnostics disk or the MS-DOS system disk.

2. When a prompt (A, B, C, etc.) appears on the screen, hit any of the white keys on the keyboard (any character or the space bar). If the character you hit appears on the screen, go to PROCEDURE 2.

3. If the character does not appear, go to PROCEDURE 3.

```
Toshiba Personal Computer MS-DOS Version 3.20 / (RXXXXX)

   (C) Copyright  Toshiba     Corporation 1983,1986
   (C) Copyright  Microsoft   Corporation 1981,1986

Current date is XXX  X-XX-19XX
Enter new date (mm-dd-yy) : _
Current time is X:XX:XX,XX
Enter new time : _

COMMAND Version 3.20
A> abcdefghijklmnopqrst.................
```

PROCEDURE 2

Keyboard Test Execution

1. Insert the diagnostics disk into the FDD and load the test and diagnostics programs. (Refer to PART 3.)

2. Run the keyboard test which is indicated in the diagnostics test menu.

3. If an error is generated during the test, go to PROCEDURE 3.

4. If no error is generated during the test, the keyboard is normal.

PROCEDURE 3

Connector Check

1. Turn the POWER switch off and disconnect the ac cord.
2. Remove the top cover. (Refer to part 4.2)
3. Lift the keyboard up and check that the keyboard cable is connected securely to the system PCB. If it is connected securely, go to PROCEDURE 4.
4. If it is not connected securely, reconnect it.

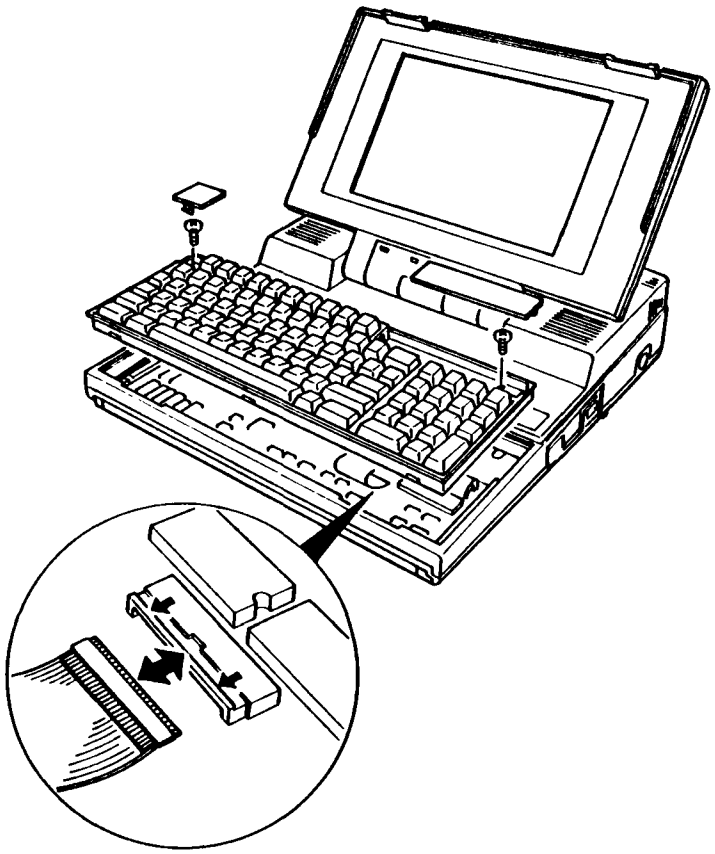


FIGURE 2-7 Keyboard Connector Check

PROCEDURE 4

New Keyboard Connection

1. Turn the POWER switch off and unplug the ac cord.
2. Remove the keyboard unit. (Refer to part 4.7.)
3. Connect the new keyboard to the system PCB.
4. If normal operation is restored after connect the keyboard, the previous keyboard was defective. Assemble the system.
5. If normal operation is not restored, system PCB is probably defective. Refer to part 2.4.

2.8 PLASMA DISPLAY ISOLATION PROCEDURES

This section describes how to determine whether the PLASMA DISPLAY is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Display Check

PROCEDURE 2: Plasma Display Contrast and Brightness Check

PROCEDURE 3: Display Test Execution

PROCEDURE 4: Plasma Display Connector Check

PROCEDURE 5: New PDP Connection

PROCEDURE 1

Display Check

1. Turn the POWER switch off.

2. After turning the POWER switch on again, the following message should appear in the upper left-hand corner of the screen:

MEMORY TEST XXXKB

3. If the message appears, go to PROCEDURE 2.

4. If the message does not appear, first do the following:

   (a) Confirm that the contrast and brightness volume is adjusted correctly.

   (b) Confirm that the display is not on an external CRT. (The CRT indicator lamp will be lit if the display is on an external CRT.)

   (C) Confirm that the DIP switch is OFF.

   After confirming (a), (b) and (c) above, perform steps 1 and 2 again. If the message still fails to appear, go to PROCEDURE 3.

PROCEDURE 2

Plasma Display Contrast and Brightness Check

1. Turn the contrast and brightness volume, then confirm that the screen becomes changed darker or brighter.

2. If the screen is changed darker or brighter, power supply inputs voltage to the PDP. Go to PROCEDURE 7.

3. If the screen is not changed, go to PROCEDURE 4.

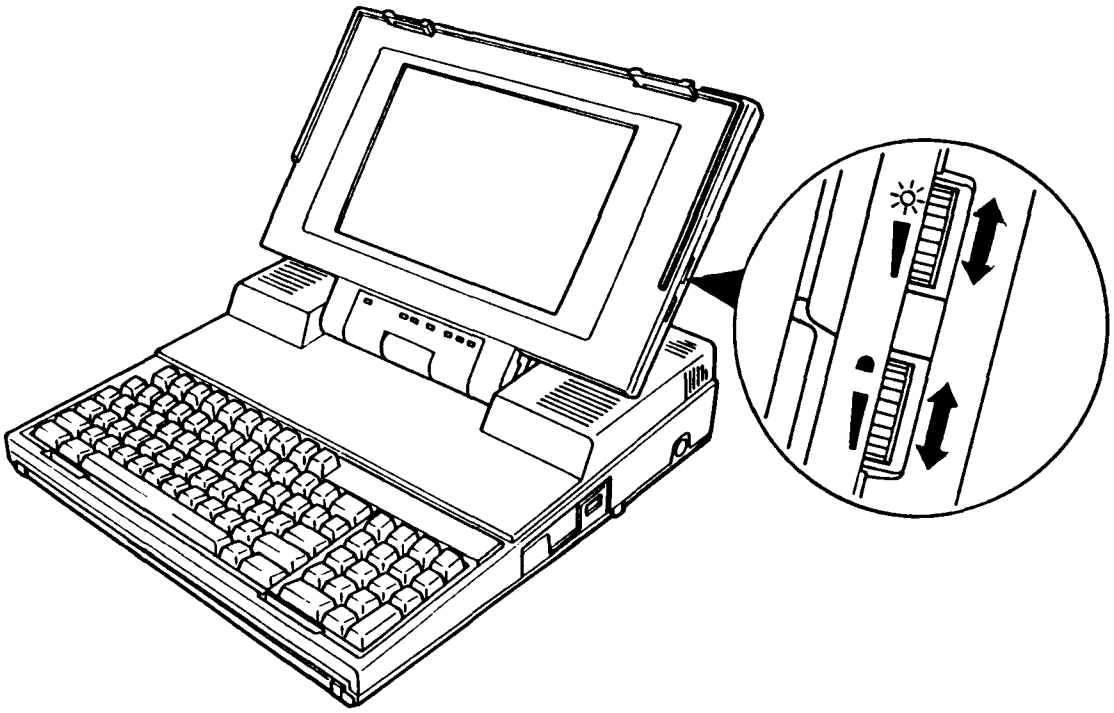


FIGURE 2-8 Plasma Display Contrast and Brightness Check

PROCEDURE 3

Display Test Execution

1. Insert the diagnostics disk into the FDD and run the test and diagnostics programs.

2. If an error is generated during the display test from the diagnostics test menu, the system PCB is probably defective. Refer to part 2.4.

3. If no error is generated, the plasma display is normal.

PROCEDURE 4

PDP Connector Check

1. Turn the POWER switch off and unplug the ac cord.
2. Take out the PDP (Refer to part 4.4.) and confirm that the plasma display cable is connected securely to the module.
3. If the cable is connected securely, go to PROCEDURE 6.
4. If the cable is not connected securely, reconnect it.

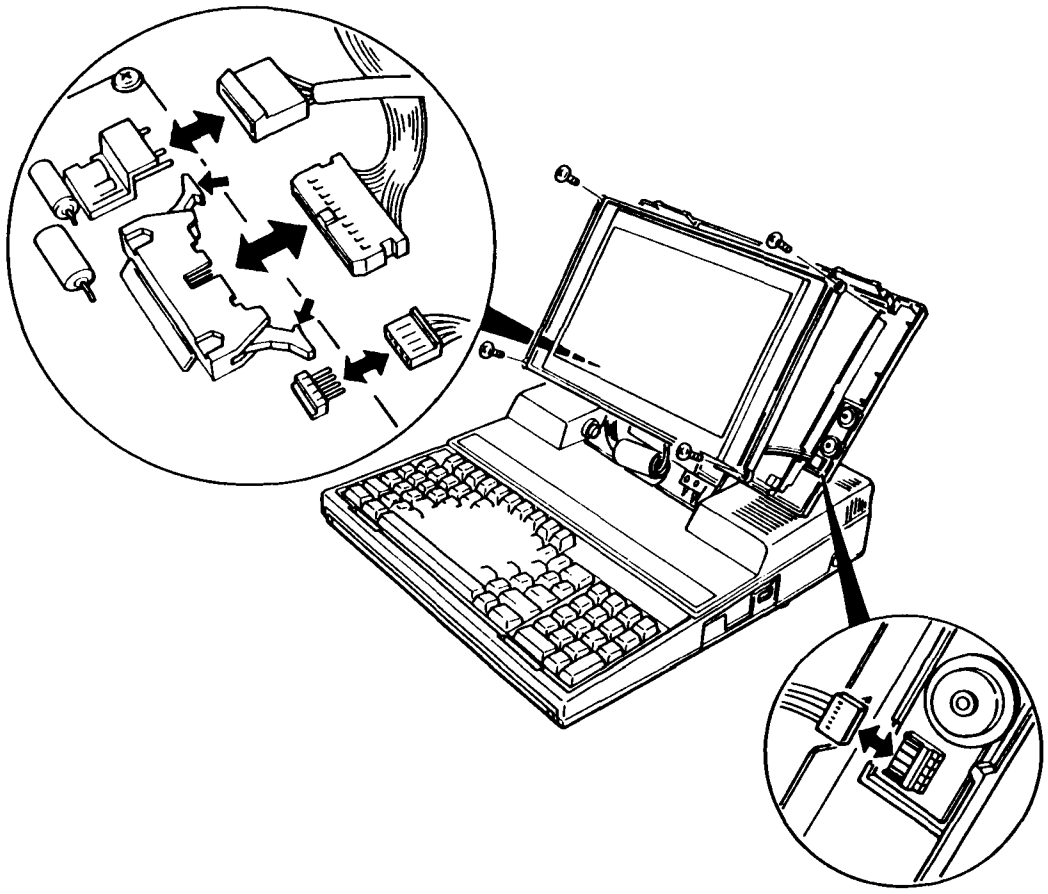


FIGURE 2-9 PDP Connector Check

PROCEDURE 5

New PDP Connection

1. Connect a new PDP and plasma display cable to the PDP.
2. If normal operation is restored after replacing the PDP, the previous PDP was defective. Assemble the system.
3. If normal operation is not restored, system PCB is probably defective. System PCB is probably defective. Refer to part 2.4.

3.1 GENERAL

This part explains test and diagnostic programs. The purpose of the test and diagnostic programs is to check the functions of all hardware modules of the T3200 Personal Computer.
There are 19 programs; they are composed of two modules: the service program module (DIAGNOSTICS MENU) and test program module (DIAGNOSTIC TEST MENU).
The service program module is composed of 8 tasks:

1. HARD DISK FORMAT
2. SEEK TO LANDING ZONE (HDD)
3. HEAD CLEANING
4. LOG UTILITIES
5. RUNNING TEST
6. FDD UTILITIES
7. SYSTEM CONFIGURATION
8. SETUP

The test program module is composed of 11 tests as follows:

1. SYSTEM TEST
2. MEMORY TEST
3. KEYBOARD TEST
4. DISPLAY TEST
5. FLOPPY DISK TEST
6. PRINTER TEST
7. ASYNC TEST
8. HARD DISK TEST
9. REAL TIMER TEST
10. NDP TEST
11. EXPANSION TEST

The following items are necessary for carrying out the test and diagnostic programs.

1. T3200 Diagnostics disk
2. MS-DOS system disk
3. Work disk (formatted)
4. Cleaning disk kit
5. Printer wraparound connector
6. RS232C wraparound connector

The service engineer utilizes these programs to isolate problems by selecting the appropriate program and operation procedures described in the part 3.2 OPERATIONS.

3.2 OPERATIONS

1. Insert the diagnostics disk in the floppy disk drive and turn the POWER switch on.

2. Input **TESTCE3** for the **A>** prompt and press Enter.

3. The following display will appear.

```
TOSHIBA personal computer T3200 DIAGNOSTICS
Version X.XX (C) copyright TOSHIBA Corp. 1987

DIAGNOSTIC  MENU :

   1 - DIAGNOSTIC TEST
   2 - HARD DISK FORMAT
   3 - SEEK TO LANDING ZONE (HDD)
   4 - HEAD CLEANING
   5 - LOG UTILITIES
   6 - RUNNING TEST
   7 - FDD UTILITIES
   8 - SYSTEM CONFIGURATION
   9 - EXIT TO MS-DOS
   0 - SETUP

PRESS [0] - [9] KEY
```

Detailed explanations of the service programs and the operations are given in parts 3.16 to 3.23.

4. Press 1 key then Enter. The following display will appear.

```
TOSHIBA personal computer T3200 DIAGNOSTICS
version X.XX (C) copyright TOSHIBA Corp. 1987

DIAGNOSTIC  TEST MENU :

    1 - SYSTEM TEST
    2 - MEMORY TEST
    3 - KEYBOARD TEST
    4 - DISPLAY TEST
    5 - FLOPPY DISK TEST
    6 - PRINTER TEST
    7 - ASYNC TEST
    8 - HARD DISK TEST
    9 - REAL TIME TEST
   10 - NDP TEST
   11 - EXPANSION TEST
   88 - FDD & HDD ERROR RETRY COUNT SET
   99 - EXIT TO DIAGNOSTICS MENU

PRESS [1] - [9] KEY
```

If you want to set the FDD and HDD retry count, type 88 then press Enter. The following message will appear.
When don't operate, error retry count number is onece.

FDD & HDD Error retry count ?

You can set the error retry count of the floppy disk test and hard disk test.

Type 99 then press Enter. Return to the DIAGNOSTICS MENU.

When select the FLOPPY DISK TEST, the following messages will appear.

Test drive number select (1:FDD1,2:FDD2,0:FDD1&2) ?

Media in drive#1 mode (1:360k,2:360k-1.2M/720k,3:1.2M,4:720k) ?

Test start track (Enter:0/dd:00-79) ?

In the case of type the test start track, test start track number of the floppy disk is one digit or two digits.
When press Enter only, test start track number is zero track.

When select the HARD DISK TEST, the following message will appear.

Test drive number select (1:HDD1,2:HDD2,0:HDD1&2) ?

5. After pressing the test number (1 to 11) of the DIAGNOSTIC TEST MENU, the following display (sample) will appear.

```
TEST NAME                                    XXXXXXX

SUB TEST    :  XX
PASS COUNT  :  XXXXX       ERROR COUNT :  XXXXX
WRITE DATA  :  XX          READ DATA   :  XX
ADDRESS     :  XXXXX       STATUS      :  XXX

SUB-TEST MENU  :

01 - ROM CHECKSUM
 :   :
 :   :
99 - Exit to DIAGNOSTIC TEST MENU

SELECT SUB-TEST NUMBER ? _
TEST LOOP (1:YES/2:NO) ? _
ERRR STOP (1:YES/2:NO) ? _
```

6. Select the subtest number. Type the subtest number then press the Enter. The following message will appear.
When select the KEYBOARD TEST, the following message will not appear.

TEST LOOP (1:YES/2:NO) ?

When select the (YES);
Each time a test cycle ends, it increments the pass counter by one and repeats the test cycle..
When select the (NO);
At the end of a test cycle, it terminares the test execution and exits to the subtest menu.

7. Type the 1 or 2 then press Enter. The following message will appear.

ERROR STOP (1:YES/2:NO) ?

When select the (YES);
When an error occurs, it displays the error status and stops the execution of the test program. The operation guide displays on the right side of the display screen.
When select the (NO);
When an error occurs, it displays the error status then it increments the error counter by one and goes to the next test.

8. Type the 1 or 2 then press the Enter. The test program will run. Each subtest names described in the part 3.3.

9. When stop the test program, press Ctrl + Break keys then return to the DIAGNOSTICS MENU.

10. When error occurs on the test program, the following message will appear.

ERROR STATUS NAME [[HALT OPERATION]]
1: Test End
2: Continue
3: Retry

1: Terminates the test program execution and exits to the subtest menu.
2: Continues the test.
3: Retry the test.

The error code and error status names described in part 3.15.

3.3 SUBTEST NAMES

The following table shows subtest name of the test program.

TABLE 3-1 Subtest Names

#	TEST NAME	SUBTEST#	TEST ITEMS
1	SYSTEM	01	ROM checksum
		02	HW status
2	MEMORY	01	RAM constant data
		02	RAM address pattern data
		03	RAM refresh
		04	Protected mode
		05	Protected mode (3MB)
		06	LIM (Expansion memory)
3	KEYBOARD	01	Pressed key display
		02	Pressed key code display
4	DISPLAY	01	VRAM read/write
		02	Character attributes
		03	Character set
		04	80*25 Character display
		05	Graphics display (color set 0/1)
		06	640*200 Graphics display
		07	640*200 Graphics display
		08	Display page
		09	"H" pattern display
		10	Special attribute test
5	FDD	01	Sequential read
		02	Sequential read/write
		03	Random address/data
		04	Write specified address
		05	Read specified address
6	PRINTER	01	Ripple pattern
		02	Function
		03	Wrapa around
7	ASYNC	01	Wrap around (channel - 1)
		02	Wrap around (channel - 2)
		03	Point to point (send)
		04	Point to point (receive)
		05	Card modem loopback
		06	Card modem on-line test
		07	Dial tester test
8	HDD	01	Sequential read
		02	Address uniquence
		03	Random address/data
		04	Cross talk & peek shift
		05	Write/read/compare(CE)
		06	Write specified address
		07	Read specified address
		08	ECC circuit (CE cylinder)
		09	Sequential write
9	REAL TIMER	01	Real time test
		02	Backup memory test
		03	Real time carry test
10	NDP	01	NDP test
11	EXPANSION UNIT	01	Box wrap around test
		02	Box mono video ram test
		03	Wrap around test (16bit bus)

3.4 SYSTEM TEST

Subtest 01 ROM checksum (Execution time: 1 second)

This test performs the ROM checksum test on the system PCB.
(Test extent : F0000H - FFFFFH 64KB)

Subtest 02 H/W status

This test reads hardware status of the system, then displays the status as shown below.

```
            76543210
H/W status = 10011101

   Bit7 --- Display mode   = Plasma
   Bit6 --- CPU clock      = 12MHz
   Bit5 --- Ten key PAD    = OFF
   Bit4 --- 2MB FDD        = 1.6MB
   Bit3 --- Internal FDDs  = 1
   Bit2 --- Drive A/B      = Normal
   Bit1 --- External FDD   = OFF
   Bit0 --- Internal FDD   = 2DD type

[DIP]
   SW1    --- Auto SW      = Disable
   SW4    --- Font Mode    = Single
   SW6    --- European Font= Other
   SW7-10 --- Monitor Type = RGB 350
```

3.5 MEMORY TEST

Subtest 01 RAM constant data (Execution time: 30 seconds)

This test writes constant data to Memory, and then reads and compares them with the original data. The constant data are "FFFFH", "AAAAH", "5555H", "0101H" and "0000H".

Subtest 02 RAM address pattern data (Execution time: 10 seconds)

This test makes the segment address and offset address by XORing, and then writes the address pattern data and reads and compares them with the original data.

Subtest 03 RAM refresh (Execution time: 20 seconds)

This test writes constant data in 256 bytes length to Memory, and then reads and compares it with the original data. The constant data are "AAAAH" and "5555H". A certain interval time will be taken between the write and the read operations.

Subtest 04 Protected mode (Execution time: 78 seconds)

This test writes fixed data and address data to memory (256 kbytes to MAX 640 kbytes or 1 Mbytes to MAX. Mbytes) in protect mode, and then reads and compares it with the original data.

Subtest 05 Protected mode (3MB) (Execution time: 74 seconds)

This test writes fixed data and address data to memory (1 Mbytes to 4 Mbyts) in protect mode, and then reads and compares it with the original data.

Subtest 06 LIM (Expansion memory) (Execution time: 84 seconds)

Run the same test as subtest 04 for the expansion memory page frame address (D0000H) and the block select register (208H/218H) and memory size (3 Mbytes + 384 kbytes). This performed for every 64 kbytes.

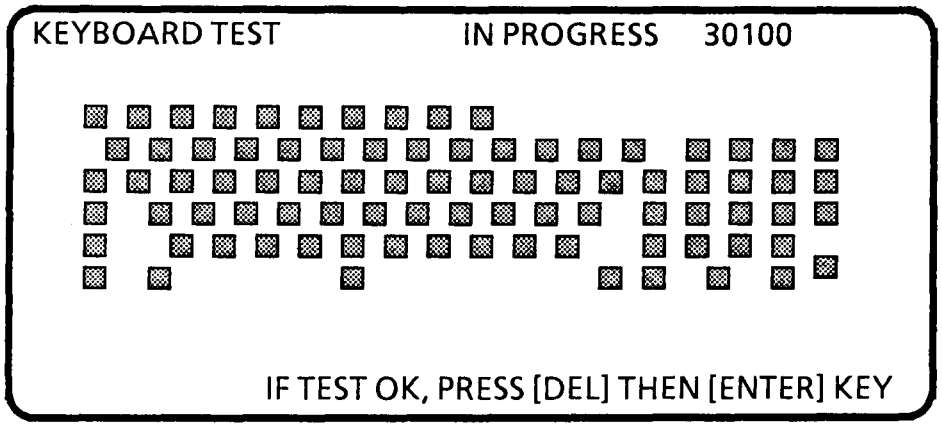
3.6 KEYBOARD TEST

Subtest 01 Pressed key display

Note: Execute the test when Num-lock key is off. If this key is on, the test cannot be carried out.

When the keyboard layout (as shown below) is drawn on the display, press a certain key and check whether the corresponding key on the screen is changed to the character "*".
When the same key again, it becomes to be the original state so that it is able to confirm the self-repeat function.
The following three keys are exceptions, and each key is changed to the character "*" only when it is pressed, and if released, it gets back to the original state.

Ctrl key, Shift key, Alt key



Subtest 02 Pressed key code display

Scan code, character code, and key top name are displayed on the screen by pressing a certain key as shown below.
Some keys such as Ins, Caps lock, Num lock, Scroll lock, Alt, Ctrl, and shift key blink on the screen when each one is pressed.
Each scan code, character code and key top name described in the TABLE 3-2.(Next page)

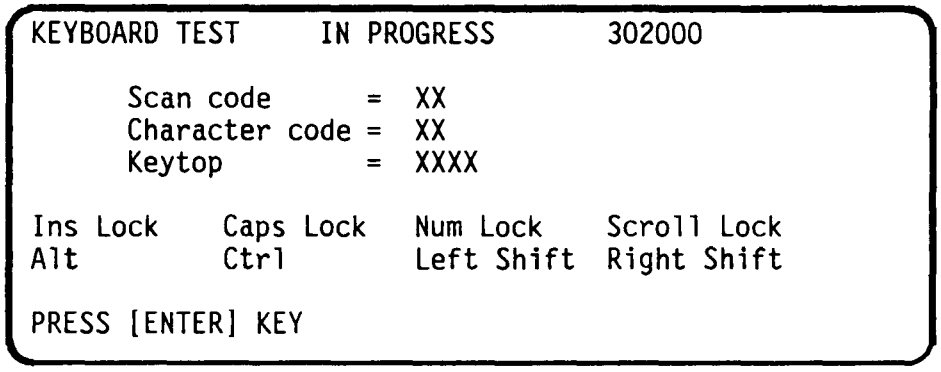


TABLE 3-2 Scan Code, Character Code, and Key Top Names

KEY TOP	SCAN CODE	CHARACTER CODE
'	29	60
1	02	31
2	03	32
3	04	33
4	05	34
5	06	35
6	07	36
7	08	37
8	09	38
9	0A	39
0	0B	30
-	0C	2D
=	0D	3D
\	2B	5C
←-	0E	08
-→	0F	09
q	10	71
w	11	77
e	12	65
r	13	72
t	14	74
y	15	79
u	16	75
i	17	69
o	18	6F
p	19	70
[	1A	5B
]	1B	5D
a	1E	61
s	1F	73
d	20	64
f	21	66
g	22	67
h	23	68
j	24	6A
k	25	6B
l	26	6C
;	27	3B

TABLE 3-2 Scan Code, Character Code, and Key Top Name

KEY TOP	SCAN CODE	CHARACTER CODE
,	28	27
z	2C	7A
x	2D	78
c	2E	63
v	2F	76
b	30	62
n	31	6E
m	32	6D
,	33	2C
.	34	2E
/	35	2F
Space	39	20
F2	3C	00
F4	3E	00
F6	40	00
F8	42	00
F10	44	00
F1	3B	00
F3	3D	00
F5	3F	00
F7	41	00
F9	43	00
Esc	01	1B
Home	47	00
←	4B	00
End	4F	00
Uper	48	00
Lower	50	00
Pg Up	49	00
→	4D	00
Pg Dn	51	00
Del	53	00
Sys Req	85	00
Prt Sc	37	2A
-	4A	2D
+	4E	2B

3.7 DISPLAY TEST

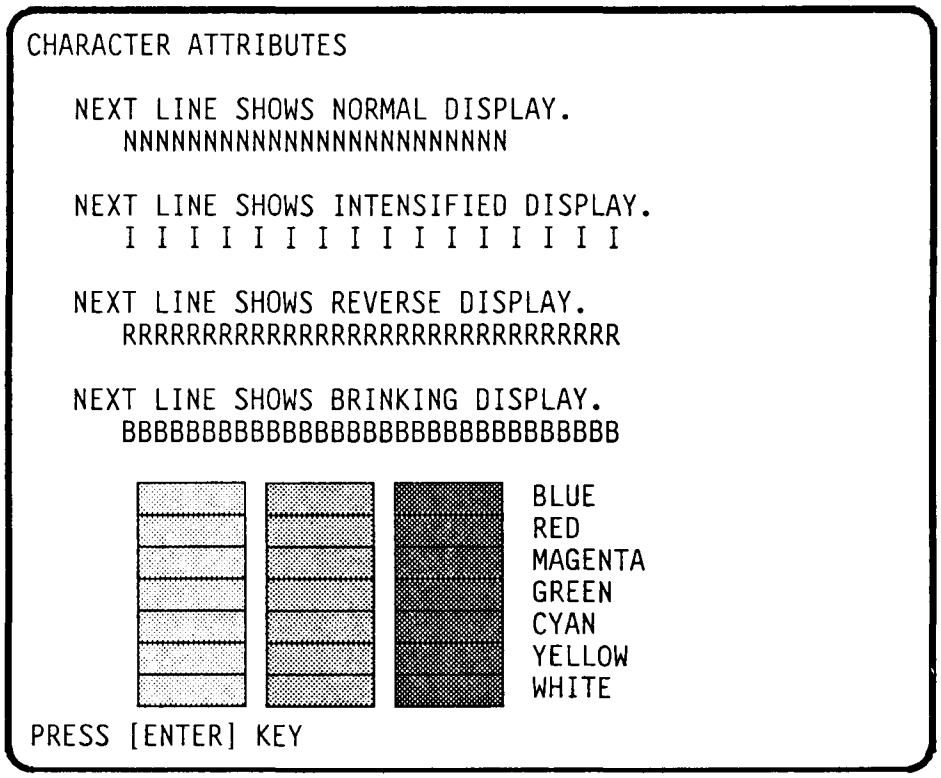
Subtest 01 VRAM read/write (Execution time: 1 second)

This test writes constant data (FFFFH, AAAAH, 5555H, 0000H) and address data to the video RAM (256 kbytes) and SRAM (2 kbytes); it then reads the data out and compares it the original data.

Subtest 02 Character attributes (Execution time: 1 second)

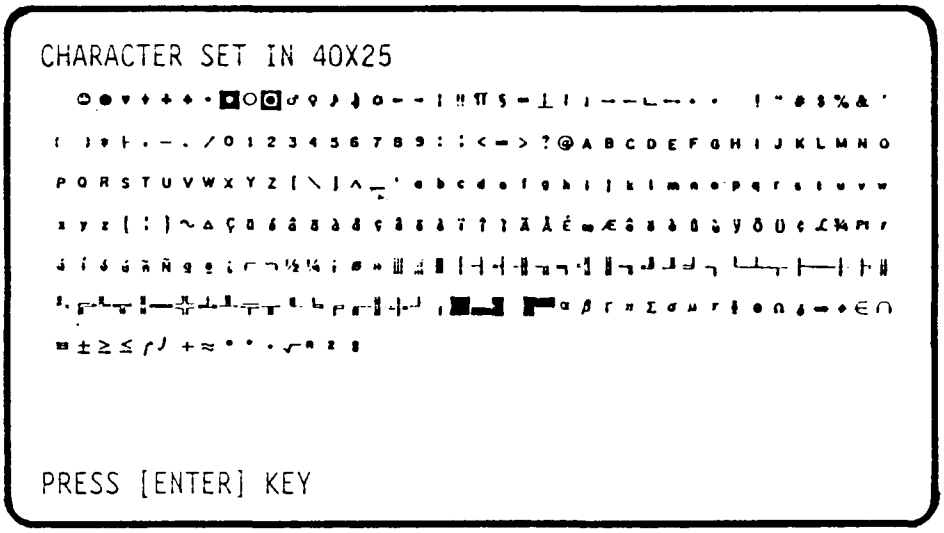
This test is for checking the various types of displays:

Normal Display
Intensified Display
Reverse Display
Blinking Display
In the case of color displays, all seven colors used (blue, red, magenta, green, cyan, yellow, white) are displayed. The background and foreground colors can then be checked for brightness. The display below appears on the screen when this test is run.



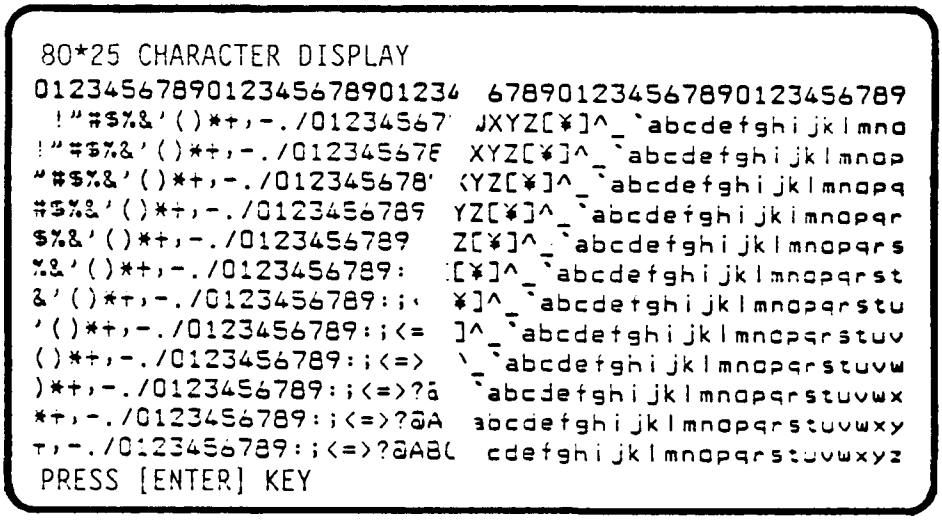
Subtest 03 Character set (Execution time: 1 second)

In this test the character code (00H to FFH) characters are displayed in the 40 x 25 pixel mode as shown below.



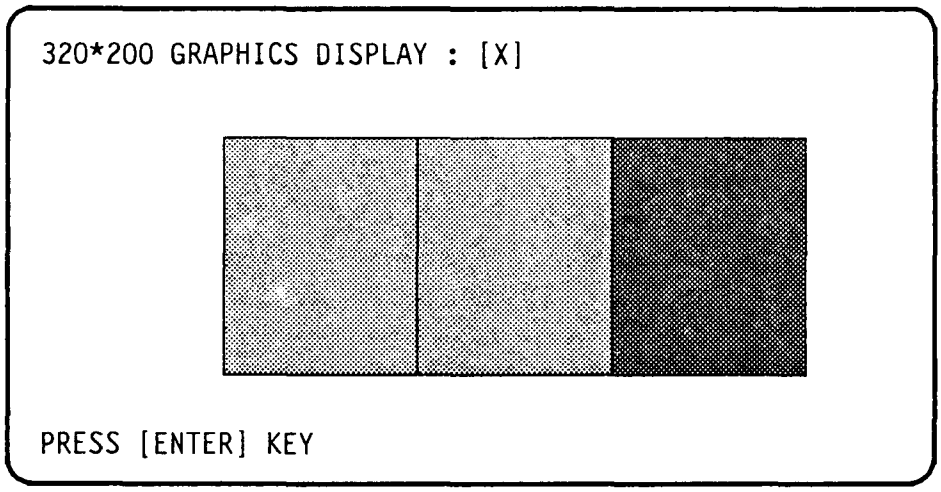
Subtest 04 80*25 Character display (Execution time: 1 second)

In this test the shift caracters are displayed in the 80 x 25 pixel mode as shown below.



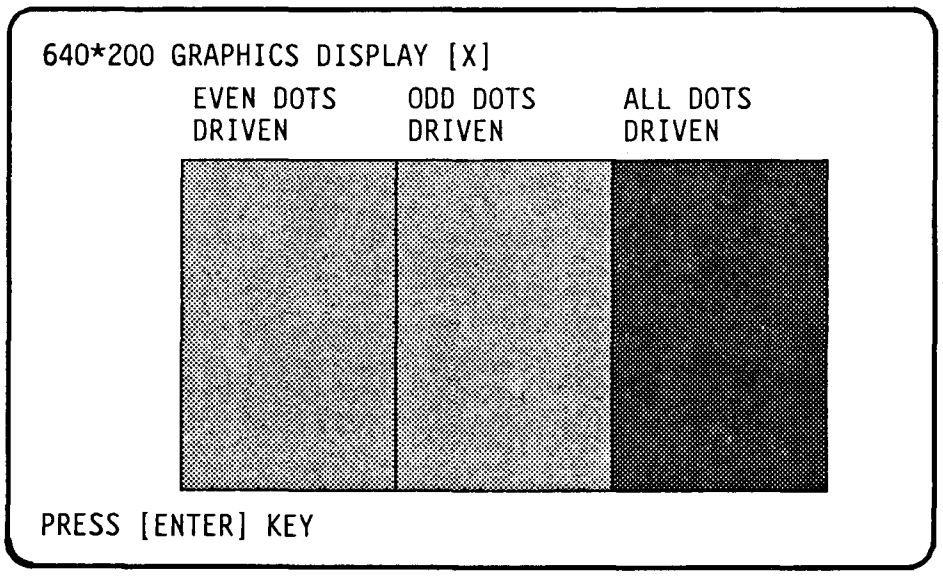
Subtest 05 320*200 Graphics display (Execution time: 3 seconds)

This test displays two sets of color blocks for the color display in the 320 x 200 dots graphics mode (Mode 4 and D) as shown below.
Color set 0: Green, red, yellow
Color set 1: Cyan, Magenta, White



Subtest 06 640*200 Graphics display (Execution time: 3 seconds)

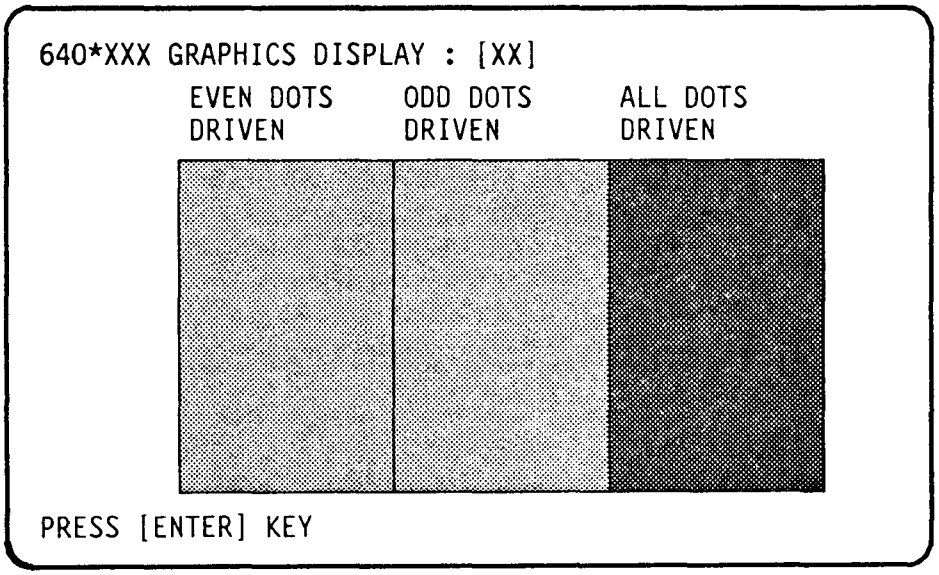
This test displays the color blocks for the black and white display in the 640 x 200 dot graphics mode (Mode 6 and E) as shown below.



Subtest 07 640 x 400 Graphics display (Execution time: 5 seconds)

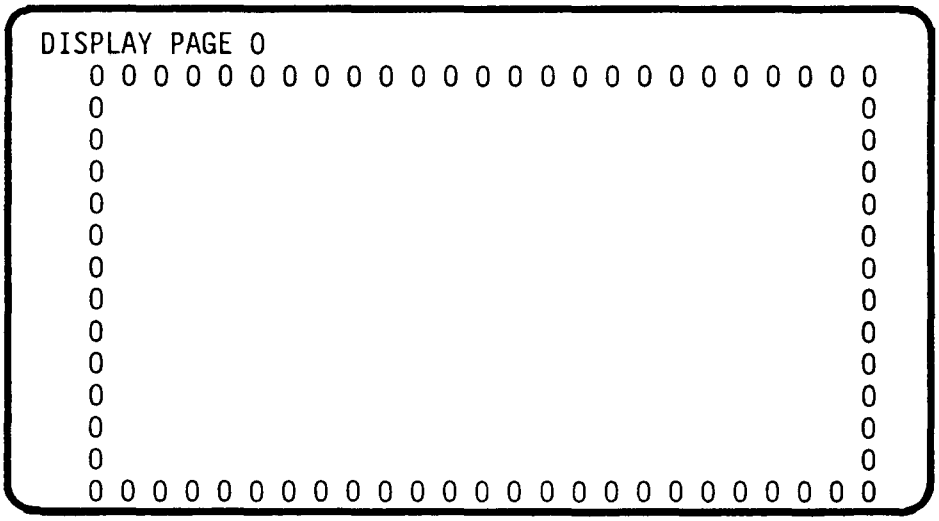
This test displays the color blocks for the black and white display in the 640 x 350 and 640 x 400 dot graphics mode (Mode 10/ 74) as shown below.

Note: Mode 74 is not applicable when the external display is selected.



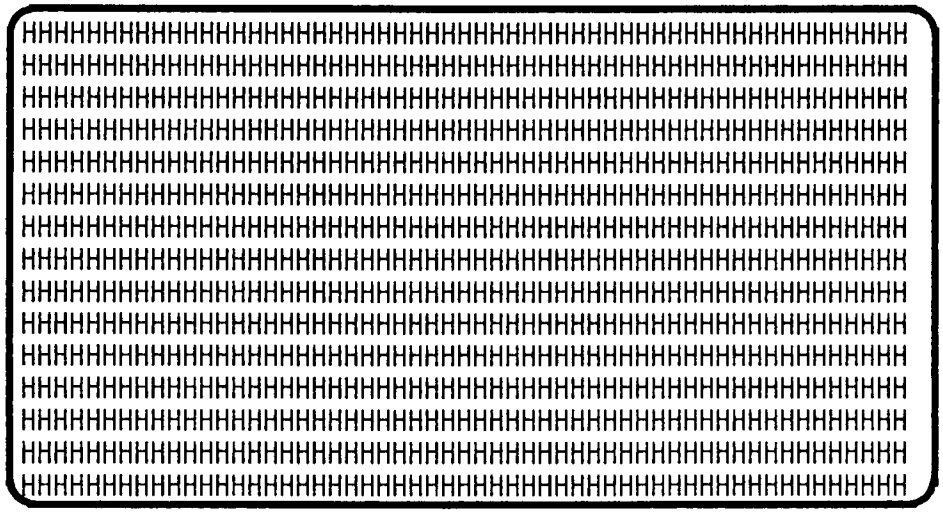
Subtest 08 Display page (Execution time: 15 seconds)

This test confirms that the pages can be changed in order (page 0 to page 7) in the 40 x 25 pixel mode.



Subtest 09 "H" pattern display

This test displays H characters on the entire screen, as shown below.



Subtest 10 Special attribute test

This test displays the following display.

```
[ CRT/Caps/Num/Scroll LED test ]

   (1) Press [ Caps Lock ] key!  ...Caps (on/off)
   (2) Press [ Num lock ]  key!  ...Num (on/off)
   (3) Press [Scroll lock ] key! ...Scroll (on/off)
   (4) Press [ Fn + End ]  key!  ...CRT (on)
   (5) Press [ Fn + Home ] key!  ...CRT (off)


Press [ENTER] KEY
```

3.8 FLOPPY DISK TEST

CAUTION: Before running the floppy disk test prepare a formatted work disk and remove the diagnostics disk then insert the work disk to the FDD.

Subtest 01 Sequential read (Execution time: 50 seconds)

This test performs a cyclic redundancy check with a continuous read operation of all track on a floppy disk.
2D (Double-sided, double density): Track 0 to 39
2DD (Double-sided, double density, double track): Track 0 to 79

Subtest 02 Sequential read/write (Execution time: 115 seconds)

This test writes data to all tracks (as defined above) continuously and then reads the data out and compares it to original data.
(The data pattern is B5ADADH repeated.)

Subtest 03 Random address/data (Execution time: 12 seconds)

This test writes random data to random address on all tracks (as defined in subtest 01) and then reads the data out and compares it with the original data.

Subtest 04 Write specified address (Execution time: 1 second)

This test writes data specified by keyboard to tracks, heads, and address specified by the keyboard.

Subtest 05 Read specified address (Execution time: 1 second)

This test reads data from tracks, heads, and address specified by keyboard.

3.9 PRINTER TEST

CAUTION: A printer (IBM compatible) must be looked up to the system in order to execute the test.

Subtest 01 Ripple pattern (Execution time: 110 seconds)

This test prints character for code 20H through 7EH line by line while shifting one character to the right at the beginning of each new line.

```
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcde
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcder
"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefg
#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefgh
$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefgh
%&'()*+,-./01
&'()*+
'
```

Subtest 02 Function (Execution time: 15 seconds)

This test prints out various print type as shown below.

Normal Print	Double Width Print
Compressed Print	Emphasized Print
Double Strike Print	All Characters Print

```
   PRINTER TEST
1.  THIS LINES SHOWS NORMAL PRINT.
2.    THIS LINE SHOWS DOUBLE WIDTH PRINT.
3.  THIS LINE SHOWS COMPRESSED PRINT.
4.  THIS LINE SHOWS EMPASIZED PRINT.
5.  THIS LINE SHOWS DOUBLE STRIKE PRINT.
  ALL CHARACTERS PRINT

 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_ abcdefghijklmn
opqrstuvwxyz{|}~
```

Subtest 03 Wrap around (Execution time: 1 second)

Note: A printer wraparound connector is necessary for executing this test. Wiring diagram of the printer wrap around connector described in the part 3.24.

Checks the data, control, and status lines with the printer wrap around connector.
Operations for the test is as follows.

1. After type the channel number, the following message will appear.

   [[[Change DIPSW-2 = ON]]] ?

2. Turn the DIP switch-2 on, then press Enter.

3. After finnished the test, turn the DIP switch-2 off.

3.10 ASYNC TEST

For subtest 01 to subtest 05, transmission is done as follows in the communication.

Speed: 9600 BPS
Data: 8 bits + parity (EVEN)
1 stop bit
20H to 7EH

Subtest 01 Wrap around (channel 1) (Execution time: 1 second)

Note: An RS232C wrap around connector must be connected to channel 1 to execute this test. RS232C wrap around connector wiring diagram described in part 3.24.

Performs a data send/receive test with the wrap around connector for the channel 1.

Subtest 02 Wrap around (channel 2) (Execution time: 1 second)

Performs the same test as subtest 01 for the channel 2.

Subtest 03 Point to point (send) (Execution time: 1 second)

Note: This test can be executed on condition that the both send and receive sides are set in the same condition, and also connected together by RS232C direct cable (Wiring diagram described in part 3.22.). Subtest 03 must be executed together with subtest 04 and vice versa.

In this test, the data (20H to 7EH) are sent as one block from one side to the other, and then returned from the later one to the first side again.
This test is used to check wheter the returned data are same as the original ones.

Subtest 04 Point to point (receive) (Execution time: 1 second)

This test is exactly the same as subtest 03 except that the data flow is completely opposite.

Subtest 05 300/1200 BPS card modem loopback (Execution time: 5 seconds)

Note: If there is no modem card in the system, this test can not be executed.

This test is used to check whether the data, which is from the modem to the RS232C inside the system, is same as the original data which had first been sent to the modem card.

Subtest 06 Card modem on-line test (Execution time: 10 seconds)

Note: After the system is connected to the PBX, unless the receive side is in the same status as the send side, the test cannot be executed.

In this test, first some data are sent to the modem card from the RS232C inside the system, then the data is again sent to the other system through the PBX (Private Branch Exchange).
This test is used whether the returned data from the other system are same as the original data.

Subtest 07 Dial tester test (Execution time: 60 seconds)

Note: To execute this test, a dial tester must be connected to the system.

This test is carried out by sending the pulse dial and tone dial twice automatically.

[Pulse dial]: "1-2-3-4-5-6-7-8-9-0-1-2"
[Tone dial]: "1-2-3-4-5-6-7-8-9-*-0-#"

3.11 HARD DISK TEST

CAUTION: The contents of the hard disk will be erased when subtest 02, 03, 04, 06, 08 and 09 is run. Before running the test, transfer the contents of the hard disk on the floppy disk. This can be done with the MS-DOS BACKUP command. After the test, enter the MS-DOS FDISK command, which will set the partition. Then enter the MS-DOS FORMAT command. (See the MS-DOS manual for details.)

Subtest 01 Sequential read (CYL.0-614,CYL.614-0) (Execution time: 8.5 minutes)

This test performs forward reading of contents from track 0 to track 610 and then performs reverse reading of the contents from track 610 to track 0.

Subtest 02 Address uniquence (Execution time: 13 minutes)

This test writes the address data(sector by sector) track by track, then reads the data and compares it to the original data.
Following three kinds of read operations are performed.
(Forward sequential, Reverse sequential, Random)

Subtest 03 Random address/data (Execution time 30 seconds)

This test write random data in random units to random address (cylinder, head, sector) and then reads the data out and compares it to the original data.

Subtest 04 Cross talk & peak shift (Execution time: 13 minutes)

This test writes the eight types of worst pattern data (shown below) to cylinders then reads the data while shifting cylinder by cylinder.

Worst pattern data
1. B5ADAD .....
2. 4A5252 .....
3. EB6DB6 .....
4. 149249 .....
5. 63B63B .....
6. 9C49C4 .....
7. 2DB6DB .....
8. D24924 .....

Subtest 05 Write/Read/Compare (CE) (Execution time: 2 seconds)

This test writes B5ADAD worst pattern data to the CE cylinder and then reads the data out and compares it to the original data.

Subtest 06 Write specified address (Execution time: 1 second)

This test writes specified data to a specified cylinder and head.

Subtest 07 Read specified address (Execution time: 1 second)

This test reads data which has been written to a specified cylinder and head.

Subtest 08 ECC circuit (CE cylinder) (Execution time: 2 seconds)

This test checks the ECC (Error check and correction) circuit functions to a specified cylinder and head.

Subtest 09 Sequential write

This test writes specified data of the two bytes to all cylinder.

3.12 REAL TIMER TEST

Subtest 01 Real time

A new data and time can be input during this test when the current data and time are displayed. Operations for the test is as follows.

1. After executing the test, the following message will appear.

```
REAL TIME TEST                          901000

   Current date:  XX-XX-XXXX
   Current time:  XX:XX:XX

   Enter new date:

PRESS [ENTER] KEY TO EXIT TEST
```

2. If current date is not correct, input the current new date. Press the Enter, the **Enter new time:** message will appear.

3. If current time is not correct, input the current new time. Press the Enter, return to the subtest menu of the REAL TIME TEST.

Subtest 02 Backup memory (Execution time: 1 second)

This test writes data (FFH, AAH, 55H, 00H) to 64 bytes of the backup memory, and then reads and compares it with the original data.

Subtest 03 Real time carry

CAUTION: When this test is executed, the current data and time is erased.

This test checks whether the real-time clock increments the time displayed correctly (month, day, year, hour, minute, second).

3.13 NDP TEST

Note: This test cannot be run if there is no NDP mounted on the system PCB.

Subtest 01 NDP test (Execution time: 1 second)

This test checks the control word, status word, bus, and addition/multiplication functions.

3.14 EXPANSION UNIT TEST

Note: If there is no expansion box connected to the system, this test cannot be executed.

Subtest 01 Box wrap around (8 bits bus) (Execution time: 3 seconds)

Note: As this test required a special tool to be executed, it can not be carried out here.

Subtest 02 Box mono video ram (Execution time: 1 second)

Note: If there is no monochrome display card in the expansion box, this test cannot be executed.

This test writes data (FF, AA, 55, 00H) into the monochrome display memory (B0000H to B0F9FH), then reads the data out and compares it to the original data.

Subtest 03 Wrap around test (16 bit bus)

Note: As this test required a special tool to be executed, it can not be carried out here.

3.15 ERROR CODE AND ERROR STATUS NAMES

The following table shows the error code and error status names.

TABLE 3-3 Error Code and Error Status Names

DEVICE NAME	ERROR CODE	ERROR STATUS NAME
EVERYTHING	FF	Compare error
SYSTEM	01	ROM Checksum Error
MEMORY	01	Parity Error
	02	PROTECTED MODE NOT CHANGE ERROR
FDD	01	Bad Command
	02	Address Mark Not Found
	03	Write Protected
	04	Record Not Found
	06	Media removed on dual attach card
	08	DMA Overrun Error
	09	DMA Boundary Error
	10	CRC Error
	20	FDC Error
	40	SEEK ERROR
	60	FDD not drive
	80	Time Out Error (Not Ready)
	EE	Write buffer error
RS232C	01	DSR Off Time Out
	02	CTS Off Time Out
	04	RX EMPTY Time Out
	08	TX BUFFER FULL Time Out
	10	Parity Error
	20	Framing Error
	40	Overrun Error
	80	Line Status Error
	88	Modem Status Error
	33	NO CARRIER (CARD MODEM)
	34	ERROR (CARD MODEM)
	36	NO DIAL TONE (CARD MODEM)
PRINTER	01	Time Out
	08	Fault
	10	Select Line
	20	Out Of Paper
	40	Power off
	80	Busy Line

TABLE 3-3 Error Code and Error Status Names

DEVICE NAME	ERROR CODE	ERROR STATUS NAME
HDD	01	Bad command error
	02	Bad address mark
	04	Record not found
	05	HDC NOT RESET
	07	Drive not initialize
	09	DMA Boundary error
	0A	Bad sector error
	0B	Bad track error
	10	ECC error
	11	ECC recover enable
	20	HDC error
	40	Seek error
	80	Time out error
	AA	Drive not ready
	BB	Undefined
	CC	Write fault
	E0	Status error
	F0	Not sense error (HW.code = FF)
NDP	01	No NDP
	02	Control word error
	03	Status word error
	04	Bus error
	05	Addition error
	06	Multiplication error

3.16 HARD DISK FORMAT

There are two types of hard disk formatting:

1. Physical formatting
2. Logical formatting

This program is for physical formatting of the hard disk; it can execute the following items.

1. All track FORMAT
2. Good track FORMAT
3. Bad track FORMAT
4. Bad track CHECK

Note: Execution of the program cannot be performed unless the HDD switch is on.

CAUTION: The contents of the hard disk will be erased when this program is run. Before running the program, transfer the contents of the hard disk on to a floppy disk. This can be done with the MS-DOS BACKUP command. (See the MS-DOS manual for details.)

3.16.1 Program description

1. **All track FORMAT** (Execution time: 15 minutes)
   Performs physical formatting of hard disk in the manner shown below.

Sector sequences:	3
Cylinders:	0 to 614
Heads:	0 to 7
Sectors:	1 to 17
Sector length:	512 bytes per sector
Bad track:	MAX. 51 tracks

2. **Good track FORMAT** (Execution time: 1 second)
   Executes the formatting of a specified cylinder and track as a good track.

3. **Bad track FORMAT** (Execution time: 1 second)
   Executes the formatting of a specified cylinder and track as a bad track.

4. **Bad track CHECK** (Execution time: 1 and 1/2 minutes)
   Checks for bad tracks by performing a read operation for all tracks on the hard disk; a list of bad tracks is then displayed.

3.16.2 Operations

CAUTION: After physical formatting is finished, enter the MS-DOS FDISK command, which will set the partition. Then enter the MS-DOS FORMAT command. (See the MS-DOS manual for details.)

1. After pressing 2 and Enter to select from the DIAGNOSTICS MENU, the following display will appear.

```
DIAGNOSTIC - HARD DISK FORMAT: V1.0
  1 - All track FORMAT
  2 - Good track FORMAT
  3 - Bad track FORMAT
  4 - Bad track CHECK
  9 - Exit to DIAGNOSTICS MENU

Press [NUMBER] key ?
```

2. **All track FORMAT** Selection

   (1) When **All track FORMAT** (1) is selected, the following message will appear.

   Interleave number (3/1-9) ?

   (2) Select an interleave number. (Usually select 3.) Type the number and press Enter. The following message will appear.

   Drive number select (1:#1, 2:#2) ?

   (3) Select a drive number. Type the drive number and press Enter. The following display will appear.

```
[HDD TYPE] : CYLINDER   = XXX
[HDD TYPE] : HEAD       = X
[HDD TYPE] : SECTOR     = XX


[WARNING : Current DISK data will be
         completely destroyed]

                              [[cylinder,head = XXX X]]
```

(4) After checking all cylinders of the hard disk, the following message will appear. If found the bad track, the following message will appear.

Press [Bad track number (CCCH) key ?

(5) If the hard disk has the bad track except the displayed number, type a bad-track number (four digits) and press Enter. (The first three digits are the cylinder number and the last digit is the head number.) If there is a bad track on the hard disk, press the Enter only. This executes the formatting of all tracks.

(6) After formatting the hard disk, the **[[cylinder, head = XXX X]]** message will appear; then all cylinders of the hard disk are checked. If there is a bad track on the hard disk, the bad track number will be displayed on the screen.

(7) **Format complete** message will then appear.

(8) Press the Enter to return to the HARD DISK FORMAT menu.

3. **Good track FORMAT** or **Bad track FORMAT** Selection

(1) When **Good track FORMAT** or **Bad track FORMAT** is selected, the following message will appear.

Interleave number (3/1-9) ?

(2) Select an interleave number. (Usually select 3.) Type the number and press Enter. The following message will appear.

Drive number select (1:#1, 2:#2) ?

(3) Select a drive number. Type the drive number and press Enter. The following message will appear.

```
[HDD TYPE] : CYLINDER   = XXX
[HDD TYPE] : HEAD       = X
[HDD TYPE] : SECTOR     = XX


Press [Track Number (CCCH)] key ?
```

(4) Type a track number (four digits) and press Enter. (The first three digits are the cylinder number and the last digit is the head number.) This executes the formatting of good tracks or bad tracks.

Note: This program can format only one track per operation. If it is desired to format several good tracks or bad tracks, repeat the operation as many times as nessary.

(5) After formatting the track of the hard disk, the **Format complete** message will appear.

(6) Press the Enter to return to the HARD DISK FORMAT menu.

4. **Bad track CHECK** Selection

(1) When **Bad track CHECK** is selected, the following message will appear.

Drive number select (1:#1, 2:#2) ?

(2) Select a drive number. Type the drive number and press Enter. When the following message appears, and bad tracks of the hard disk are checked.

```
[HDD TYPE] : CYLINDER   = XXX
[HDD TYPE] : HEAD       = X
[HDD TYPE] : SECTOR     = XX


                              [[cylinder,head = XXX X]]
```

(3) After checking the bad tracks of the hard disk are checked, the **Format complete** message will appear.

(4) Press the Enter to return to the HARD DISK FORMAT menu.

3.17 SEEK TO LANDING ZONE (HDD)

3.17.1 Program description

When moving the unit, if an HDD head touches a data area, the data will be lost. In order to protect the data, this program moves HDD heads to safe areas. Theese areas called "landing zones."

Note: When the built-in T3200 hard disk does not issue a command to the HDD for an interval of 5 seconds, the HDD heads move to a landing zone automatically.

3.17.2 Operations

1. After pressing "3" and Enter to select from the DIAGNOSTICS MENU. The program is then automatically executed and the following message will appear.

```
Landing seek completed. (HDD#1)
Press [enter] key.
```

2. After pressing Enter, return to the DIAGNOSTICS MENU.

3.18 HEAD CLEANING

3.18.1 Program description

This program executes head loading and seek/read operations for head cleaning. A cleaning kit is necessary for cleaning the FDD head.

3.18.2 Operations

1. After pressing 4 and Enter to select from the DIAGNOSTICS MENU, the following message will appear.

```
HEAD CLEANING

Mount cleaning disk(s) on drive(s).
Press any key when ready.
```

2. After above message appears, remove the Diagnostics disk, insert the cleaning disk, and press any key.

3. When the following message appears, FDD head cleaning will begin.

```
HEAD CLEANING

Mount cleaning disk(s) on drive(s).
Press any key when ready.
     Cleaning start
```

4. When cleaning is finished, the display automatically returns to the DIAGNOSTICS MENU.

3.19 LOG UTILITIES

3.18.1 Program description

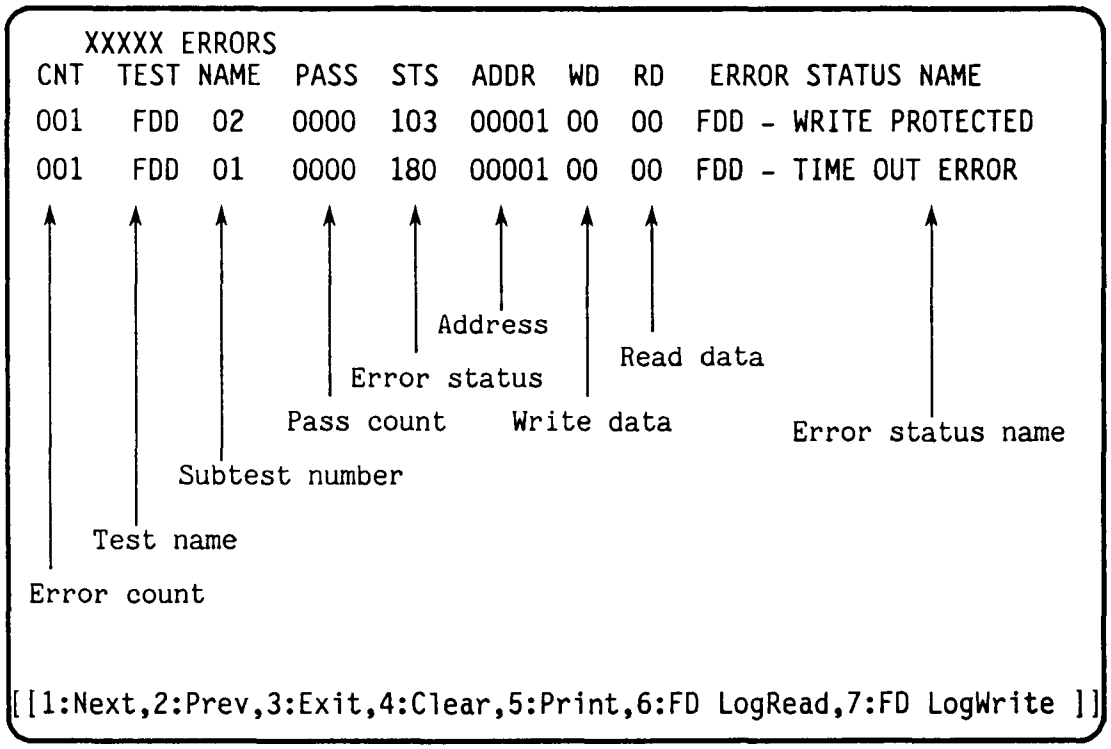
This program logs error information generated, while a test is in progress; the information is stored in the RAM.
However if the POWER switch is turned off the error information will be lost. The error information itself is displayed as the following.

1. Error count (CNT)
2. Test name (TEST)
3. Subtest number (NAME)
4. Pass count (PASS)
5. Error status (STS)
6. Address (FDD, HDD 1 or memory; ADDR)
7. Write data (WD)
8. Read data (RD)
9. Error status name

This program can store data on a floppy disk or output information to a printer.

3.19.2 Operations

1. After pressing 5 and Enter to select from the DIAGNOSTICS MENU, the error information logged in the RAM or on the floppy disk is displayed as shown below.



2. Error information to be displayed on the screen can be manupulated with the following key operation.

   The 1 key scrolls the display to the next page.
   The 2 key scrolls the display to the previous page.
   The 3 key returns the display to the DIAGNOSTIC MENU.
   The 4 key erases all error log information in RAM.
   The 5 key outputs error log information to a printer.
   The 6 key reads log information from a floppy disk.
   The 7 key writes log information to a floppy disk.

3.20 RUNNING TEST

3.20.1 Program description

This program automatically runs the following tests in sequence.

1. System test (subtest number 01)
2. Memory test (subtest number 01, 02, 03, 04, 06)
3. Display test (subtest number 01 to 08)
4. FDD test (subtest number 02)
5. Printer test (subtest number 03)
6. Async test (subtest number 01)
7. HDD test (subtest number 01, 05)
8. Real timer (subtest number 02)

When running an FDD test, this system automatically decides whether there are one or two FDDs.

3.20.2 Operations

CAUTION: Do not forget to load a work disk. If a work disk is not loaded, an error will be generated during FDD testing.

1. Remove the diagnostics disk and insert the work disk into the floppy disk drive.

2. After pressing 6 and Enter to select from the DIAGNOSTIC MENU, the following message will appear.

Printer wrap around test (Y/N) ?

3. Select whether to execute the printer wraparound test (Yes) or not (No). Type the desired Y or N and press Enter key. (If Y is selected, a wraparound connector must be connected to the printer connector on the back of the unit.) The following message will appear.

Async wrap around test (Y/N) ?

4. Select whether to execute the test (Yes) or not (No). Type the desired Y or N and press Enter Key. (If Y is selected, an RS232C wraparound connector must be connected to the COMMS connector on the back of the unit.)

5. This program is repeated continuously. To stop the program, press Ctrl + Break key.

3.21 FDD UTILITIES

3.21.1 Program description

These programs format and copy floppy disks, and display dump list for both the FDD and the HDD.

1. **FORMAT**

This program can format floppy disk (5.25"/3.5") as follows.

(a) **2D:** Two-sided, double-density, 48 TPI, MFM mode, 512 bytes, 9 sectors/track.
(b) **2DD:** Two-sided, double-density, double-track, 96 TPI, MFM mode, 512 bytes, 15 sectors/track.
(c) **2HD:** Two-sided,high-density, double-track, 96/135 TPI, MFM mode, 512 bytes, 15 sectors/track.

2. **COPY**

This program copies floppy disks.

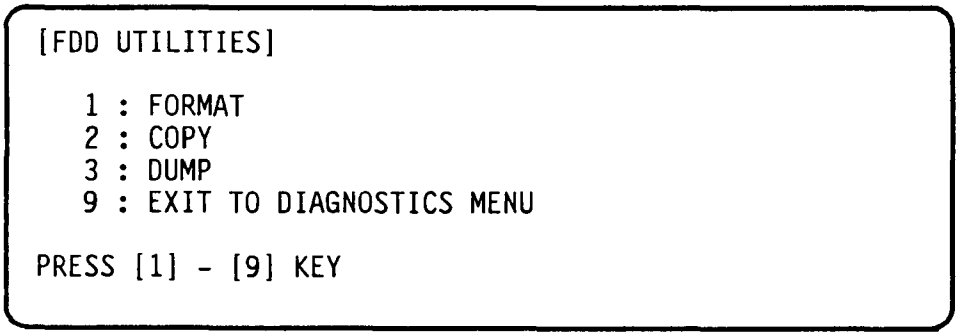
Copy with one FDD (Drive A)
Copy with two FDDs (Drive A to Drive B)

3. **DUMP**

This program display the contents of floppy disks (both 3.5" and 5.25") and hard disks (designated sectors).

3.21.2 Operations

1. After pressing 7 and Enter key to select from the DIAGNOSTICS MENU, the following display will appear before program execution.



2. **FORMAT** Selection

(1) When **FORMAT** is selected, the following message appears.

```
DIAGNOSTICS - FORMAT
Drive number select (1:A, 2:B) ? _
```

(2) Select a drive number. Type the number and the following message will then appear.

Type select (0:2DD-2DD,1:2D-04DE,2:2D-08DE,3:2HD-08DE)

(3) Select a media-drive type number. Type the number and the following message will appear.

```
Warning : Disk data will be destroyed.

Insert work disk in to drive A :
Press any key when ready.
```

(4) Remove the diagnostics disk from the FDD and insert the work disk; press any key.
The **Format start** message will appear; formatting is then executed. After the floppy disk is formatted, the following message will appear.

Format complete
Another format (1:Yes/2:No) ?

(5) If you type 1 and press Enter key, the display will return to the message in (3) above. If you type 2 the display will return to the DIAGNOSTICS MENU.

3. **COPY** Selection

(1) When **COPY** is selected, the following message will appear.

```
DIAGNOSTICS - COPY
Type select (0:2DD-2DD,1:2D-04D,2:2D-08DE,3:2HD-08DE) ?_
```

(2) Select a media/drive type number. Type the number. The following message will then appear.

```
Insert source disk into drive A :
Press any key when ready.
```

(3) Remove the diagnostics disk from the FDD and insert the source disk; press any key. The **Copy started** message will then appear. After that, the following message will appear.

```
Insert target disk into drive A :
Press any key when ready.
```

(4) Remove the source disk from the FDD and insert the work disk (formatted); press any key. When coping can not be done with one operation, message (2) is displayed again. Repeat the operation. After the floppy disk has been copied, the following message will appear.

```
Copy complete
Another copy (1:Yes/2:No) ?
```

(5) If you type 1 the display will return to the message in (1) above. If you type 2 the display will return to the DIAGNOSTICS MENU.

4. **DUMP** Selection

(1) When **DUMP** is selected, the following message will appear.

```
[HDD&FLOPPY DISK DATA DUMP]
format type select (0:2DD,1:2D,2:2HD,3:HDD) ? _
```

(2) Select a format type number. Type the number. If 3 is selected, the dump lists for the hard disk are displayed automatically.

0: Display a dump list for a floppy disk (2DD)
1: Display a dump list for a floppy disk (2D).
2: Display a dump list for a floppy disk (2HD).
3: Displays a dump list for a hard disk.

(3) If 0, 1, or 2 is selected, the following message will appear.

Select FDD number (1:A/2:B) ?

(4) Select an FDD drive number; the following message will then appear.

```
Insert source disk into drive A :
Press any key when ready.
```

(5) Remove the diagnostics disk from the FDD and insert a source disk; press any key. The **Track number ??** message will then appear. Type the track number and press Enter.

(6) The **Head number ?** message will then appear. Type the head number and press Enter.

(7) The **Sector number ??** message will then appear. Type the sector number and press Enter. The dump list for the floppy disk will be displayed.

(8) After a dump list appears on the screen, the **Press number key (1:up,2:down,3:end) ?** message will appear.

1. Displays the next sector dump.
2. Displays a previous sector dump.
3. Displays the following message.

Another dump (1:Yes/2:No) ?

(9) If you type 1 the display will return to the message shown after (4) above. If you type 2 the display will return to the DIAGNOSTICS MENU.

3.22 SYSTEM CONFIGURATION

3.22.1 Program description

This program displays the following system configuration.

1. Memory size
2. Display type
3. Floppy disk drive number
4. Async port number
5. Hard disk drive number
6. Printer port number
7. Co-processor number
8. Extended memory size

3.22.2 Operations

After pressing 8 and Enter key to select from the DIAGNOSTICS MENU, the following display will appear.

```
SYSTEM CONFIGURATION :

* - 640KB MEMORY
* - PLASMA DISPLAY
* - 1 FLOPPY DISK DRIVE(S)
* - 1 ASYNC ADAPTOR
* - 1 HARD DISK DRIVE(S)
* - 1 PRINTER ADAPTOR
* - 0 MATH CO-PROCESSOR
* - XXXXKB EXTENDED MEMORY


PRESS [ENTER] KEY
```

Press Enter key to return to the DIAGNOSTICS MENU.

3.23 SETUP

3.23.1 Program description

This program displays the following items, and then can change it by automatically or manual.

1. Floppy disk drive number and type
2. Hard disk drive number and type
3. System memory size
4. Extended memory size
5. Expanded memory size
6. External display card status

3.23.2 Operations

1. After pressing 0 and Enter to select the DIAGNOSTICS MENU, the following display will appear.

```
[[ System setup ]]
 1. Floppy disk drives     = 1
      drive#1 type         = 2 - 720KB/1.2MB
      drive#2 type         = 0 - No drive

 2. Hard disk drives       = 1
      drive#1 type         = 4- Cyl=614,h=8,S/T=17

 3. Memory size
      System memory        = 640KB
      Extended memory      =   0MB
      Expanded memory      = 384KB +   0MB

 4. External display card  = None



Select setup change (1:no/2:yes) ?
```

2. Select the (yes) or (no). Type the number and press Enter.
   If select (yes), the following message will appear.
   If select (no), load the system again.

3. Select the (auto) or (manual). Type the number and press Enter. If select the (manual), the following message will appear.

```
[ Floppy disk setup ]

     0: No drive
     1: 360KB
     2: 720KB/1.2MB

   (1) Floppy disk drive#1 type = 2 ?
```

4. Select the floppy disk drive#1 type. Type the number and press Enter. (In the case of the floppy disk drivr type is 720KB or 1.2MB, press Enter only.)
The following message will appear.

```
     0: No drive
     1: 360KB
     2: 720KB/1.2MB

   (2) Floppy disk drive#1 type = 0 ?
```

5. Select the floppy disk drive#2 type. Type the number and press Enter. (In the case of the floppy disk drive#2 is no drive, press Enter only.) The following message will appear.

```
[ Hard disk setup ]


   (3) Is hard disk available ? (Y/N)
```

6. Select the (YES) or (NO). Type "Y" or "N" and press the Enter. Return to the SETUP menu.
   Note: If the system has a optional memory card, the following message will appear.

```
[ Extended memory setup ]

   0: No memory
   1: 0.5MB
   2: 1MB
   3: 1.5MB
   4: 2MB
   5: 2.5MB
   6: 3MB


(4) Extended memory size = 06 ? [   3MB]

   (Expanded memory size  [384KB+  0MB])
```

7. Select the expanded memory size. Type the number and press the Enter. Return to the SETUP menu.
   Note: If the DIP switch 5 is ON and the system has a optional display board to the expansion slot, the following message will appear.

```
[External display card type setup]

   1: Color display card (40*25 column)
   2: Color display card (80*25 column)
   3: Monochrome display card
   0: Others

(5) External display type = 0 ?
```

8. Select the external display card type. Type the number and press the Enter. Return to the SETUP menu.

3.24 WIRING DIAGRAM

1. Printer wrap around connector

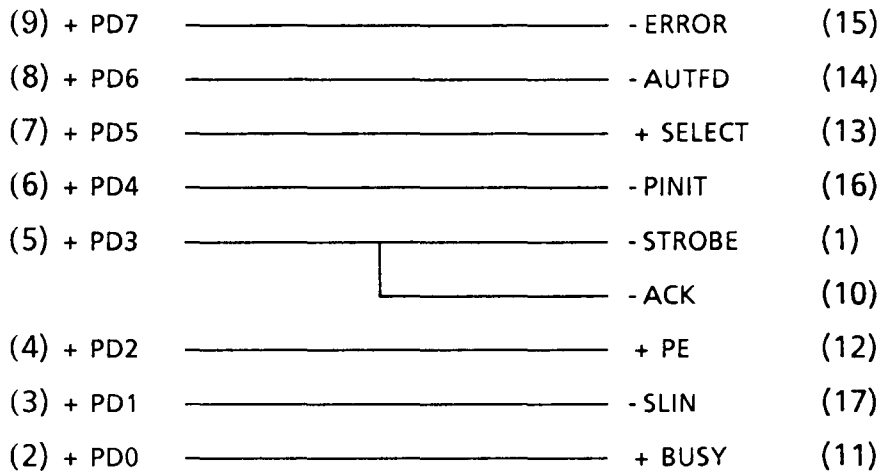


FIGURE 3-1 Printer Wrap Around Connector

2. RS232C Wrap around connector

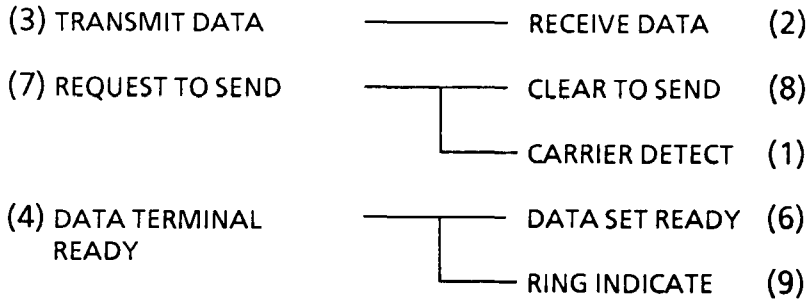


FIGURE 3-2 RS232C Wrap Around Connector

3. RS232C direct cable (9-pin to 9-pin)

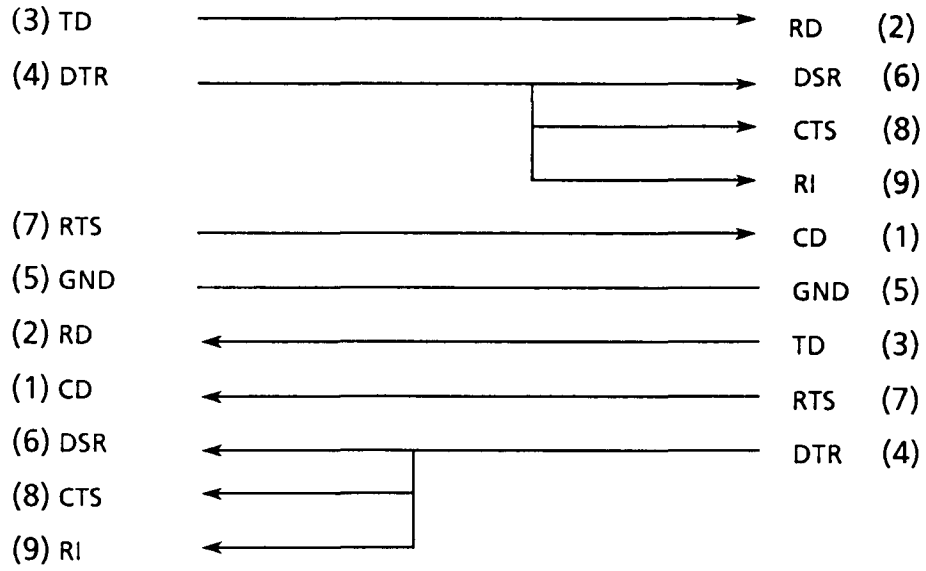


FIGURE 3-3 RS232C Direct Cable (9-pin to 9-pin)

4. RS232C direct cable (9-pin to 25-pin)

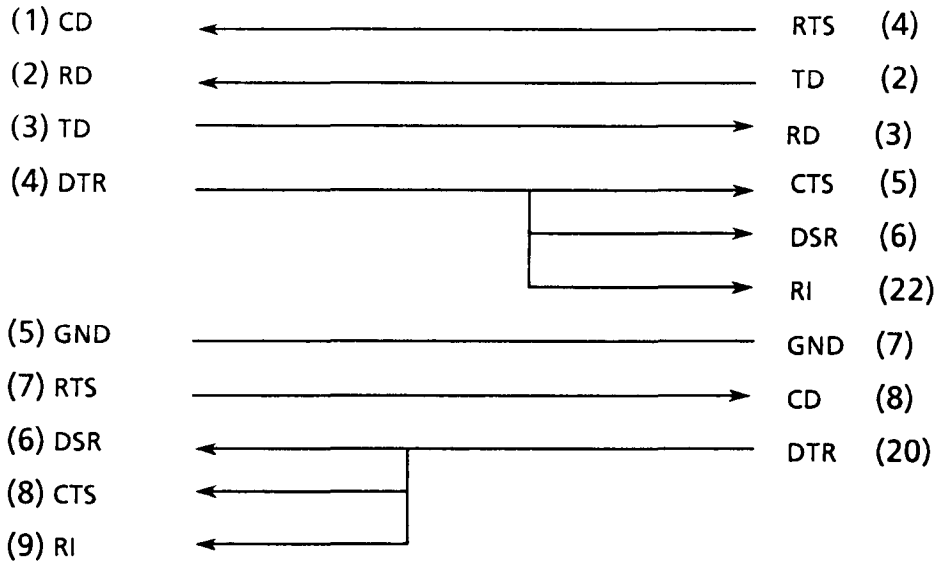


FIGURE 3-4 RS232C Direct Cable (9-pin to 25-pin)

4.1 GENERAL

This section gives a detailed description of the procedures used to replace FRUs (field replaceable units).

FRUs consist of the following:

1. Top Cover
2. PDP (Plasma Display Panel) Mask
3. PDP
4. Indicator PCB
5. Cable Guide
6. PDP Cover Assembly
7. Keyboard Unit
8. Speaker
9. Lithium Battery
10. Power Supply Unit
11. FDD (Floppy Disk Drive)
12. HDD (Hard Disk Drive)
13. Expansion Bus PCB
14. Fan
15. HDC (Hard Disk Control PCB)
16. Syatem PCB

The following points must be kept in mind:

1. The system should never be disassembled unless there is a problem (abnormal operation, etc.)
2. Only approved tools may be used.
3. After deciding the purpose of replacing the unit, and the procedures required, do not carry out any other procedures which are not absolutely necessary.
4. Be sure to turn the POWER switch off before beginning.
5. Be sure to disconnect the ac cord and all external cables from the system.
6. Follow only the fixed, standard procedures.
7. After replacing a unit, confirm that the system is operating normally.

Tools needed for unit replacement:

1. Phillips Screwdriver
2. Bladehead Screwdriver
3. Tweezers

4.2 REMOVING/REPLACING THE TOP COVER

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Turn the unit upside down and pull the handle (A) forward.
3. Remove the five screws (B) from the base assembly (C).

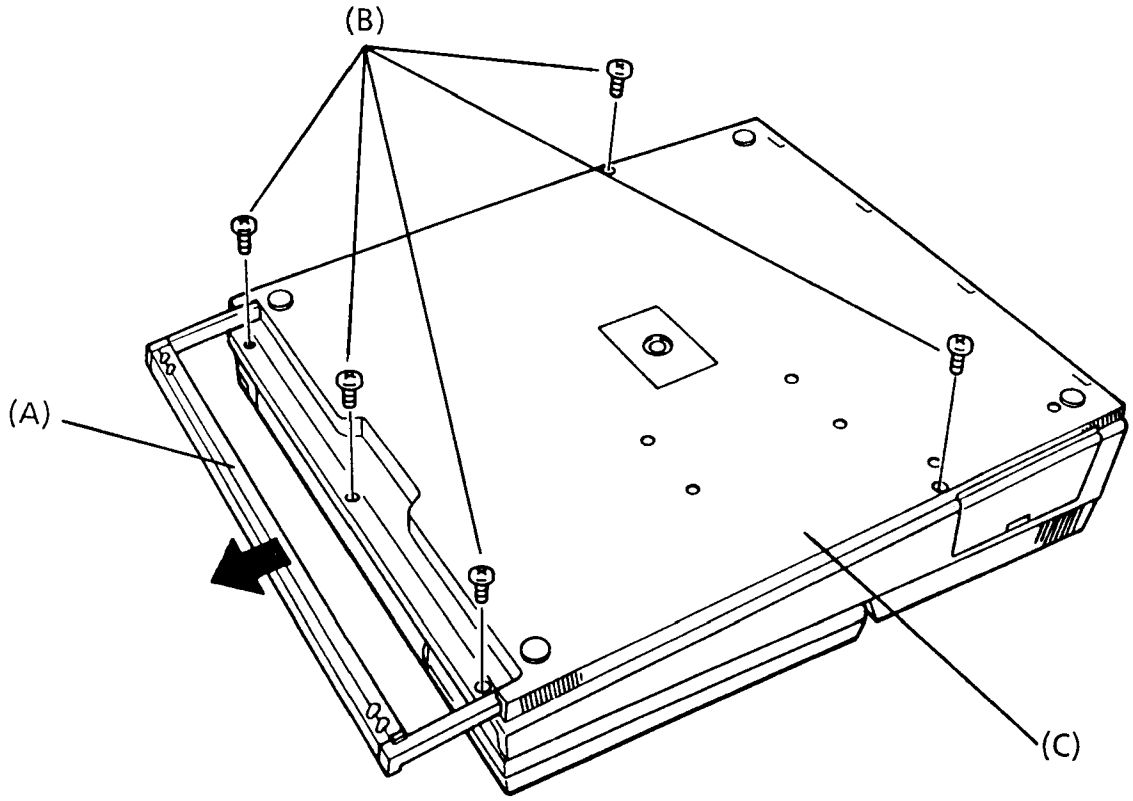


FIGURE 4-1 Removing the Screws from the Base Assembly

4. Turn the unit back over and remove the two screws (D) from the rear panel (E), then remove the rear panel.

5. To remove the support back panel (F), remove the two screws (G) from the support back panel.

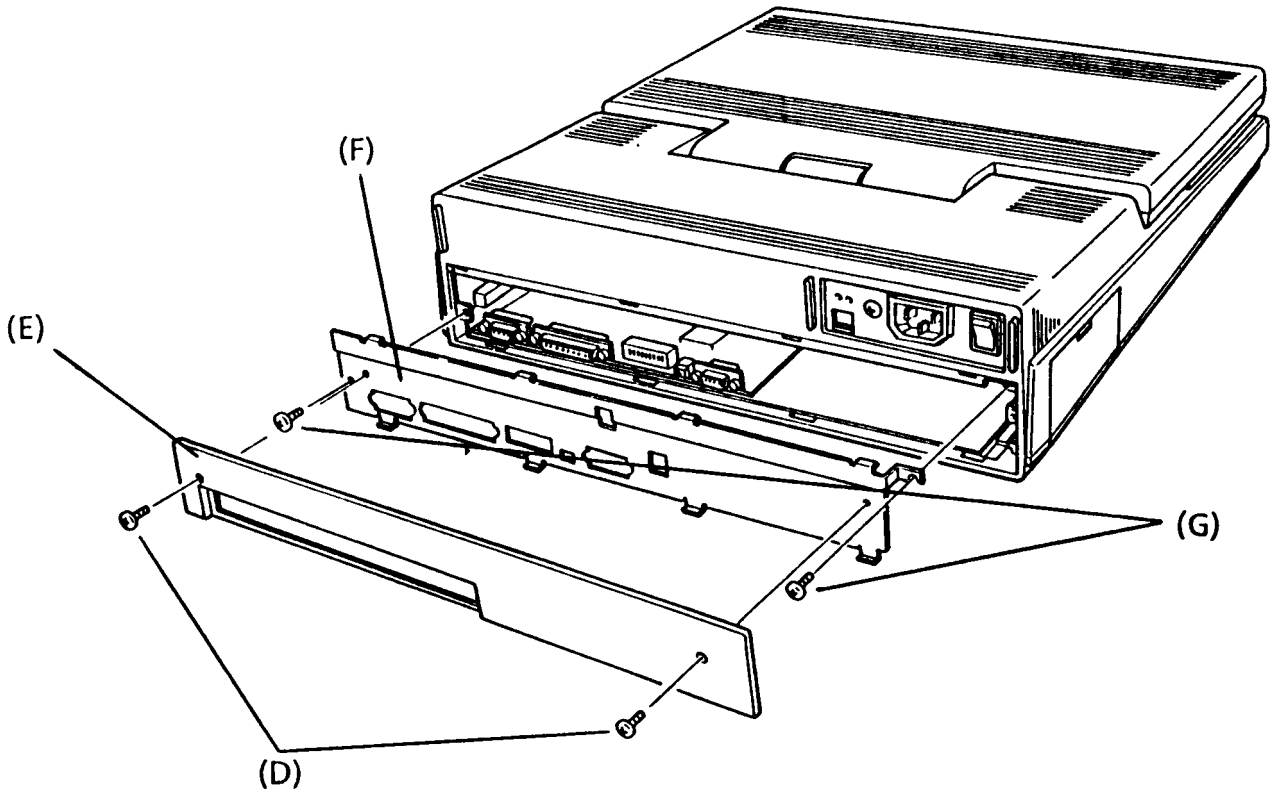


FIGURE 4-2 Removing the Rear Panel and Support Back Panel

6. Open the plasma display, then remove the PDP, the indicator PCB and cable guide as directed in part 4.3, 4.4 and 4.5.

7. Remove the keyboard unit as directed in part 4.7.

8. To remove the top cover (H), pass the four cable (I) through a slit (J) of the top cover.
   At this time, remove the connector panel (K) from the top cover.

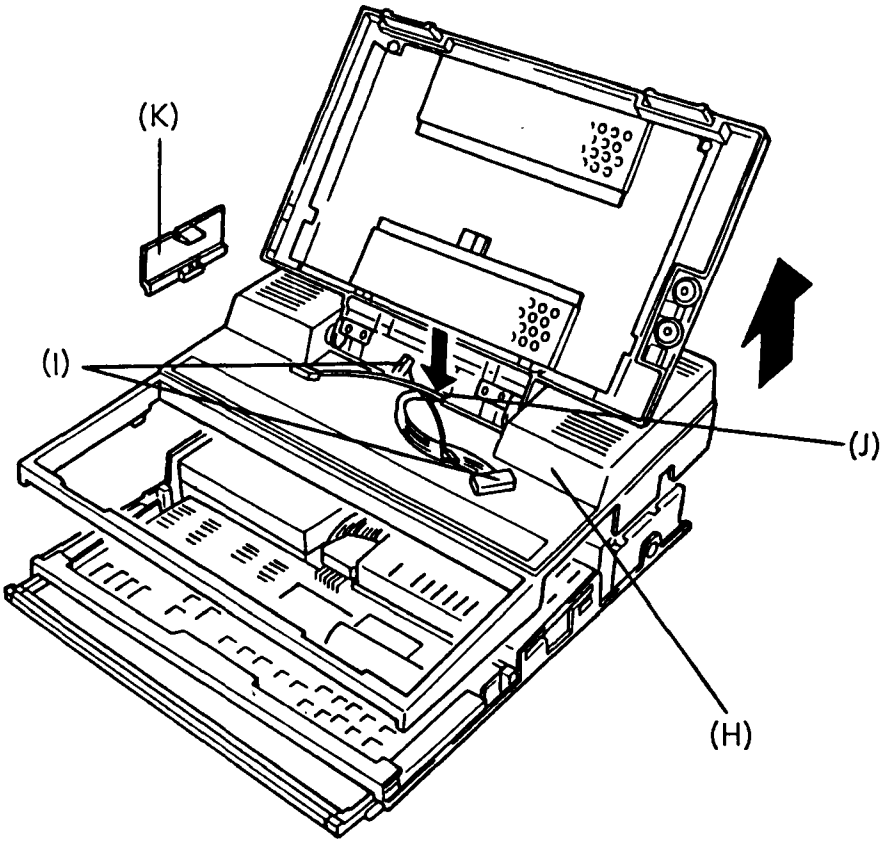


FIGURE 4-3 Removing the Top Cover

9. To install a top cover, follow the above procedures in reverse.

4.3 REMOVING/REPLACING THE PDP MASK

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Open the plasma display.
3. Using tweezers or fine-pointed instruments, peel off the function label (A) and keep it in a clean place.
4. Remove the two screws (B) from the PDP mask (C), then remove the PDP mask pulling it up.

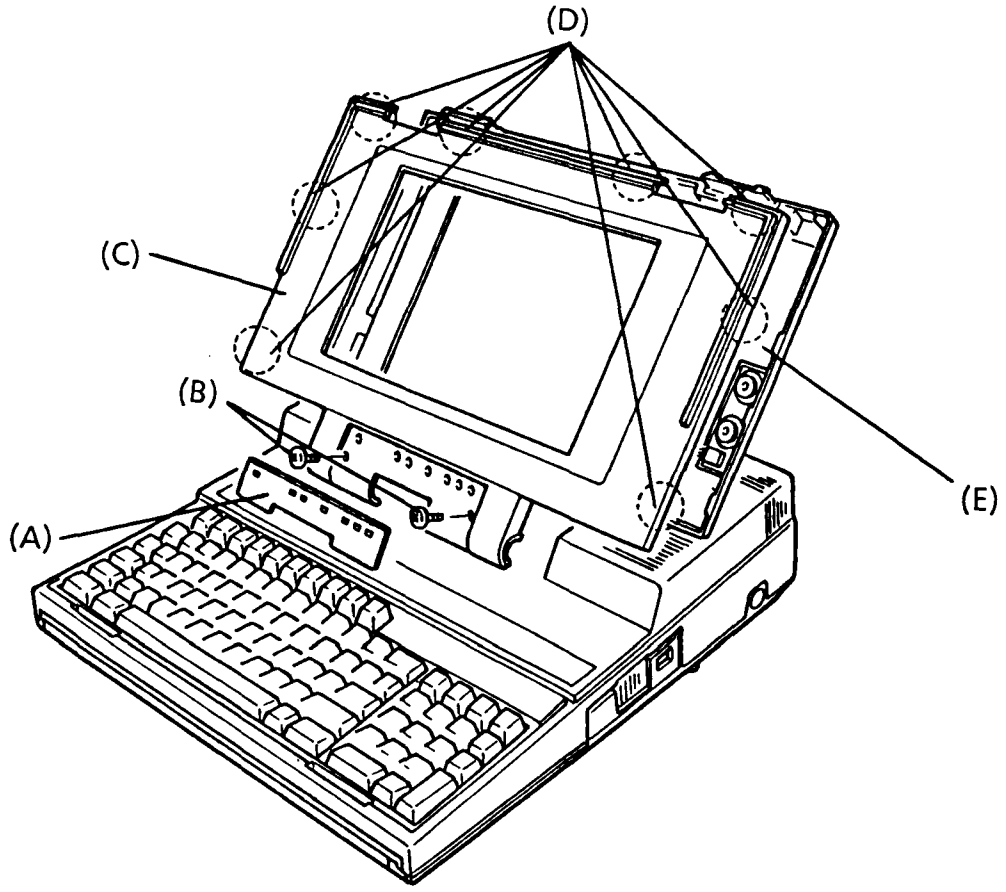


FIGURE 4-4 Removing the PDP Mask

5. To install a new PDP mask, follow the above procedures in reverse.
   Note: Confirm that the eight latches (D) of the PDP cover assembly (E) are inserted into the PDP mask.

4.4 REMOVING/REPLACING THE PDP

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Remove the PDP mask as directed in part 4.3.
3. Remove the four screws (A) on the PDP (B).
4. Lift up the PDP, then put it on the keyboard (C).
5. Disconnect the three cable (D) from the rear of the PDP.

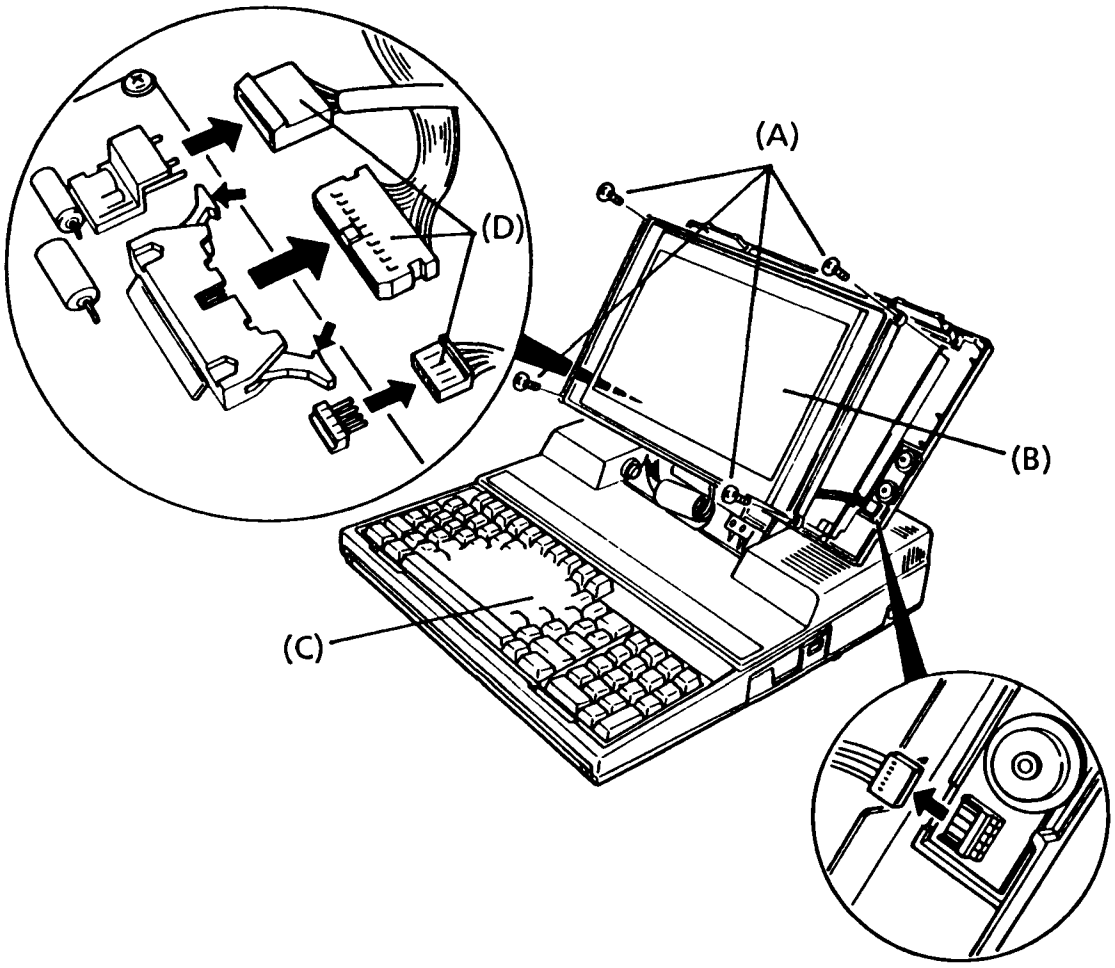


FIGURE 4-5 Removing the PDP

6. To install a PDP, follow the above procedures in reverse.

4.5 REMOVING/REPLACING THE INDICATOR PCB, THE CABLE GUIDE AND THE PLASMA PCB

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Remove the PDP as directed in part 4.4.
3. Pull the ground cable (A) from the PDP cover assembly (B).
4. Lift the indicator PCB (C), then disconnect an indicator cable (D) from the indicator PCB.
4. Take off the indicator cable, ground cable, plasma display power cable (E) and plasma display signal cable (F) from the cable guide (G), then remove the cable guide.
5. To remove the volume PCB (H), remove the single screw (I) from the PDP cover assembly.

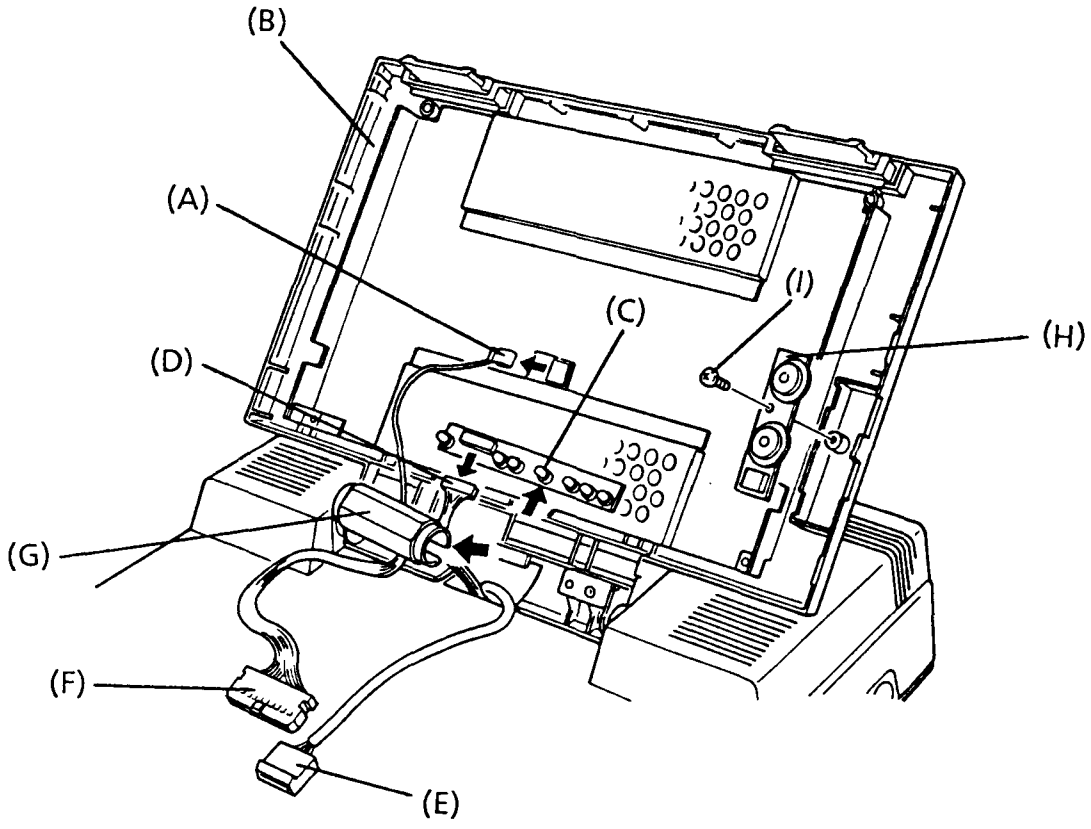


FIGURE 4-6 Removing the Indicator PCB and the Cable Guide

6. To install an indicator PCB and cable guide, follow the previous page procedures in reverse.

Note: When put the four cables through cable guide, be careful as following items.

(1) Put plasma display power cable (J) to your right, and plasma ground cable (K), indicator cable (L) and plasma display signal cable (M) to your left as shown in the figure 4-7.

(2) Position the cable guide so that thicker part (N) comes to the upper side as shown in the figure 4-8.

(3) Put the cable guide in the top cover, then place each cable in the two ditches (O) of the PDP cover assembly as shown in the figure 4-7.

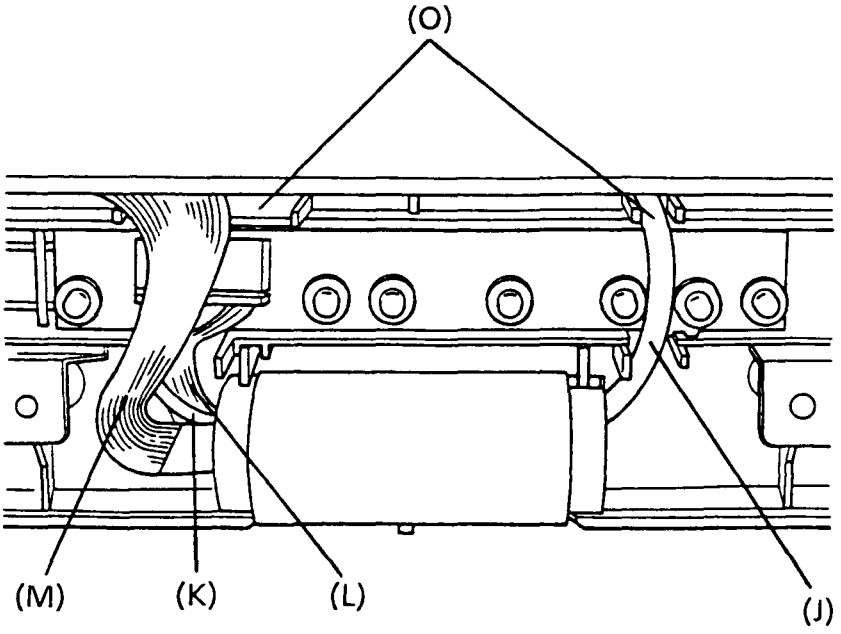


FIGURE 4-7 Cable Position

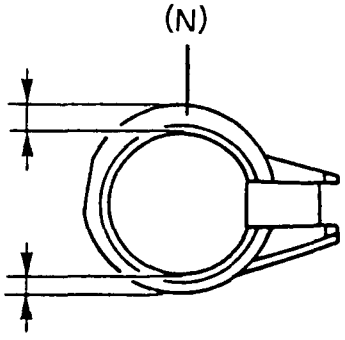


FIGURE 4-8 Cable Guide

4.6 REMOVING/REPLACING THE PDP COVER ASSEMBLY

1. Confirm that the POWER switch is off and unplug the ac coad.
2. Remove the indicator PCB and cable guide as directed in part 4.5.
3. Remove the two screws (A) from the two hinges (B).
4. To remove the PDP cover assembly (C), shift the two hinges to inside, then turn the PDP cover assembly down and lift it up.

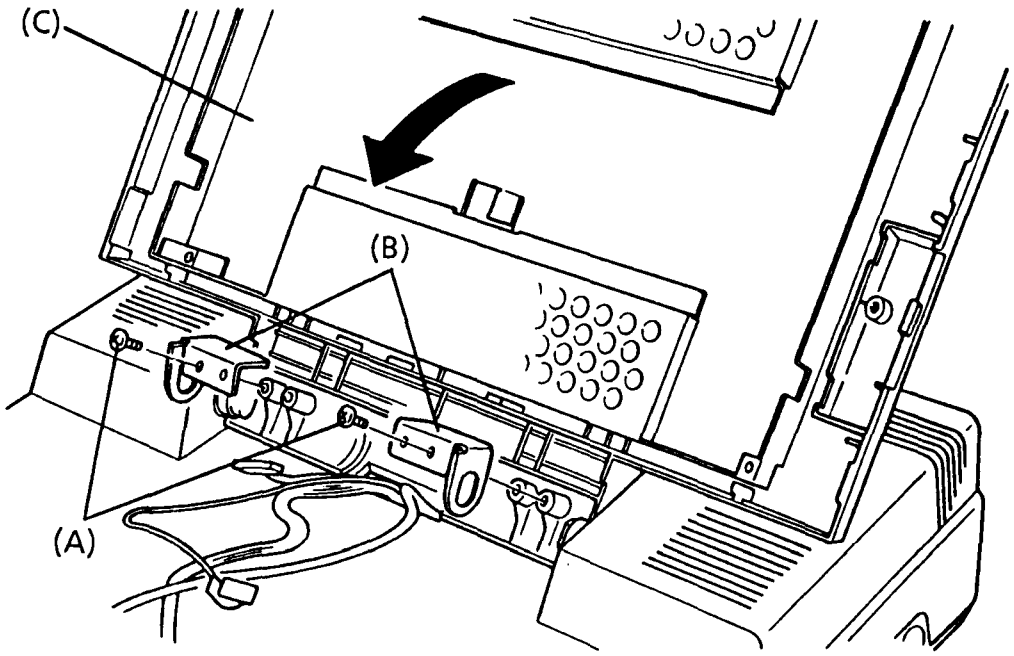


FIGURE 4-9 Removing the PDP Cover Assembly

5. To install a new PDP cover assembly, follow the above procedures in reverse.

4.7 REMOVING/REPLACING THE KEYBOARD UNIT

1. Confirm that the POWER switch is off and unplug the ac cord.

2. Open the plasma display, then remove the two mask panels (A) by using bladehead screwdriver.

3. Remove the two screws (B) located beneath the two mask panels and lift up the keyboard unit (C).

4. Release the pressure plate (D) of connector PJ 3 to disconnect the keyboard cable (E) from the system PCB (F).

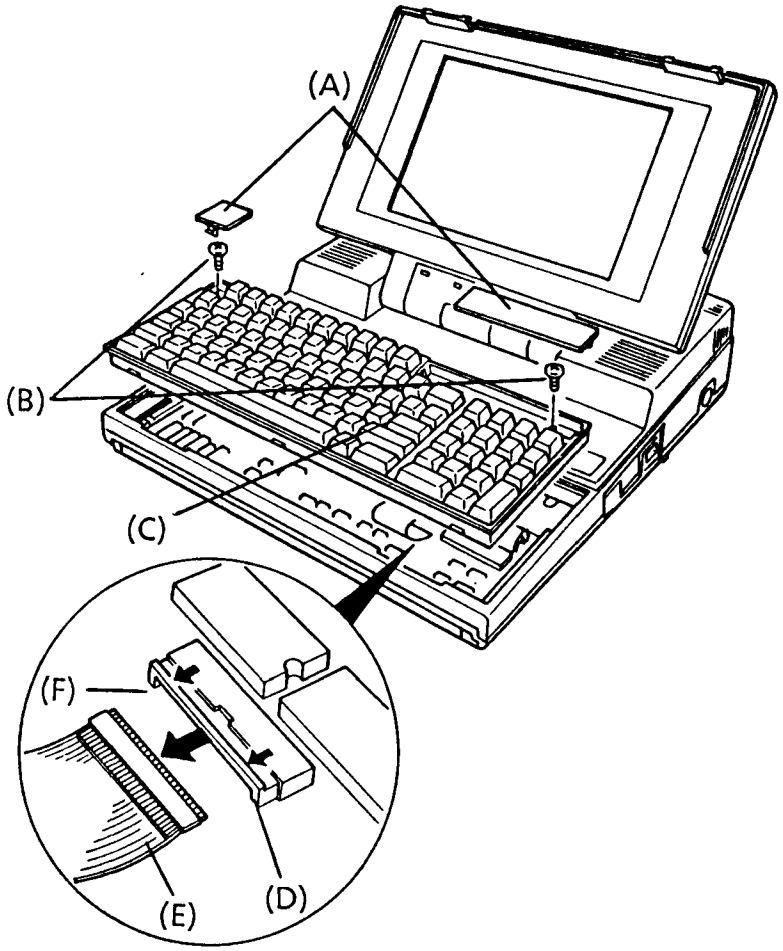


FIGURE 4-10 Removing the Keyboard Unit

5. To install a keyboard unit, follow the above procedures in reverse.

4.8 REMOVING/REPLACING THE SPEAKER AND THE LITHIUM BATTERY

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Remove the top cover as directed in part 4.2.
3. To remove the lithium battery (A), disconnect the lithium battery cable (B) from the system PCB (C) and lift it up.
4. Disconnect the speaker cable (D) from the system PCB.
5. Remove the speaker (E) by pushing the plastic latch (F) outward until the speaker can be pulled out.

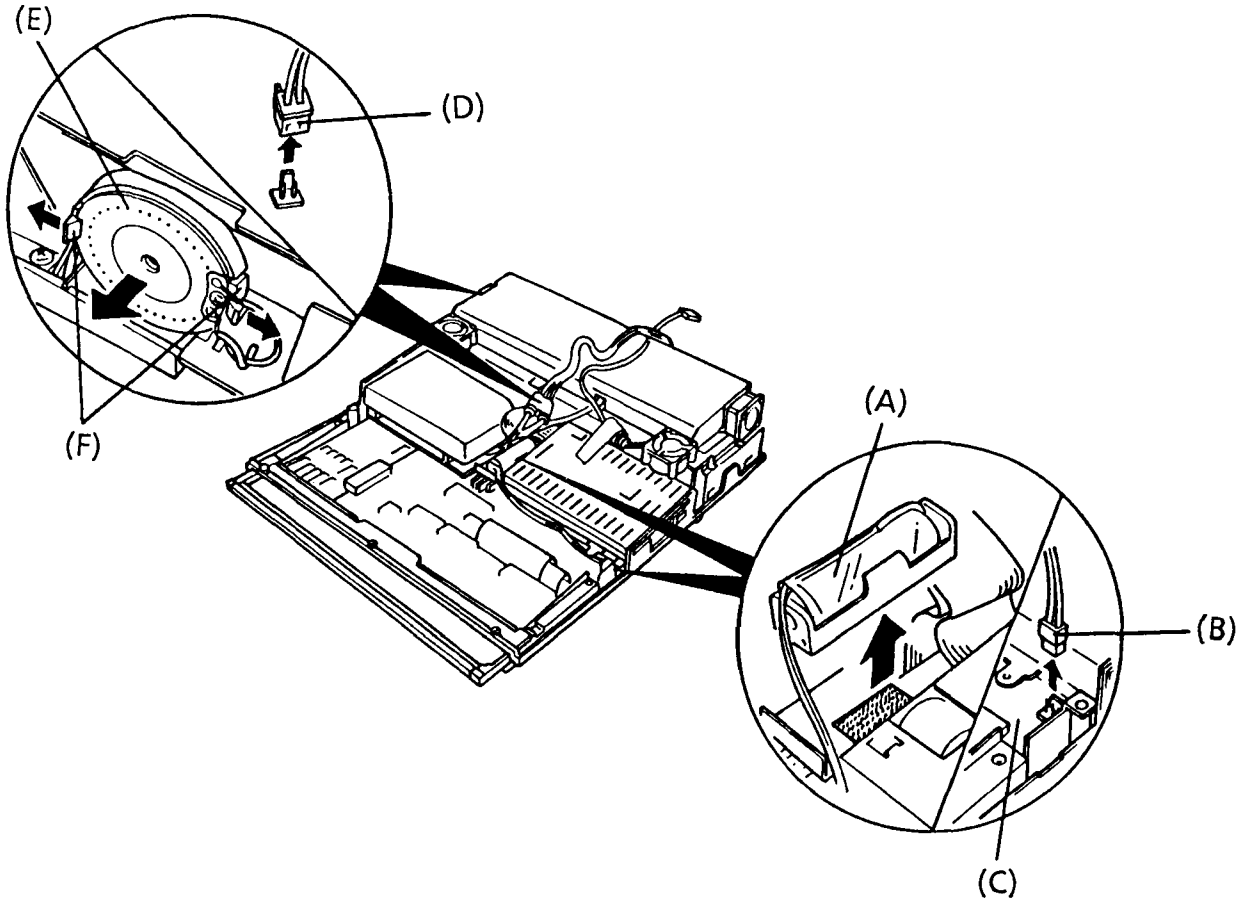


FIGURE 4-11 Removing the Lithium Battery and the Speaker

6. To install a new lithium battery and speaker, follow the above procedures in reverse.

4.9 REMOVING/REPLACING THE POWER SUPPLY UNIT

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Remove the top cover as directed in part 4.2.
3. Disconnect the two power supply cable (A) from the system PCB (B).
4. To remove the power supply unit (C), remove the three screws (D) from the power supply unit.

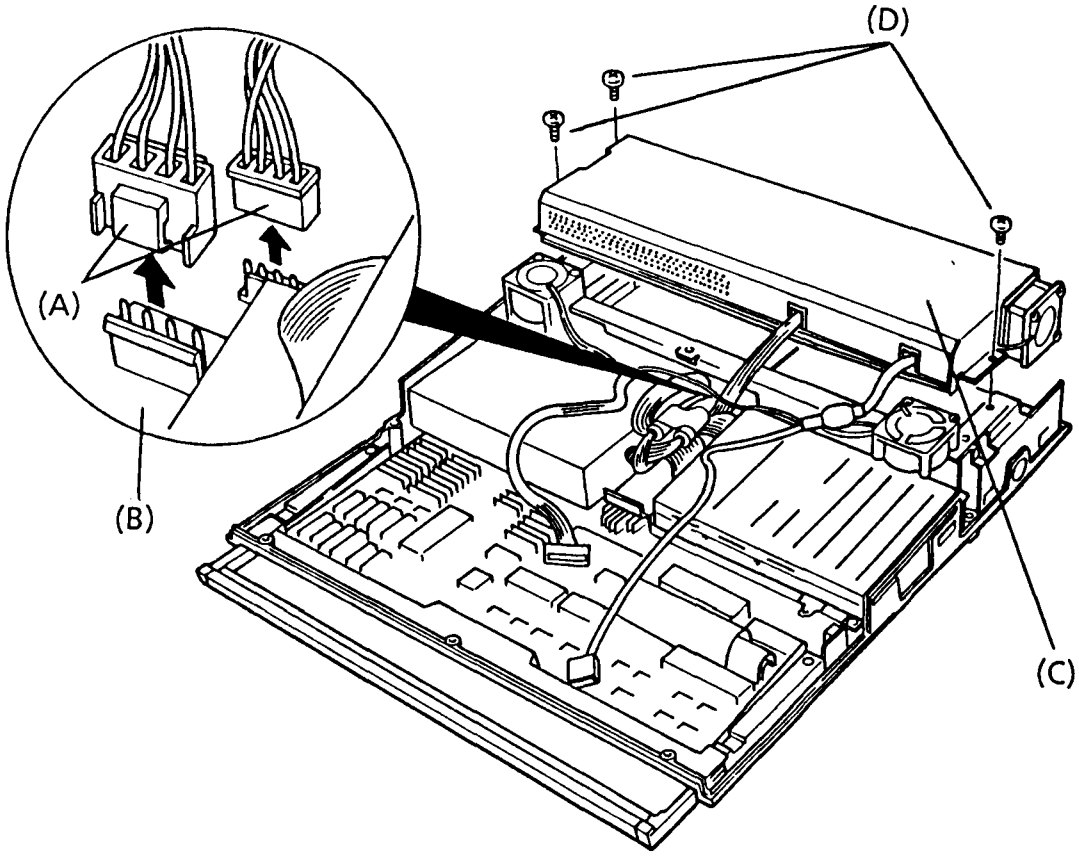


FIGURE 4-12 Removing the Power Supply Unit

5. To install a power supply unit, follow the above procedures in reverse.

4.10 REMOVING/REPLACING THE FDD

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Remove the top cover as directed in part 4.2.
3. Remove the lithum battery (A) from the FDD base (B).
4. Disconnect the FDD cable (C) from the system PCB (D).
5. Remove the five screws (E) and ground cable (F) from the FDD base.

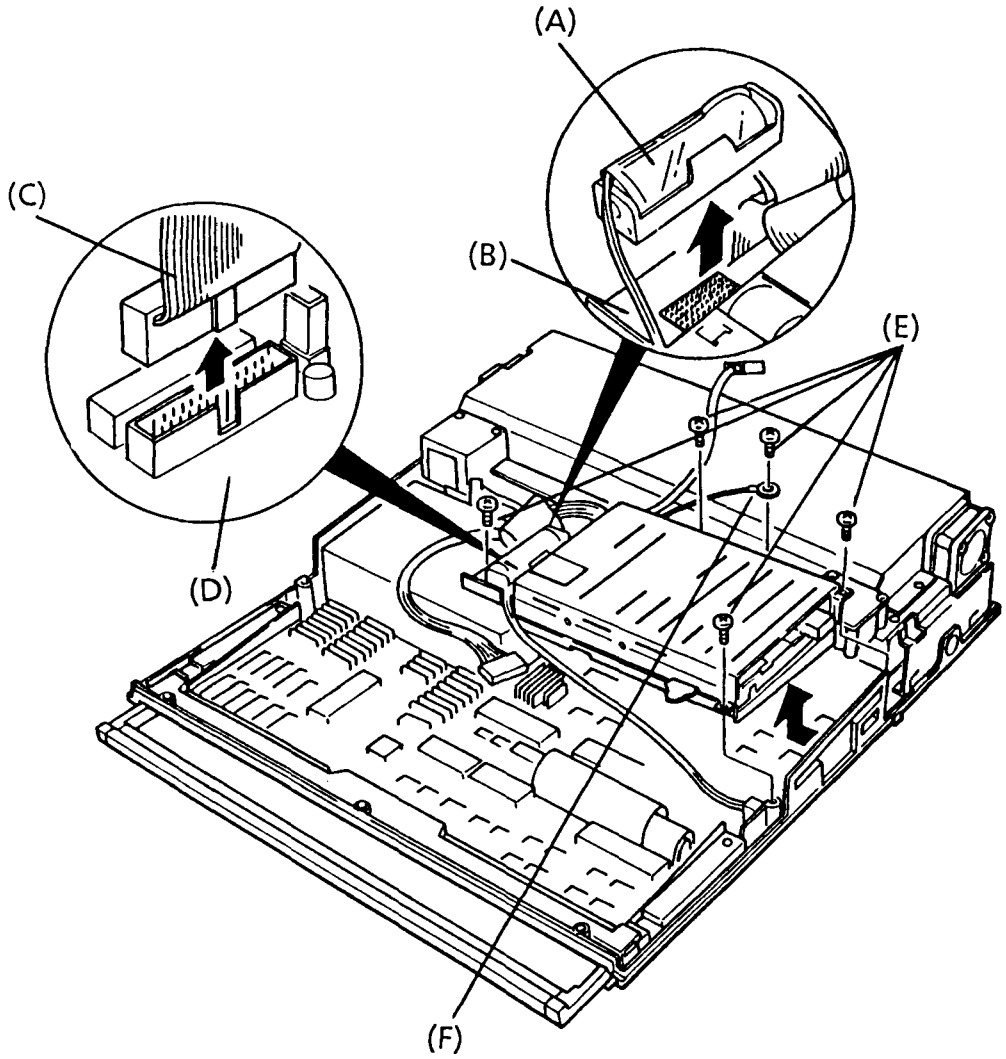


FIGURE 4-13 Removing the FDD Base

6. Remove the three screws (G) from the bottom of the FDD base.

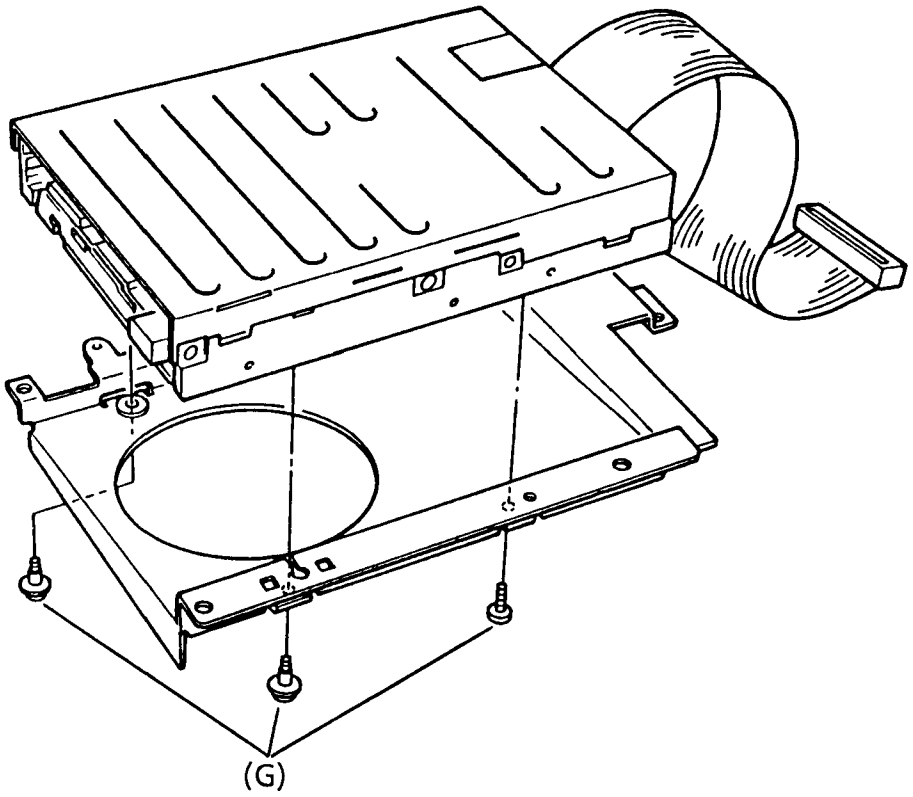


FIGURE 4-14 Removing the FDD

7. To install a new FDD, follow the above procedures in reverse.

4.11 REMOVING/REPLACING THE HDD

CAUTION: The hard disk contents will remain in the old hard disk. If desired, transfer the contents of the old hard disk onto a floppy disk before replacing the hard disk. This can be done with the MS-DOS BACKUP command. (See the MS-DOS manual for details.)

1. Confirm that the POWER switch is off and unplug the ac cord.

2. Remove the top cover and FDD base as directed in part 4.2 and 4.10.

3. Disconnect the HDD power cable (A) and HDC cable (B) from the HDD (C).

4. To remove the HDD, hold the HDD and remove the four screws (D) from the bottom of the base assembly (E).

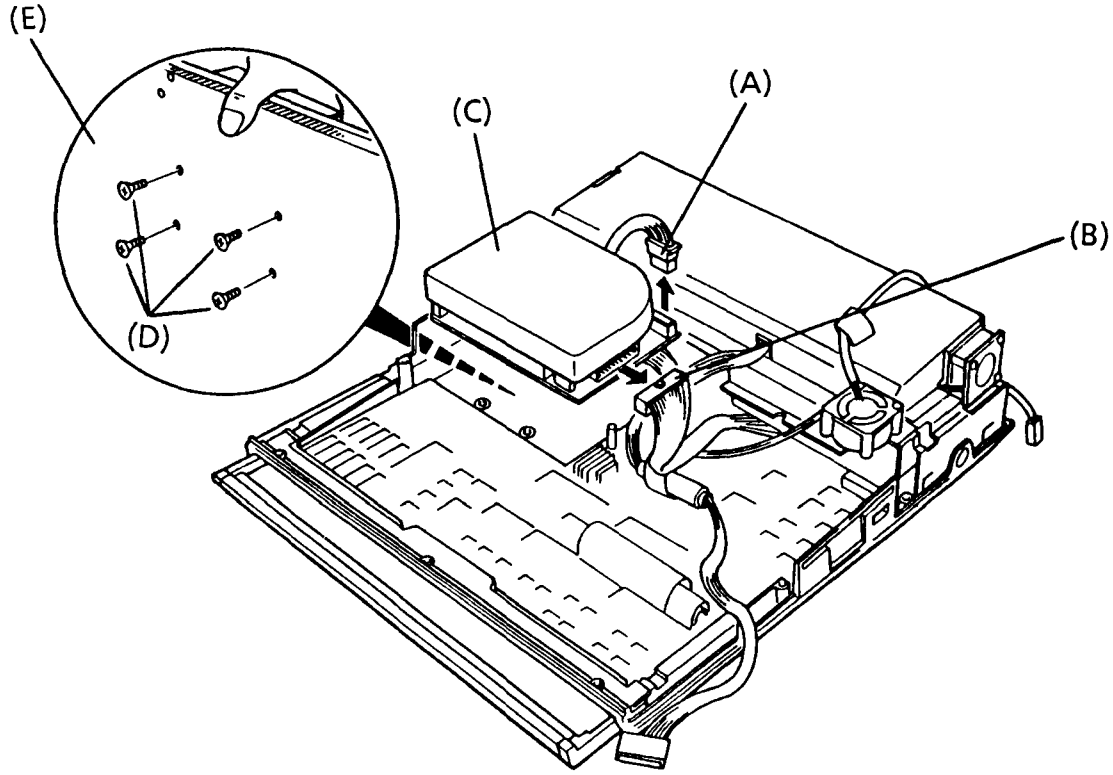


FIGURE 4-15 Removing the HDD

5. To install a new HDD, follow the above procedures in reverse.

6. Enter the MS-DOS FDISK command, which will set the partition. Then enter the MS-DOS FORMAT command. (See the MS-DOS manual for details.)

4.12 REMOVING/REPLACING THE EXPANSION BUS PCB AND THE FAN

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Remove the top cover and the FDD base as directed in part 4.2 and 4.10.
3. Disconnect the fan and HDD power cable (A) from the HDD (B) and the system PCB (C).
4. Remove the two screws (D), then lift it up.
5. To remove the fan on the expansion bus PCB (E), remove the two screws (F).

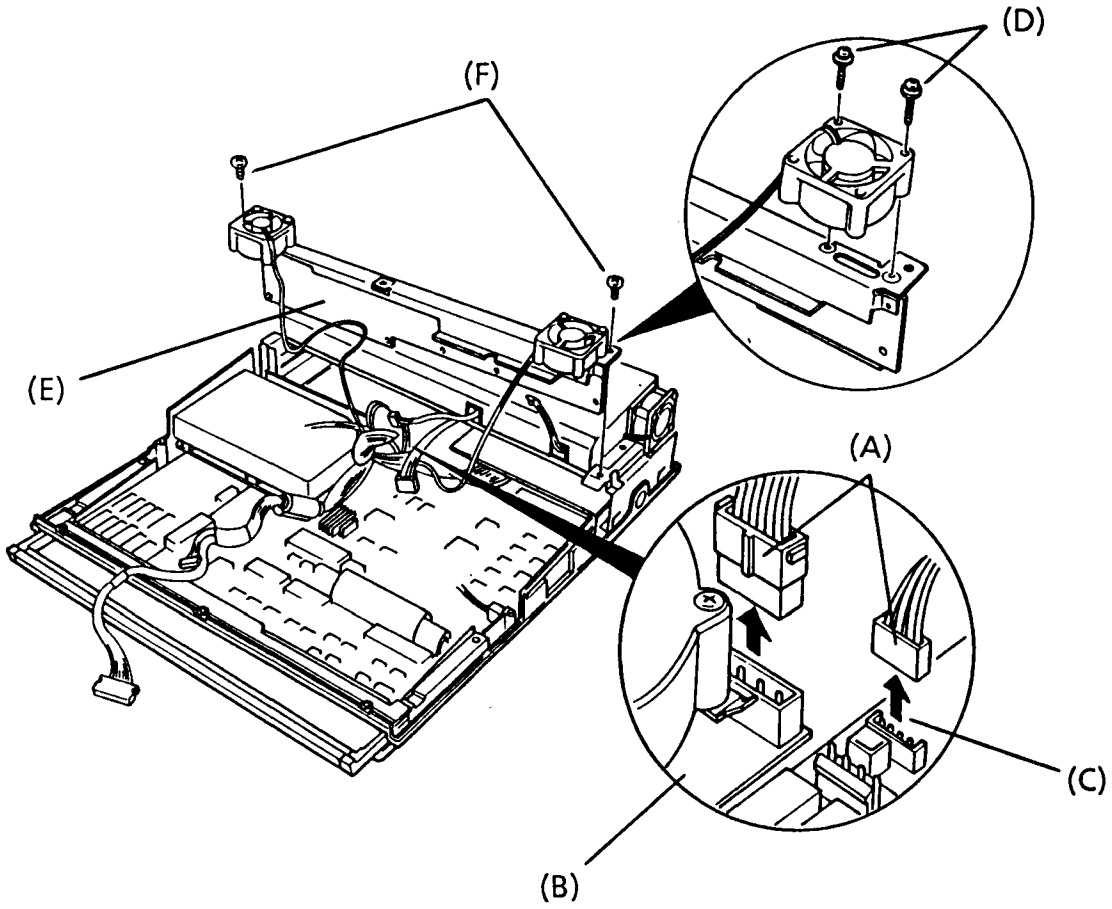


FIGURE 4-16 Removing the Expansion Bus PCB and the Fan

6. To install a new expansion bus PCB and a new fan, follow the above procedures in reverse.

4.13 REMOVING/REPLACING THE HARD DISK CONTROL PCB

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Remove the expansion bus PCB as directed in part 4.12.
3. Disconnect the HDC cable (A) from the HDD (B), then remove the two screws (C) from the HDC (D).
4. To remove the HDC from the system PCB (E) lift it up.

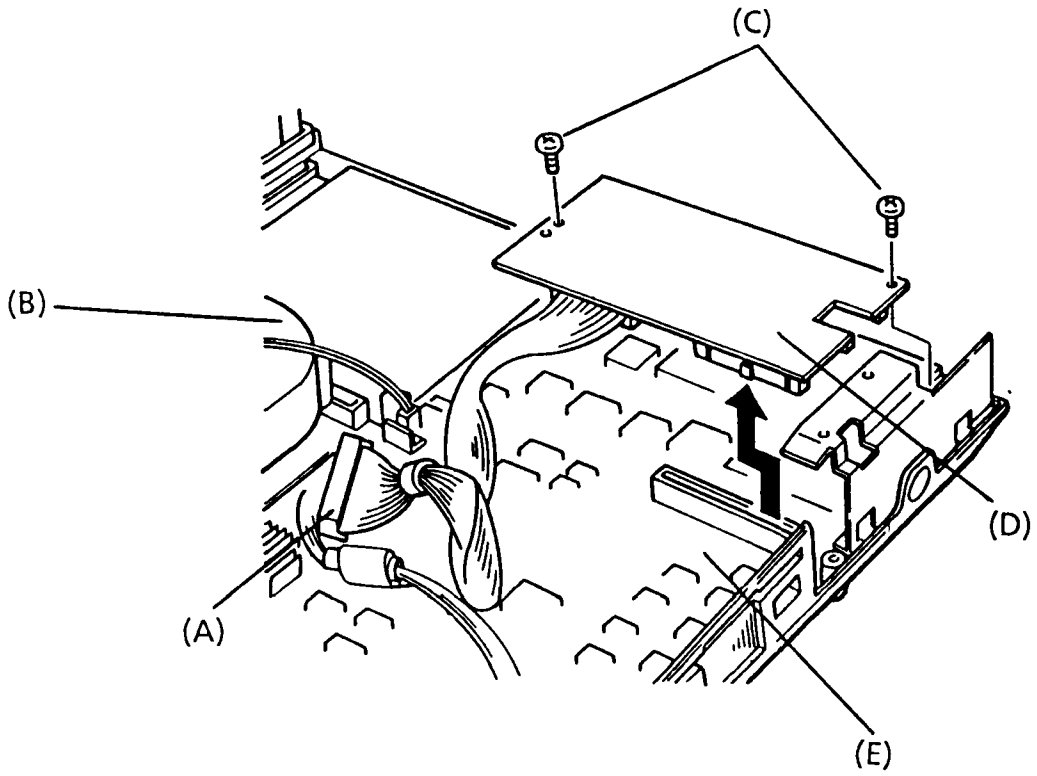


FIGURE 4-17 Removing the HDC

5. To install a new HDC, follow the above procedures in reverse.

4.14 REMOVING/REPLACING THE SYSTEM PCB

1. Confirm that the POWER switch is off and unplug the ac cord.

2. Remove the power supply unit, the FDD base and the expansion bus PCB as directed in part 4.9, 4.10 and 4.12.

3. Disconnect the speaker cable (A) from the system PCB (B).

4. Remove the thirteen screws (C) and three spacer (D) on the system PCB.
   If the system has optional memory card, remove the optional memory card from the system PCB after removing the system PCB. (Refer to part 4.15.)

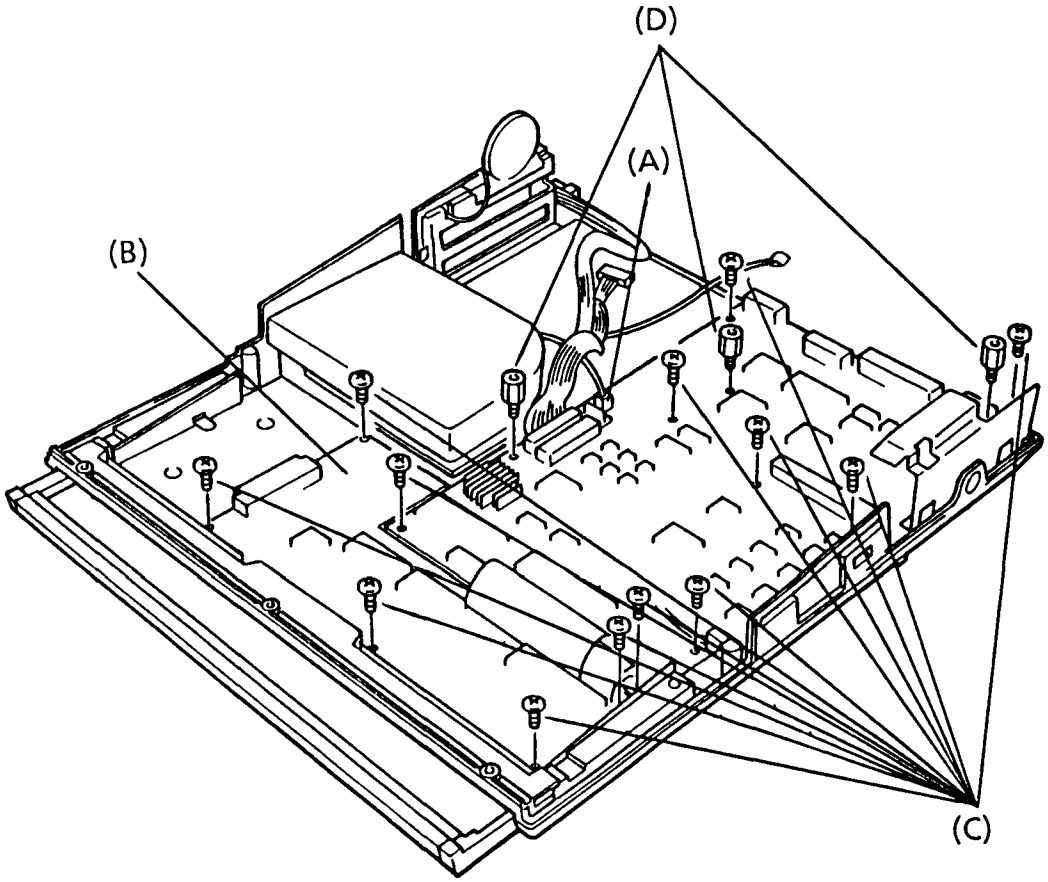


FIGURE 4-18 Removing the System PCB

5. To install a new system PCB, follow the above procedures in reverse.

4.15 REMOVING/REPLACING THE OPTIONAL MEMORY CARD

1. Confirm that the POWER switch is off and unplug the ac cord.
2. Remove the keyboard unit as directed in part 4.7.
3. Remove the single screw (A) from the optional memory card (B).
4. To remove the optional memory card, lift up a part of the system PCB and optional memory card, then disconnect the optional memory card connector (C) from the system PCB.

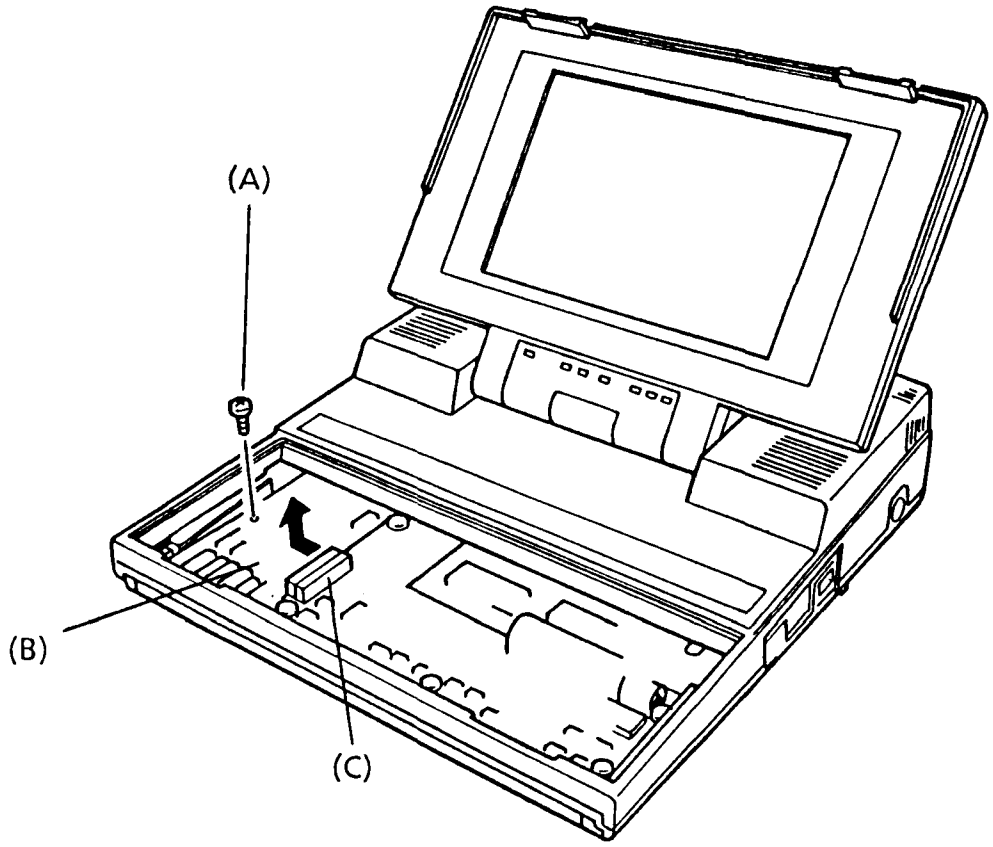


FIGURE 4-19 Removing the Optional Memory Card

5. To install a new optional memory card, follow the above procedures in reverse.

5.1 PCB LAYOUT

5.1.1 System PCB connectors

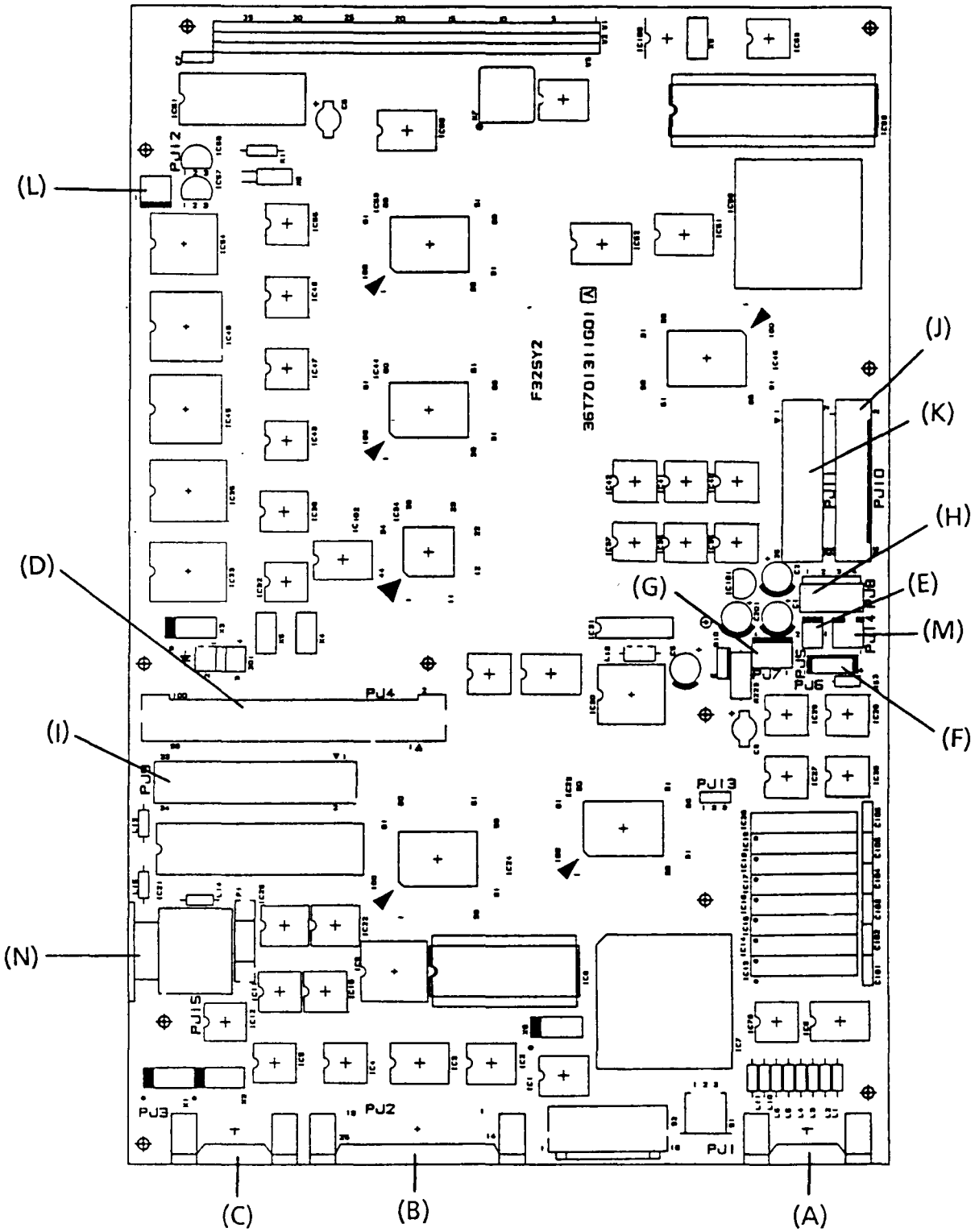


FIGURE 5-1 System PCB Connectors

(A) PJ 1 CRT connector

(B) PJ 2 PRT/FDD connector

(C) PJ 3 COMMS connector

(D) PJ 4 Expansion connector

(E) PJ 5 Speaker connector

(F) PJ 6 HDD power connector

(G) PJ 7 Power supply connector (± 12 V)

(H) PJ 8 Power supply connector (+ 5 V)

(I) PJ 9 HDC connector

(J) PJ 10 PDP connector

(K) PJ 11 FDD connector

(L) PJ 12 Lithium battery connector

(M) PJ 14 Sensor connector

(N) PJ 15 External keyboard connector

5.1.2 System PCB ICs

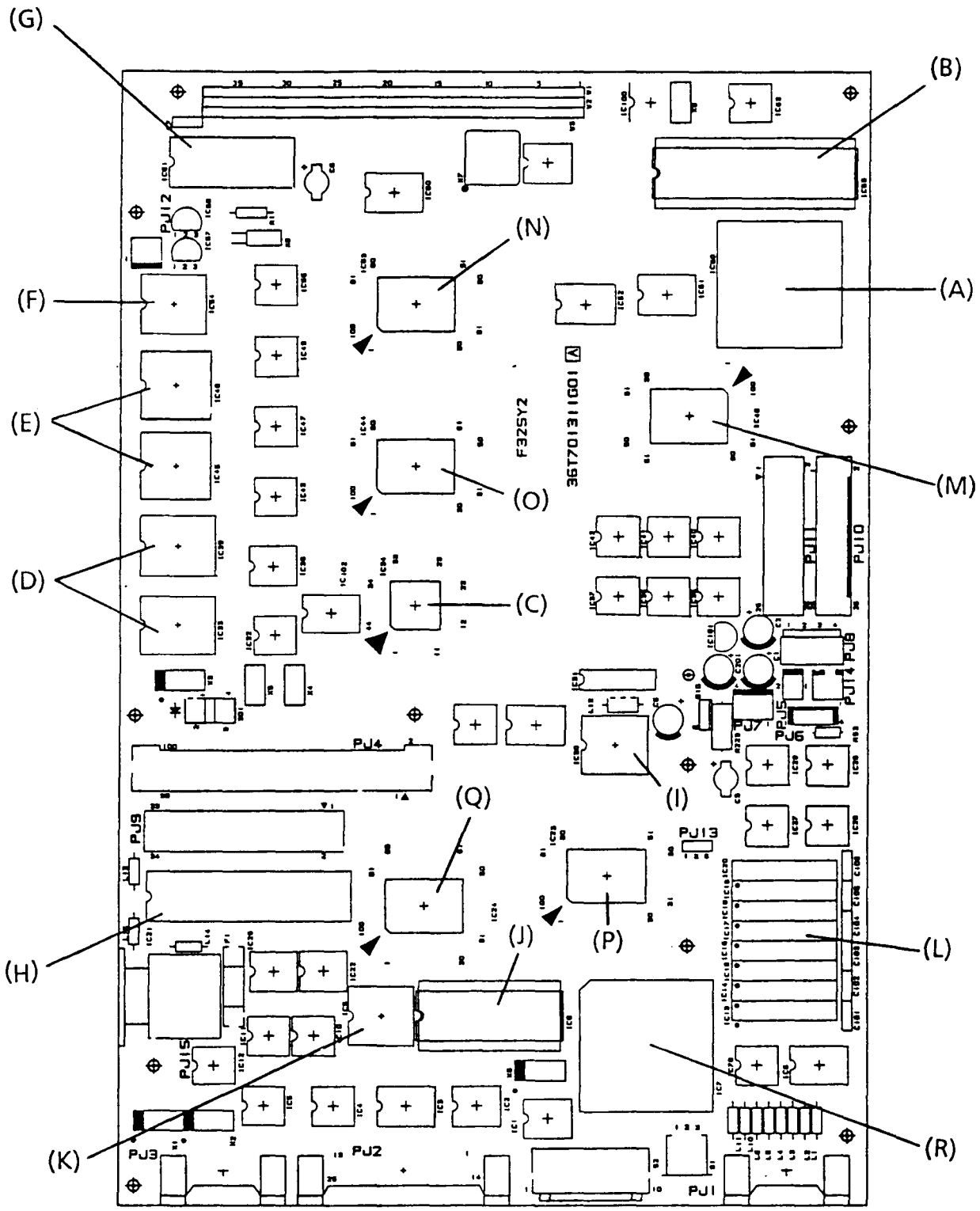


FIGURE 5-2 System PCB ICs

(A) CPU: Central processing unit (80286-12)

(B) NDP: Numeric data processor socket (option)

(C) FDC: Floppy disk controller (TC8565)

(D) PIC: Programmable interrupt controller (82C59)

(E) DMA: Direct memory access controller (82C37)

(F) PIT: Programmable interval timer (82C54)

(G) RTC: Rial time clock (46818)

(H) SIO: Serial input/output controller (T8570)

(I) VFO: Variable frequency oscillator (4108A)

(J) AGS ROM

(K) AGS RAM

(L) V-RAM (256 kbytes)

(M) Gate array (bus driver)

(N) Gate array (memory mapper)

(O) Gate array (DMA)

(P) Gate array (AGS)

(Q) Gate array (I/O controller)

(R) PEGA2

5.1.3 Keyboard control PCB

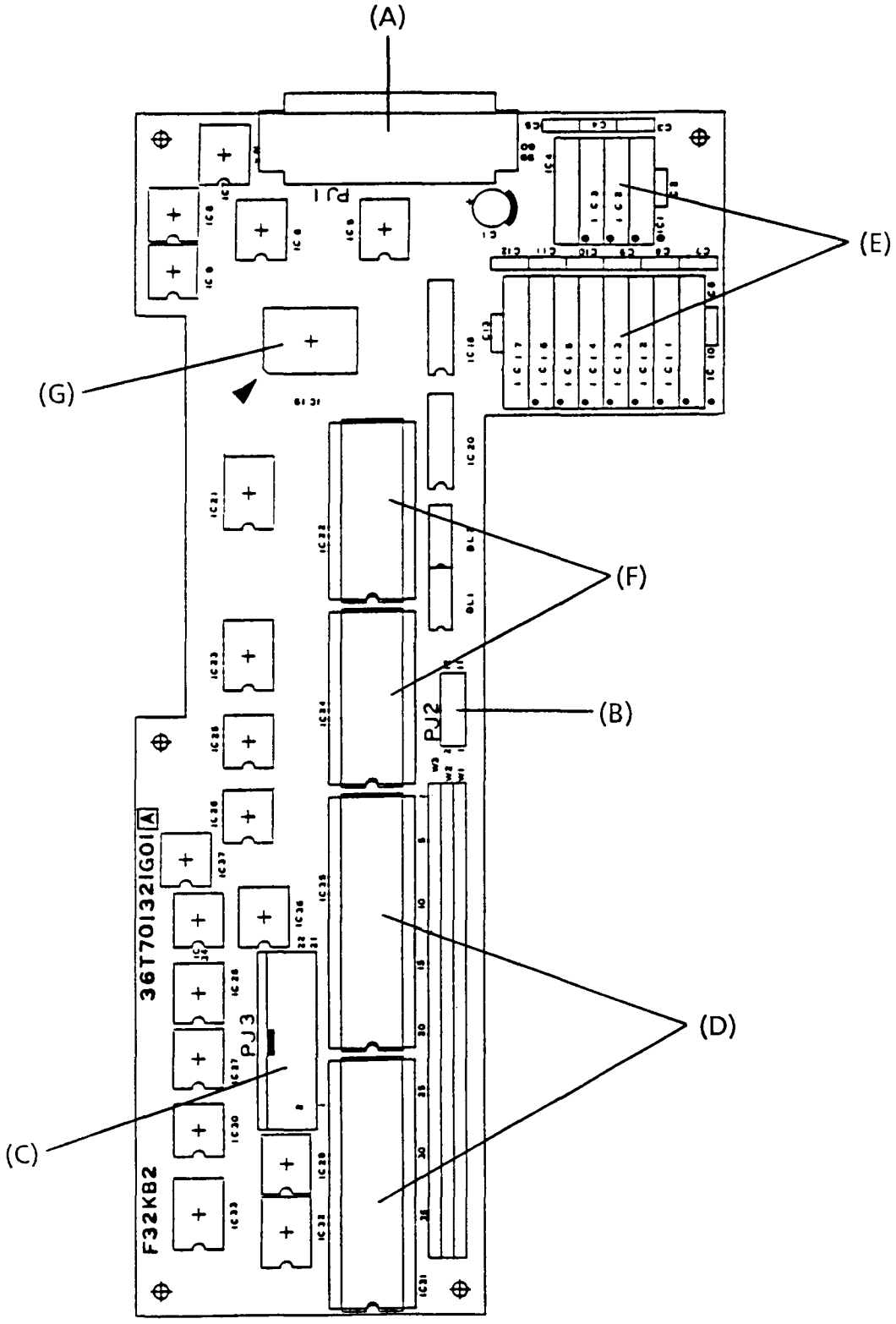


FIGURE 5-3 Keyboard Control PCB

(A) PJ 1 Memory card connector

(B) PJ 2 Jumper straps

(C) PJ 3 Keyboard connector

(D) Keyboard controller (8742)

(E) System RAM

(F) BIOS ROM

(G) Gate array (EMS)

5.2 CONNECTORS

5.2.1 PRT/EXT FDD connector

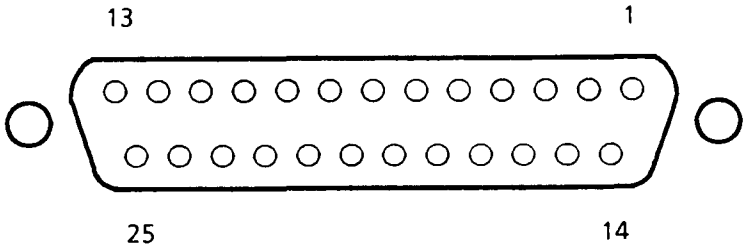


FIGURE 5-4 PRT/EXT FDD Connector

TABLE 5-1 PRT/EXT FDD Connector Signal Names

PIN	(FOR PRT)			(FOR EXT FDD)		
	SIGNAL	I/O	DESCRIPTION	SIGNAL	I/O	DESCRIPTION
1	STROBE;000	O	- STROBE	READY;000	I	- EXTERNAL DRIVE READY
2	PD0;110	O	+ DATA BIT 0	INDEX;000	I	- INDEX
3	PD1;110	O	+ DATA BIT 1	TRACK0;000	I	- TRACK ZERO
4	PD2;110	O	+ DATA BIT 2	WPROTC;000	I	- WRITE PROTECTED
5	PD3;110	O	+ DATA BIT 3	RDDA;000	I	- READ DATA
6	PD4;110	O	+ DATA BIT 4	DSKCHG;000	I	- DISK CHANGE
7	PD5;110	O	+ DATA BIT 5	-		(NOT USED)
8	PD6;110	O	+ DATA BIT 6	-		(NOT USED)
9	PD7;110	O	+ DATA BIT 7	-		(NOT USED)
10	ACK;000	I	- ACKNOWLEDGE	SWFDP;100	O	+ DRIVE SELECT
11	BUSY;100	I	+ BUSY	SWMONB;000	O	+ MOTOR ON
12	PE;100	I	+ PAPER END	WRDATA;100	O	+ WRITE DATA
13	SELECT;100	I	+ SELECT	EXFWE;100	O	+ WRITE ENABLE
14	AUTFD;000	O	- AUTO FEED	XRATE0;100	O	+ LOW DENSITY
15	ERROR;000	I	- ERROR (FAULT)	SIDE;100	O	+ SIDE SELECT
16	PINIT;000	O	- PRINTER INITIALIZE	FDCDRC;100	O	+ DIRECTION
17	SLIN;000	O	- SELECT INPUT	STEP;100	O	+ STEP
18-25	GND		GROUND (0 V)	GND		GROUND (0 V)

5.2.2 RGB connector

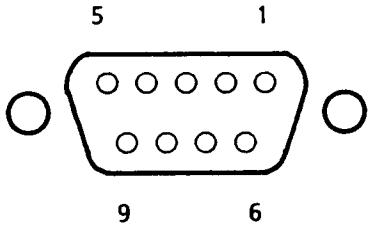


FIGURE 5-5 RGB Connector

TABLE 5-2 RGB Connector Signal Names

PIN	I/O	SIGNAL	MONOCHROME	STANDARD RGB	ENHANCED RGB
1		GND	Ground	Ground	Ground
2	O	PESR;100	Ground	Ground	S.Red
3	O	PERE;100	Not connected	Red	Red
4	O	PEGR;100	Not connected	Green	Green
5	O	PEBL;100	Not connected	Blue	Blue
6	O	PESG;100	Intensity	Intensity	Intensity/ S.Green
7	O	PESB;100	Video	Not connected	S.Blue
8	O	PEHS;100	H.Sync	H.Sync	H.Sync
9	O	PEVS;100	V.Sync	V.Sync	V.Sync

5.2.3 COMMS connector

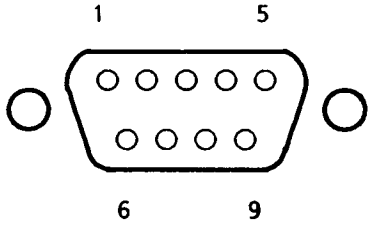


FIGURE 5-6 COMMS Connector

TABLE 5-3 COMMS Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	MDCD;100	I	+ DATA CARRIER DETECT
2	MDRD;100	I	+ RECEIVE DATA
3	MDTD;100	O	+ SEND DATA
4	MDDTR;100	O	+ DATA TERMINAL READY
5	GND		GROUND (0 V)
6	MDDSR;100	I	+ DATA SET READY
7	MDRTS;100	O	+ REQUEST TO SEND
8	MDCTS;100	I	+ CLEAR TO SEND
9	MDRI;100	I	+ RING INDICATOR

5.2.4 Expansion bus connector (in the system unit)

There are two typs of expansion bus connectors; one is 8-bit bus type, and the other is 16-bit bus type. 8 bit bus-type has signal names only at A side and B side.

TABLE 5-4 Expansion Bus Connector (A side/B side) Signal Names

PIN	SIGNAL	I/O	PIN	SIGNAL	I/O
A1	IOCHCK ; 000	I	B1	GND	
A2	SD7;100	I/O	B2	RESET;100	O
A3	SD6;100	I/O	B3	VCC	
A4	SD5;100	I/O	B4	IRQ9;100	I
A5	SD4;100	I/O	B5	M5V	
A6	SD3;100	I/O	B6	DREQ2;100	I
A7	SD2;100	I/O	B7	M12V	
A8	SD1;100	I/O	B8	OWAIT;000	I
A9	SD0;100	I/O	B9	P12V	
A10	IORDY;100	I	B10	GND	
A11	AEN;100	O	B11	SMEMW;000	O
A12	SA19;100	I/O	B12	SMEMR;000	O
A13	SA18;100	I/O	B13	IOW;000	I/O
A14	SA17;100	I/O	B14	IOR;000	I/O
A15	SA16;100	I/O	B15	DACK3; 000	O
A16	SA15;100	I/O	B16	DREQ3;100	I
A17	SA14;100	I/O	B17	DACK1;000	O
A18	SA13;100	I/O	B18	DREQ1;100	I
A19	SA12;100	I/O	B19	REFRSH;000	I/O
A20	SA11;100	I/O	B20	CLK;100	O
A21	SA10;100	I/O	B21	IRQ7;100	I
A22	SA9;100	I/O	B22	IRQ6;100	I
A23	SA8;100	I/O	B23	IRQ5;100	I
A24	SA7;100	I/O	B24	IRQ4;100	I
A25	SA6;100	I/O	B25	IRQ3;100	I
A26	SA5;100	I/O	B26	DACK2;000	O
A27	SA4;100	I/O	B27	TC;100	O
A28	SA3;100	I/O	B28	ALE;100	O
A29	SA2;100	I/O	B29	VCC	
A30	SA1;100	I/O	B30	CLKCRT;100	O
A31	SA0;100	I/O	B31	GND	

TABLE 5-5 Expansion Bus Connector (C side/D side) Signal Names

PIN	SIGNAL	I/O	PIN	SIGNAL	I/O
C1	SBHE;000	I/O	D1	MEM16;000	I
C2	A23;100	I/O	D2	IO16;000	I
C3	A22;100	I/O	D3	IRQ10;100	I
C4	A21;100	I/O	D4	IRQ11;100	I
C5	A20;100	I/O	D5	IRQ12;100	I
C6	A19;100	I/O	D6	IRQ15;100	I
C7	A18;100	I/O	D7	IRQ14;100	I
C8	A17;100	I/O	D8	DACK0;000	O
C9	MEMR;000	I/O	D9	DREQ0;100	I
C10	MEMW;000	I/O	D10	DACK5;000	O
C11	SD8;100	I/O	D11	DREQ5;100	I
C12	SD9;100	I/O	D12	DACK6;000	O
C13	SD10;100	I/O	D13	DREQ6;100	I
C14	SD11;100	I/O	D14	DACK7;000	O
C15	SD12;100	I/O	D15	DREQ7;100	I
C16	SD13;100	I/O	D16	VCC	
C17	SD14;100	I/O	D17	MASTER;000	I
C18	SD15;100	I/O	D18	GND	

5.2.5 External keyboard connector

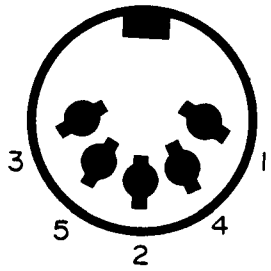


FIGURE 5-7 External Keyboard Connector

TABLE 5-6 External Keyboard Connector Signal Names

Pin	I/O	Signal Name
1	I/O	KBCLK (clock)
2	I/O	KBDAT (data)
3		N.C.
4		Vcc
5		GND

5.3 KEYBOARD LAYOUT

5.3.1 USA version

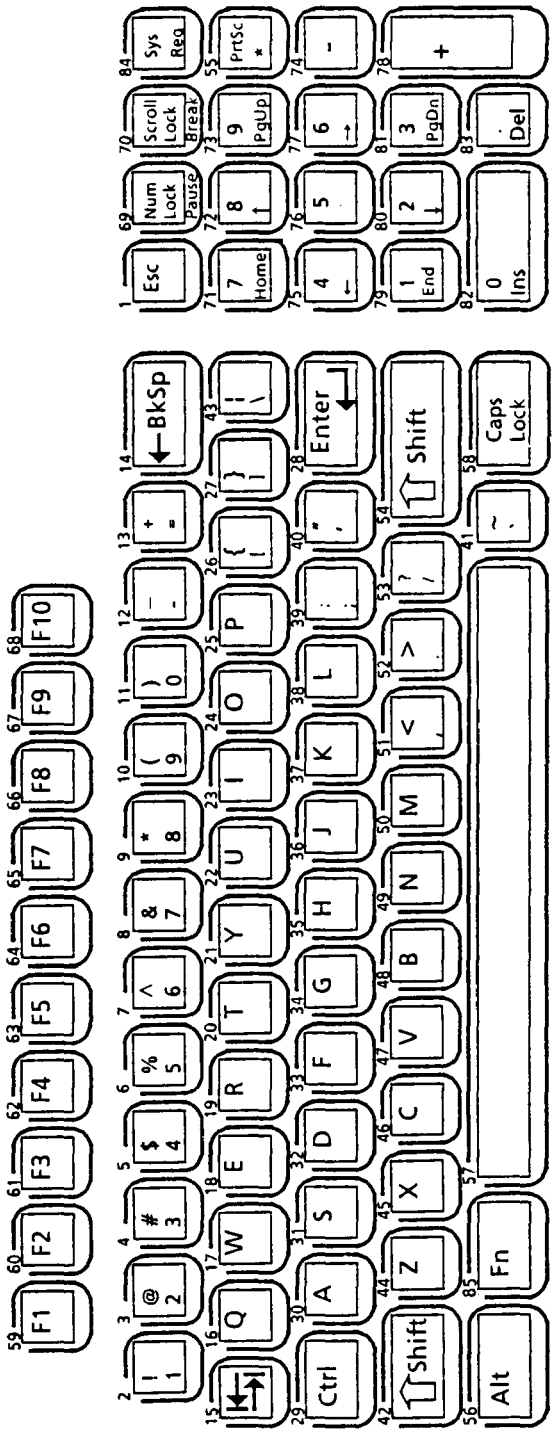


FIGURE 5-8 USA Version

5.3.2 England version

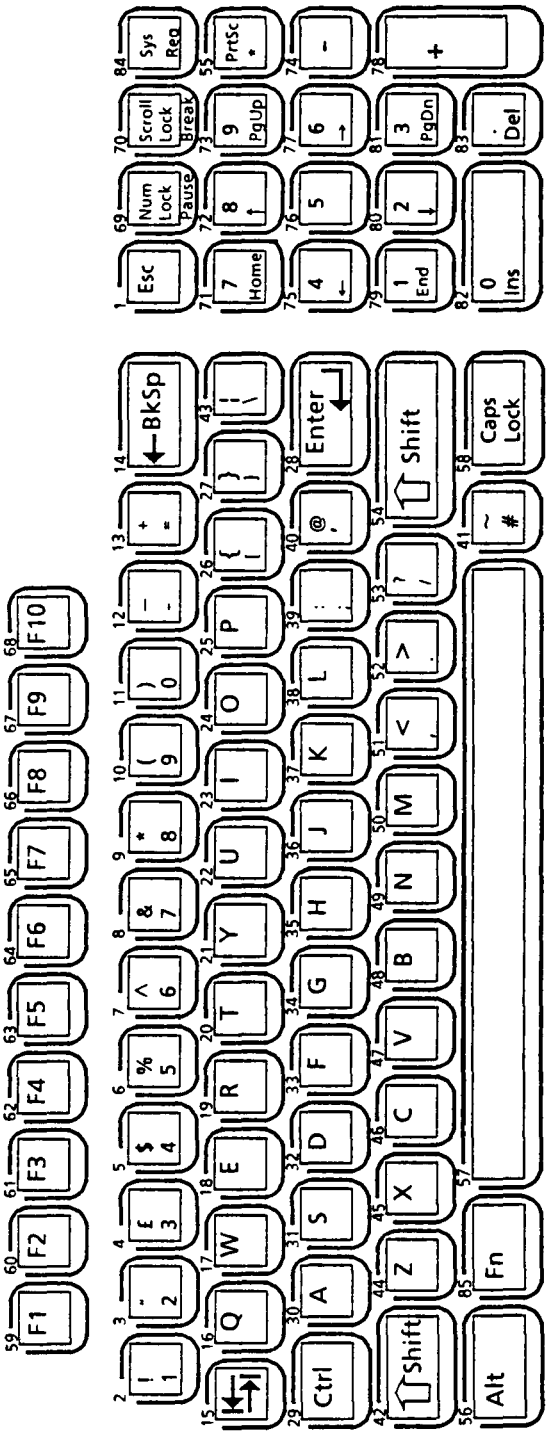


FIGURE 5-9 England Version

5.3.3 German version

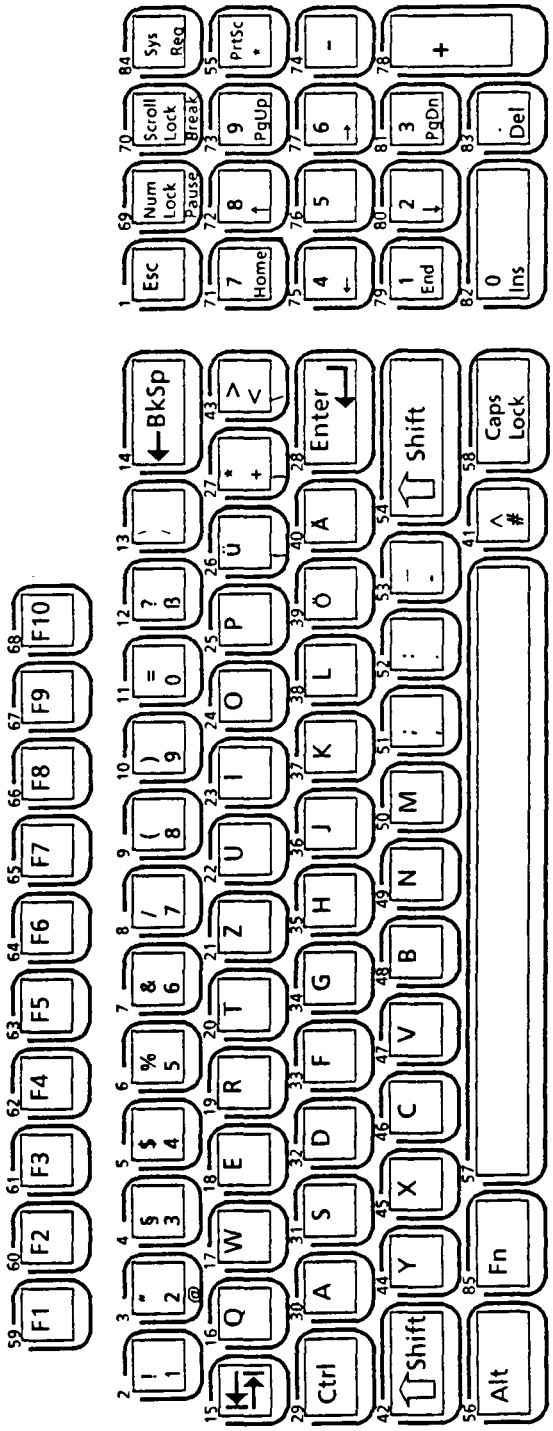


FIGURE 5-10 German Version

5.3.4 France version

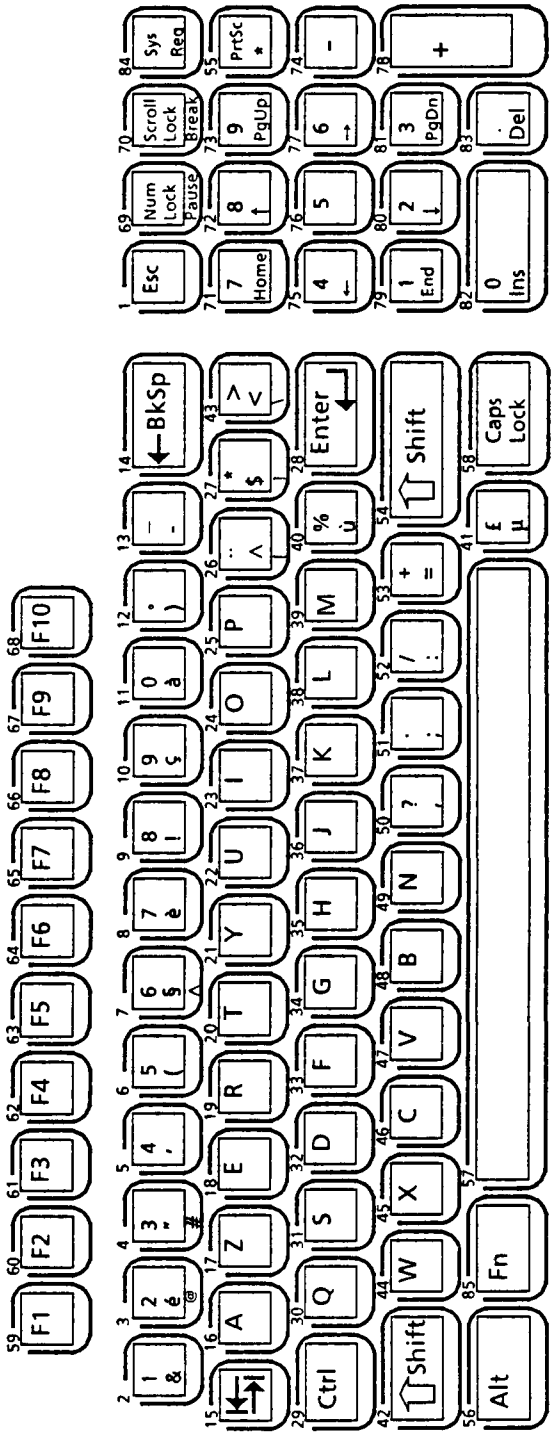


FIGURE 5-11 France Version

5.3.5 Spain version

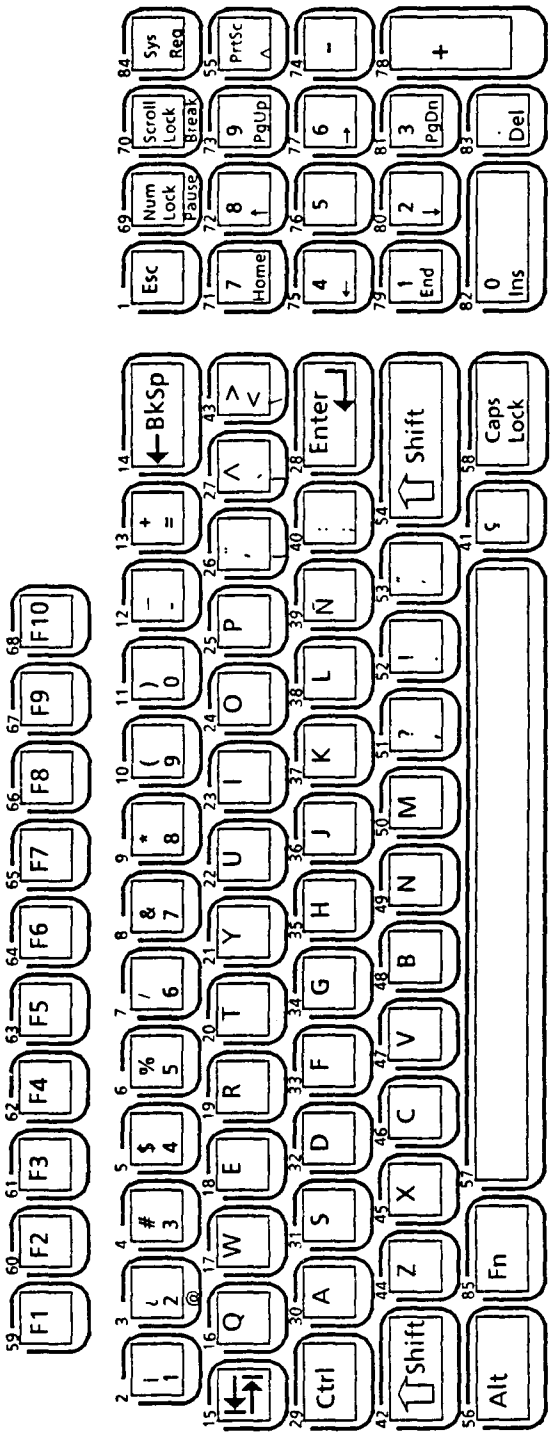


FIGURE 5-12 Spain Version

5.3.6 Italy version

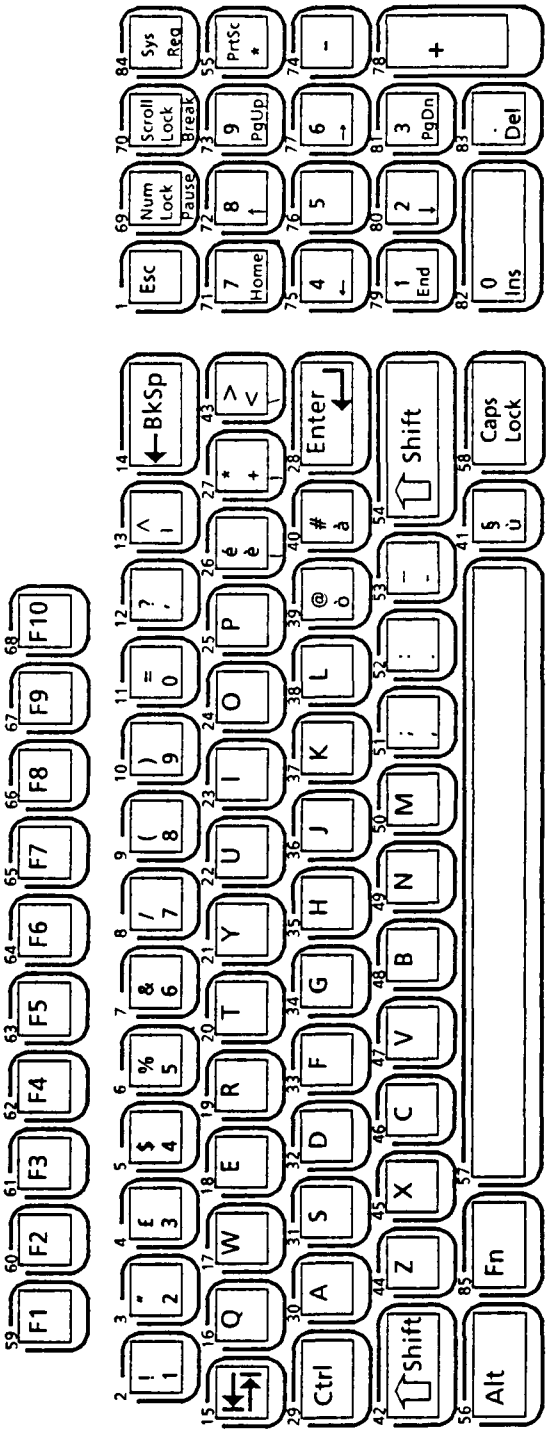


FIGURE 5-13 Italy Version

5.3.7 Scandinavia version

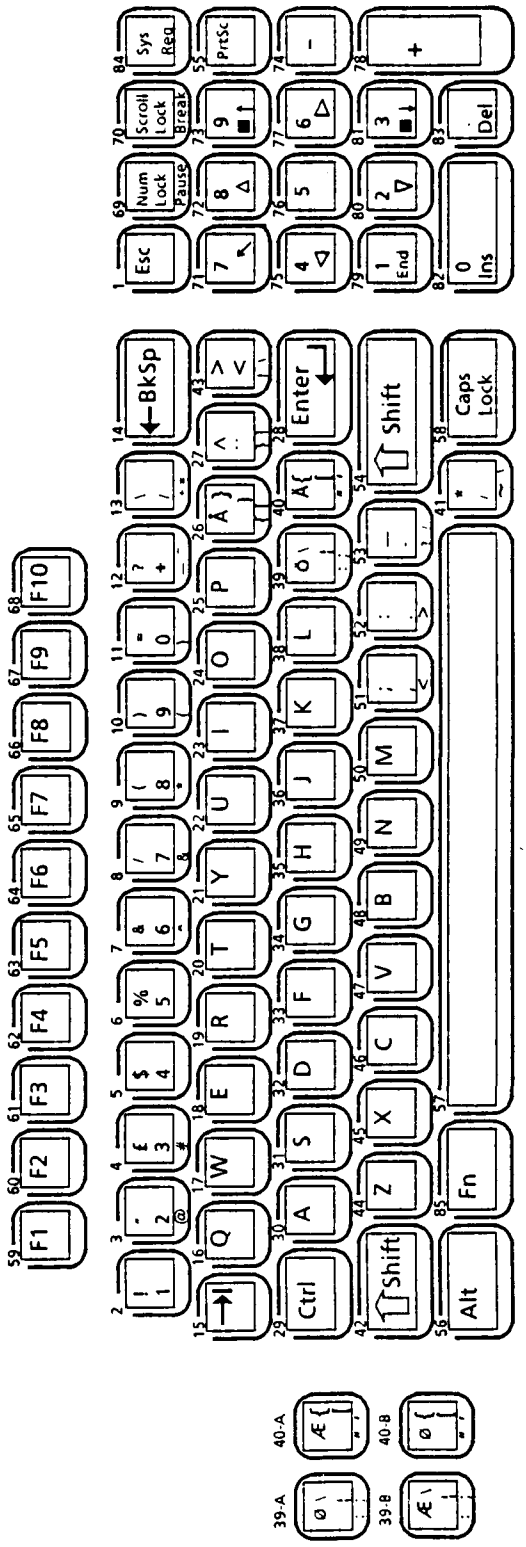


FIGURE 5-14 Scandinavia Version

5.3.8 Switzerland version

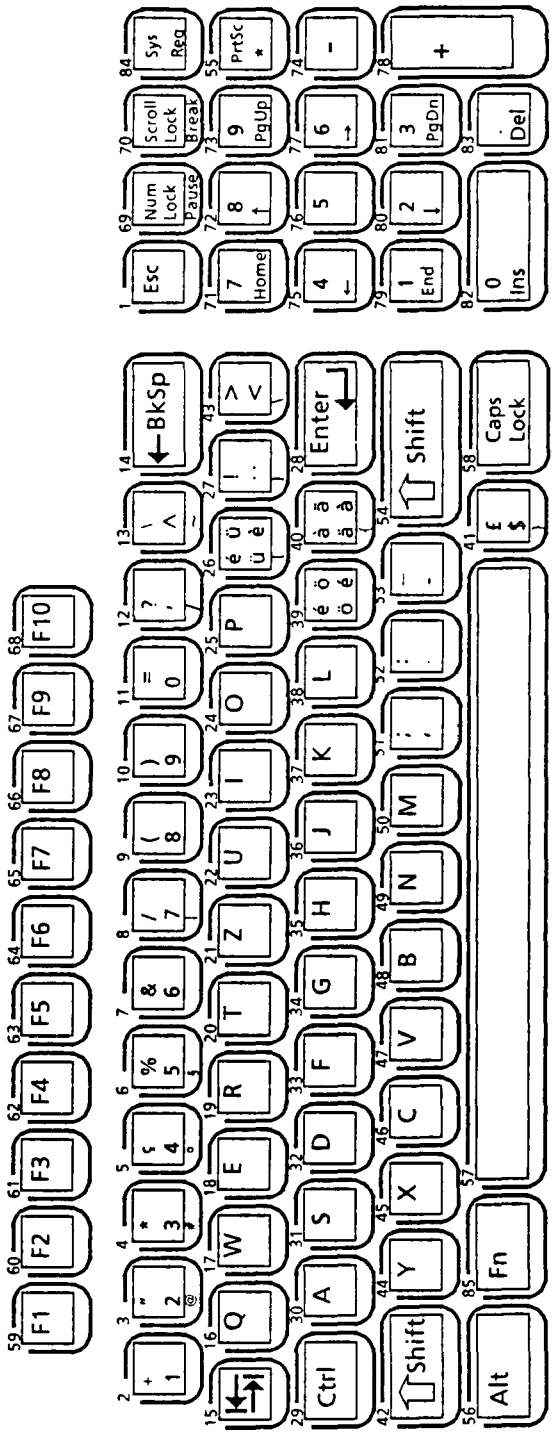


FIGURE 5-15 Switzerland Version

5.3.9 Keycap number

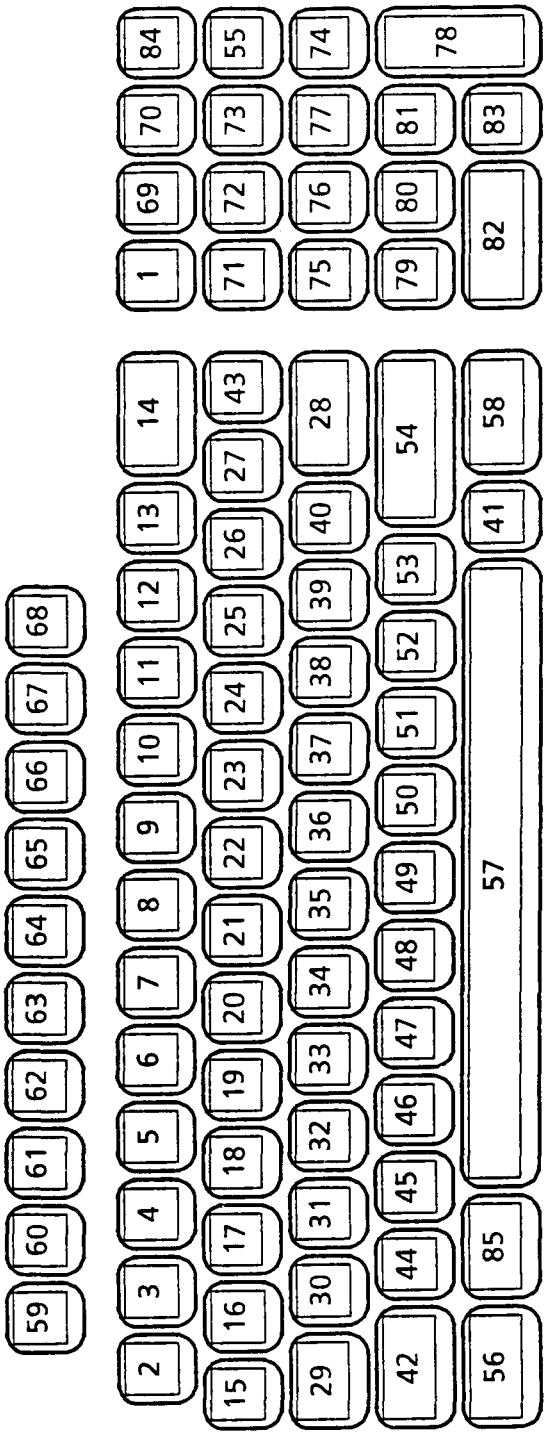


FIGURE 5-16 Keycap Number

5.4 DISPLAY CODE

TABLE 5-7 Display Code

HEXA DECIMAL VALUE	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BLANK (NULL)	►	BLANK (SPACE)	0	@	P	`	p	Ç	É	á	░	└	╨	α	≡
1	☺	◄	!	1	A	Q	a	q	ü	æ	í	▒	┴	╤	β	±
2	☻	↕	"	2	B	R	b	r	é	Æ	ó	▓	┬	╥	Γ	≥
3	♥	‼	#	3	C	S	c	s	â	ô	ú	│	├	╙	π	≤
4	♦	¶	$	4	D	T	d	t	ä	ö	ñ	┤	─	╘	Σ	⌠
5	♣	§	%	5	E	U	e	u	à	ò	Ñ	╡	┼	╒	σ	⌡
6	♠	▬	&	6	F	V	f	v	å	û	ª	╢	╞	╓	µ	÷
7	•	↨	'	7	G	W	g	w	ç	ù	º	╖	╟	╫	τ	≈
8	◘	↑	(	8	H	X	h	x	ê	ÿ	¿	╕	╚	╪	Φ	°
9	○	↓	)	9	I	Y	i	y	ë	Ö	⌐	╣	╔	┘	Θ	∙
A	◙	→	*	:	J	Z	j	z	è	Ü	¬	║	╩	┌	Ω	•
B	♂	←	+	;	K	[	k	{	ï	¢	½	╗	╦	█	δ	√
C	♀	∟	,	<	L	\	l	¦	î	£	¼	╝	╠	▄	∞	n
D	♪	↔	-	=	M	]	m	}	ì	¥	¡	╜	═	▌	φ	2
E	♫	▲	.	>	N	∧	n	~	Ä	Pt	«	╛	╬	▐	∈	■
F	☼	▼	/	?	O	_	o	△	Å	ƒ	»	┐	╧	▀	∩	BLANK FF

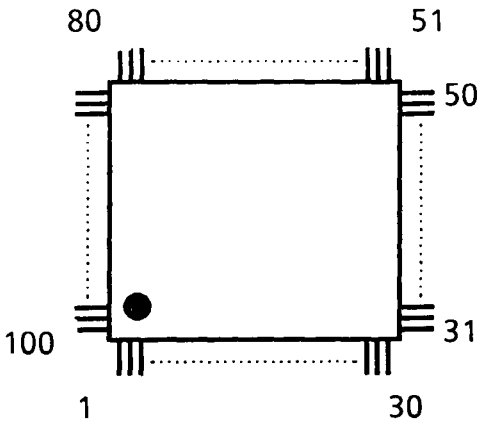
APPENDIX A

BUS DRIVER GA (Gate Array)

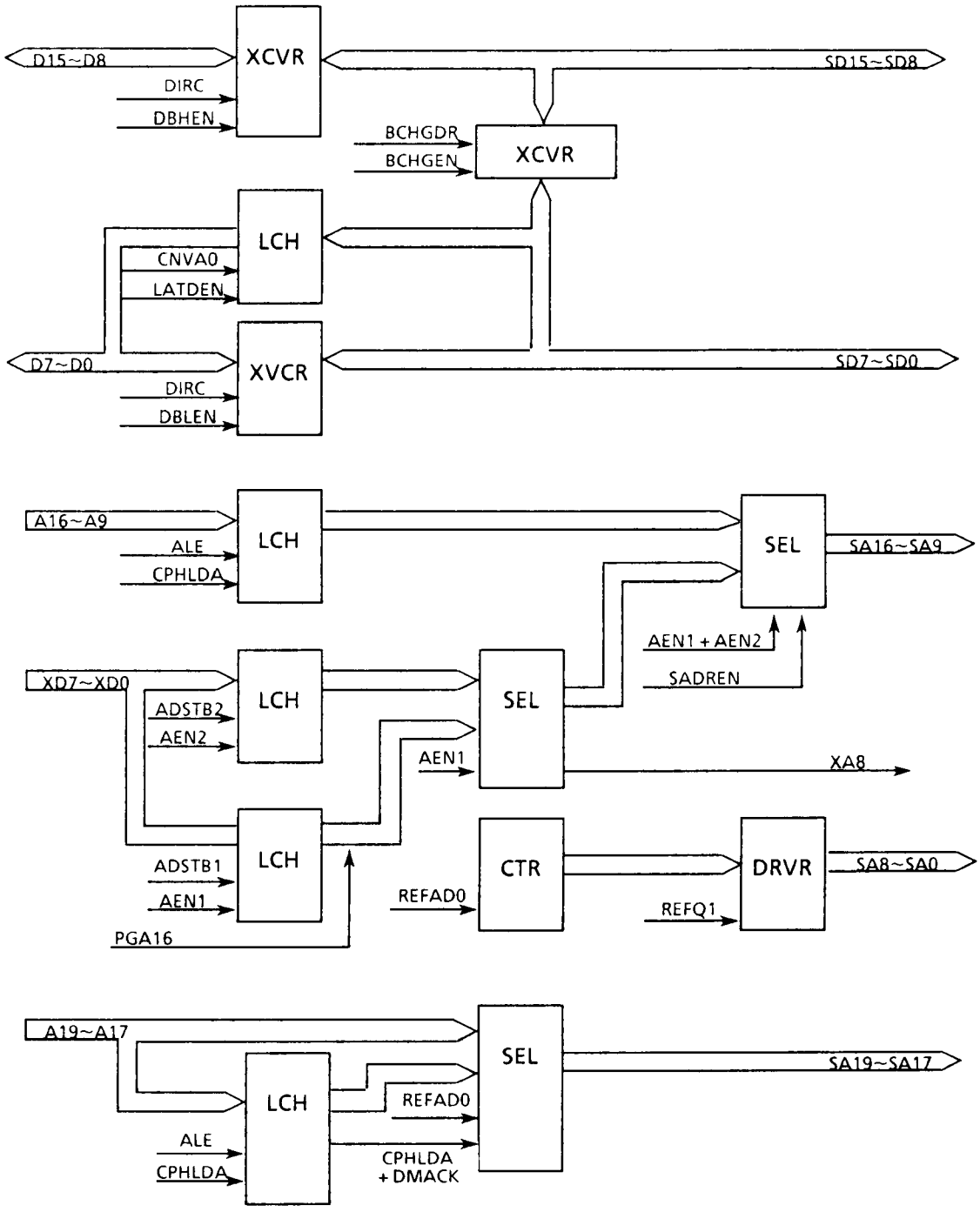
A.1 GENERAL

The Bus Driver Gate Array is a flat package typed chip with 100 lead pins, and it controls the busses between the CPU and Memory, or the CPU and I/O devices.
The Bus Driver Gate Array has the following functions.

- Input/ Output control of the 16-bit data bus
- Generation of the system address
- Generation of the Memory refresh address



A.2 **BLOCK DIAGRTAM**



XCVR : Transceiver
DRVR : Driver
SEL : Selector
LCH ; Latch
CTR : Counter

FIGURE A-1 Bus Driver GA Block Diagram

A.3 SIGNAL DESCRIPTION AND PIN ASSIGNMENT

TABLE A-1 Pin Description

Pin	I/O	Signal Name	Description
1	I	CPHLDA	CPU hold acknowledge signal. When this signal is high, the system bus is used by any other controller than the CPU.
2	I	ALE	CPU address latch signal. This signal is active high.
3		Vcc	+ 5V
4	I	PGA16	This signal is a part of DMA address from the page register of the Memory Mapper GA.
5	I	DIRC	Data transfer direction signal in the CPU access mode. When this signal is low, the data goes to the CPU (read cycle), and when it is high, the data comes from the CPU (write cycle).
6	I	BUSEN	Data bus enable signal. This signal controls data enable timing during the CPU read/ write operation. This signal is active high.
7	I	XD0	XD7~XD0 are data bus from the I/O controllers. The DMAC outputs DMA address on the data bus during the DMA operation. Data bus bit 0.
8	I	XD1	Data bus bit 1.
9	I	XD2	Data bus bit 2.
10	I	XD3	Data bus bit 3.
11	I	XD4	Data bus bit 4.
12	I	XD5	Data bus bit 5.
13	I	XD6	Data bus bit 6.
14	I	XD7	Data bus bit 7.
15		GND	Ground
16	I	AEN1	Address enable signal for the slave DMA. This signal is active low.
17	I	AEN2	Address enable signal for the master DMA. This signal is active low.
18	I	A9	A19~A9 are the CPU address lines. These lines also come from the Memory Mapper GA for the DMA address transfer. CPU address line bit 9.
19	I	A10	CPU address line bit 10.
20	I	A11	CPU address line bit 11.
21	I	A15	CPU address line bit 15.

Pin	I/O	Signal Name	Description
22	I	A12	CPU address line bit 12.
23	I	A13	CPU address line bit 13.
24	I	A17	CPU address line bit 17.
25	I	A19	CPU address line bit 19.
26	I	A14	CPU address line bit 14.
27	I	A16	CPU address line bit 16.
28		Vcc	+ 5V
29	I	A18	CPU address line bit 18.
30	I	DMACK	This signal is generated by CPHLDA signal. When this signal is low, CPU mode is activated, and when it is high, DMA mode is activated.
31	O	XA8	DMA address
32	I/O	SD15	Each of SD15~SD0 is the system data bus. The lines SD15~SD8 are in the high bank, while SD7~SD0 are in the low bank. System data bus bit 15.
33	I/O	SD14	System data bus bit 14.
34	I/O	SD13	System data bus bit 13.
35	I/O	SD12	System data bus bit 12.
36	I/O	SD11	System data bus bit 11.
37	I/O	SD10	System data bus bit 10.
38	I/O	SD9	System data bus bit 9.
39	I/O	SD8	System data bus bit 8.
40		GND	Ground
41	I/O	SD7	System data bus bit 7.
42	I/O	SD6	System data bus bit 6.
43	I/O	SD5	System data bus bit 5.
44	I/O	SD4	System data bus bit 4.
45	I/O	SD3	System data bus bit 3.
46	I/O	SD2	System data bus bit 2.
47	I/O	SD1	System data bus bit 1.
48	I/O	SD0	System data bus bit 0.
49	I	BCHGEN	This is an enable signal to transfer the 2nd byte during 16/8 bit conversion. It is also enabled while DMA byte is transferred. This signal is active low.
50	I	BCHGDR	This signal controls the direction of the 2nd byte transfer during 16/8 bit conversion or DMA byte transfer.

Pin	I/O	Signal Name	Description
51	O	SA6	System address lines. SA8~SA0 are used during the memory refresh cycle, and SA15~SA9 are used during the CPU/DMA mode as a part of the system address. System address line bit 6.
52			Not used
53		Vcc	+ 5V
54	O	SA9	System address line bit 9.
55	O	SA7	System address line bit 7.
56	O	SA8	System address line bit 8.
57	O	SA10	System address line bit 10.
58	O	SA13	System address line bit 13.
59	O	SA11	System address line bit 11.
60	O	SA12	System address line bit 12.
61	O	SA5	System address line bit 5.
62	O	SA3	System address line bit 3.
63	O	SA4	System address line bit 4.
64	O	SA2	System address line bit 2.
65		GND	Ground
66	O	SA1	System address line bit 1.
67	O	SA14	System address line bit 14.
68	O	SA15	System address line bit 15.
69	O	SA16	System address line bit 16.
70	O	SA17	System address line bit 17.
71	O	SA18	System address line bit 18.
72	O	SA0	System address line bit 0.
73	O	SA19	System address line bit 19.
74	I	DBHEN	High bank data bus (SD15~SD8) enable signal. This is active high.
75	I	DBLEN	Low bank data bus (SD7~SD0) enable signal. This signal is active high.
76	I	LATDEN	This signal is to read the 1st byte stored in the internal buffer during 16/8 bit conversion. The 1st byte is read out when starting the 2nd byte reading if this signal is active.
77	I	CNVA0	This signal is dummy address for the 2nd byte during 16/8 bit conversion. This signal stores the 1st byte in the internal buffrer while read operation is being executed.
78		Vcc	+ 5V

Pin	I/O	Signal Name	Description
79	I	REFAD0	This signal is a refresh address (the lowest bit). It is output as SA0. This signal is also used as a clock signal for the internal refresh address counter.
80	I	REFQ1	This signal is to output the refresh address to the system bus. This signal outputs the content of the refresh address counter, when it is low.
81	I	ADSTB1	Slave DMAC address strobe signal. This signal is used to latch the DMA address which has been output on the data bus,.
82	I/O	D15	CPU data bus from / to the CPU. (D15~D8 are in the high bank, and D7~D0 are in the low bank) CPU data bus bit 15.
83	I/O	D14	CPU data bus bit 14.
84	I/O	D13	CPU data bus bit 13.
85	I/O	D12	CPU data bus bit 12.
86	I/O	D11	CPU data bus bit 11.
87	I/O	D10	CPU data bus bit 10.
88	I/O	D9	CPU data bus bit 9.
89	I/O	D8	CPU data bus bit 8.
90		GND	Ground
91	I	ADSTB2	Master DMAC address strobe signal. This signal generates DMA address. It is active high.
92	I/O	D7	CPU data bus bit 7.
93	I/O	D6	CPU data bus bit 6.
94	I/O	D5	CPU data bus bit 5.
95	I/O	D4	CPU data bus bit 4.
96	I/O	D3	CPU data bus bit 3.
97	I/O	D2	CPU data bus bit 2.
98	I/O	D1	CPU data bus bit 1.
99	I/O	D0	CPU data bus bit 0.
100			Not used.

A.4 **DATA BUS CONTROL**

This circuit controls the data bus between the CPU and I/O port or the CPU and Memory. 8/16 bit conversion is performed by this circuit.

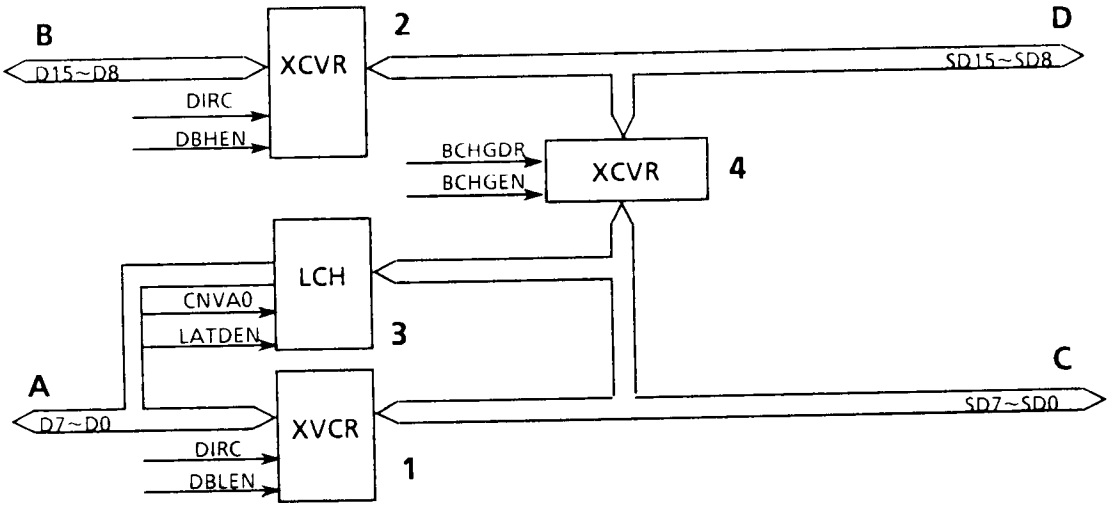


FIGURE A-2 Data Flow among the CPU, I/O Port, and Memory

A.4.1 Word access

When the I/O port connected to the data bus is word oriented, no data conversion is performed.

Low bank : A ⟷ C

High bank : B ⟷ D

(refer to Figure A-2)

In this case, read/ write cycle is completed in three CPU cycles. (No wait cycle request is included.)

A.4.2 Byte access

Following are the cases of byte access.
The I/O port is connected to the low bank of the data bus.

- Word Read Operation

The 1st data byte (even address data) transferred from **C** is latched in the buffer **3** temporarily.
The following second byte data (odd address data) is transferred to the D15-D8 (**B**) through the trsansceiver **4**.
At this time, the 1st data byte in the buffer **3** is enabled to be output to the data bus D7-D0 (**A**), thus, 16-bit data is transferred to the CPU. The transceiver **1** is disabled while the 2nd data byte is being transferred.

1st data byte : C → 3 → A

2nd data byte : C → 4 → B

(refer to Figure A-2)

- Word Write Operation

16-bit write data from the CPU is output to **A** and **B** through the data bus D15-D0.
The low bank data D8-D0 is transferred to **C** through the transceiver **1** as the 1st data byte.
The high bank data D15-19 is transferred to **C** through the transceiver **2** and trnasceiver **4** as the 2nd byte.

1st data byte : A → 1 → C

2nd data byte : B → 2 → 4 → C

(refer to Figure A-2)

The transceiver **1** is disabled during the 2nd byte transfer.
The buffer **3** is disabled while write operation is being executed.
This word/ byte conversion occupies 12 system clock cycle time.

A.4.3 DMA operation

- Byte DMA operation

DMA data transfer between I/O port connected to the low bank data bus and memory location of odd address is as follows.

Case of I/O to Memory : C ⟶ 4 ⟶ D

Case of Memory to I/O : D ⟶ 4 ⟶ C

(refer to Figure A-2)

- Word DMA operation

The GA is not concerned with the word DMA operation.

A.5 **Address Generation**

System address busses SA19-SA0 are generated in this GA, and each of these lines are used for the following purposes.

- CPU address output : SA19 - SA9
- DMA address output : SA19 - SA9, XA8
- Refresh address output : SA8 - SA0

To generate the system address, following three functional blocks are applied.

A.5.1 SA19 -SA17

SA19 - 17 come from the CPU and from the Memory Mapper GA. They are wired ORed.

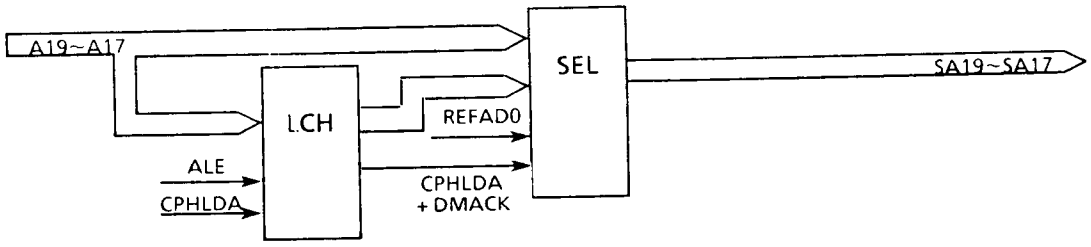


FIGURE A-3 System Address Bus 19 - 17

A.5.2 SA16 - SA9, XA8

These lines are used to output the CPU address A16-A9 to SA16 - SA9 or output the DMA address PGA16, XD7 - XD0 to SA16 - SA9, XA8.

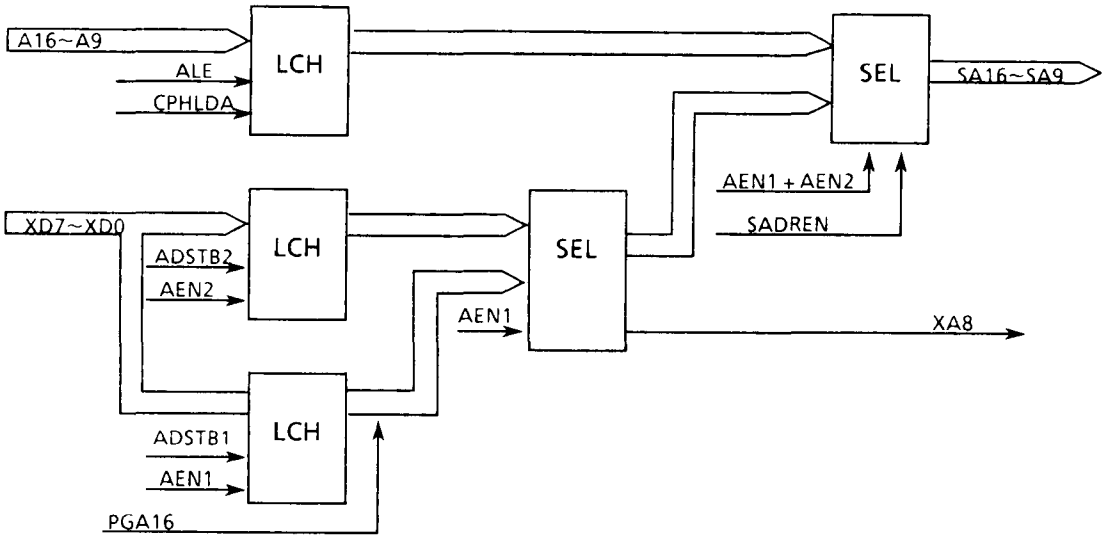


FIGURE A-4 System Address Bus SA16 - 9, XA8

A.5.3 SA8 - SA0

These address lines are used to output memory refresh address. The address is generated by refresh address counter and it is output at every 15 micro seconds.

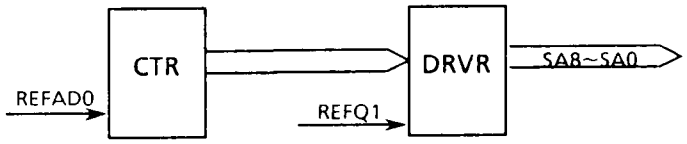


FIGURE A-5 System Address Bus SA8 - 0

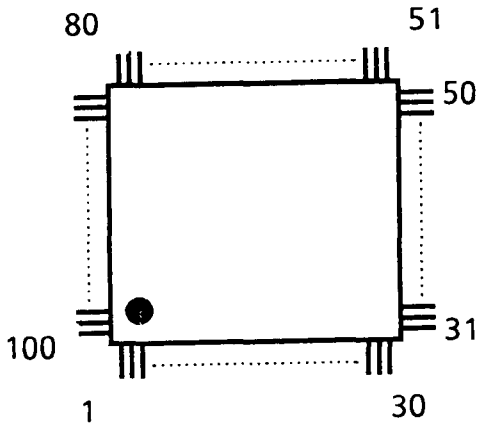
APPENDIX B

MEMORY MAPPER GA (Gate Array)

B.1 GENERAL

The Memory Mapper Gate Array is a flat package typed chip with 100 lead pins, and it contains the following functions.

- Generation of the DMA memory address.
- I/O address decoding.
- Other various functions such as;
    * ROM control signal
    * Timer clock
    * Parity error detection control
    * NMI (Non Maskable Interrupt) signal



B.2 **BLOCK DIAGRAM**

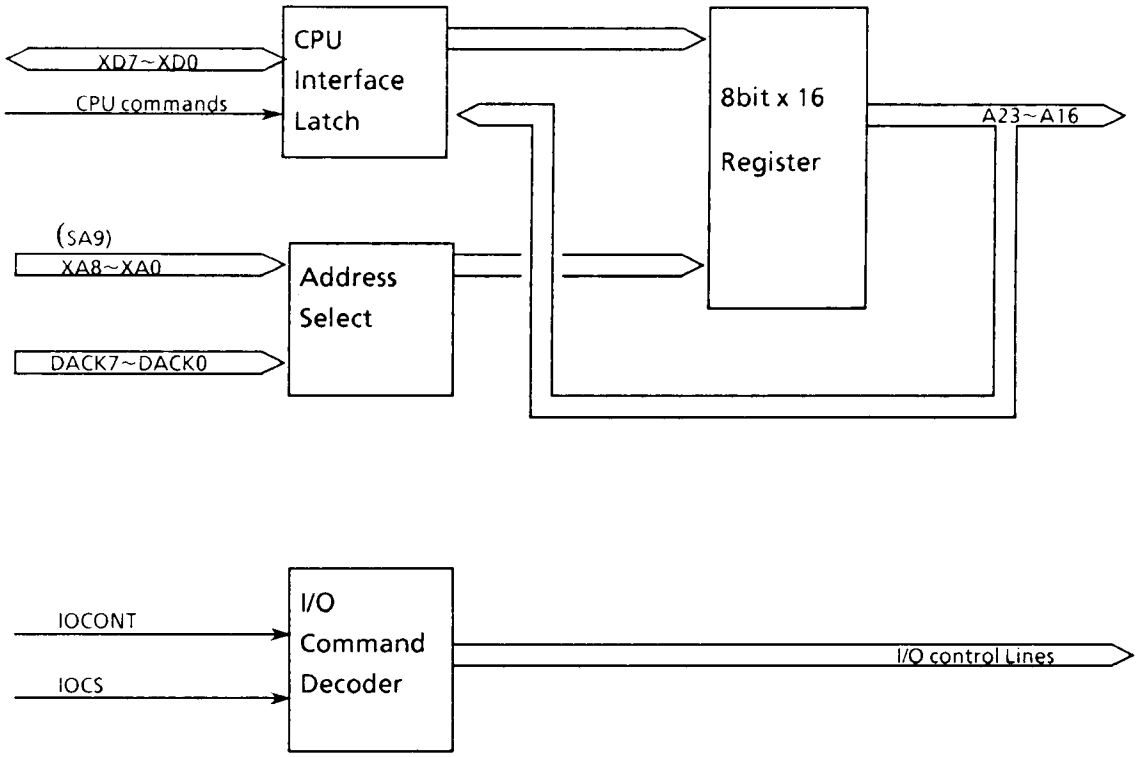


FIGURE B-1 Memory Mapper GA Block Diagram

B.3 SIGNAL DESCRIPTION AND PIN ASSIGNMENT

TABLE B-1 Pin Description

Pin	I/O	Signal Name	Description
1	I	CPHLDA	CPU hold acknowledge signal. When this signal is high, the system bus is used by any other controller than the CPU. If this signal is low, the system bus is used by the CPU.
2	I	MIO	Memory I/O select signal. When this signal is high, memory cycle is being executed, and when low, I/O cycle.
3		VCC	+5V
4	O	SPK	Buzzer signal from the external circuit.
5	O	KBCCS	Keyboard controller select signal. This signal becomes low when the I/O port address is 062H/ 068H and also KBSEL = 0, or when the address is 8062H/ 8068H.
6	O	LROMCS	Chip select signal to the BIOS ROM. This signal is active low. The address ranges are: 0E0000H~0FFFFFH FE0000H~FFFFFFH
7	O	ROMOE	Output enable signal to the BIOS ROM. This signal is generated by the ROM chip select signal and memory read command. This signal is active high.
8	O	SBHE	System bus high enable signal. This signal generates the data bus high enable signal. This signal is active low.
9	I	MEMR	Memory read command.
10	I	LATA0	This signal comes from the DMA controller GA and it is generated by SA0. When this signal is high, the low bank of the data bus is selected.
11	I	CNVALE	Dummy address latch enable signal for the 2nd byte transfer in 16/8 bit conversion. This signal also generates output enable signal of the 1st byte which has been latched.
12	O	PGA16	Address line from the Memory Mapper register during the DMA cycle or memory refresh cycle. This signal is used as the system address SA16 during the slave DMA operation.

Pin	I/O	Signal Name	Description
13	O	NDPCS	This signal defines that the NDP (80287) has been selected. If this signal is low, the system data bus is disabled. When 0F8H*SMIO*INTA1 is made, this signal is activated.
14	I	DIRC	Direction signal for CPU data transfer. When this signal is low, read data is on the data bus, and when it is high, write data is on the data bus.
15		GND	Ground
16	I	HCS1	HDD address decode signal 1 (not used).
17	O	DBLEN	Data (low bank) enable signal . This signal is generated from LATA0 signal. This signal is active high.
18	O	DBHEN	Data bus (high bank) enable signal. This signal is generated from SHBE signal. This signal is active high. each data bus is controlled inside the GA.
19	O	LATDEN	This signal is read enable signal for the 1st byte transfer in 16/8 bit conversion. The 1st byte has been stored in a buffer of the Bus Controller GA during the 1st read cycle.
20	O	NMI	NMI interrupt signal. It is active high. This signal is output when memory parity error or any error from the expansion unit occurs.
21	O	BSYCPU	CPU busy signal to NDP. This signal is active low.
22	O	IORDY	I/O channel ready signal: This signal is used to expand the NDP reset signal in order to meet the timing specification of the NDP.
23	O	ROMCS	ROM chip select signal. This signal is active low. The address ranges are: 0F0000H~0FFFFFH FE0000H~FFFFFFH
24	I	RAM16	This signal becomes low when the system memory (0~640 Kbytes) is accessed. This signal enables internal parity error detection flag.
25	O	PPICS	Peripheral I/O select signal. This signal becomes active when the I/O port address is 06*H~07*H. This signal is active low.

Pin	I/O	Signal Name	Description
26	I	PUCLR	Power on reset signal. This signal is active low. This signal inhibits real timer write command during the reset period.
27	I	IOCHK	Error signal from an external expansion unit. If this signal is low, the NMI flag becomes effective.
28		Vcc	+5V
29	I	INTA	This signal is to read the interrupt vector address. This signal comes from the interrupt controller (U8259A).
30	I	REFRSH	DMA refresh enable signal. This signal is active high. The Memory Mapper address A23~A17 and PGA16 are output during the memory refresh operation.
31	I	TM2OUT	Buzzer sound signal used in the system. This signal comes from the timer (U8254).
32	I	RESET	System reset signal. This signal is active high.
33	I	IOR	I/O read command. This signal is active low. It is used to write memory address register in the GA, system status, and also to generate command.
34	I	IOW	I/O write command. This signal is active low. It is used to write memory address sregister in the GA, or to generate various commands.
35	I	ALE	Address latch enable signal from the CPU. This signal is active high.
36	O	TMCLK	Clock signal (1.19 MHz) to the timer (U8254).
37	O	TMGATE	Count control signal to the timer. When this signal is low, it disables from counting, and when it is high, counting is enabled.
38	O	PITCS	Timer (U8254) chip select signal. This signal is active low, and becomes active when the I/O port address is 04*H~05*H.
39	O	PIC1CS	Chip select signal to the master interrupt controller (U8259A). This signal is active low, and becomes active when I/O port address is 02*H~03*H.
40		GND	Ground

Pin	I/O	Signal Name	Description
41	O	DSTRB	Data read strobe signal to the real timer. This signal becomes active when read operation to the I/O port address 071H is executed. This signal is active low.
42	I	SA14	Address line bit 14.
43	I	SA15	Address line bit 15.
44	I	DACK6	DMA acknowledge signal from channel 6.
45	I	DACK2	DMA acknowledge signal from channel 2.
46	I	DACK4	DMA acknowledge signal from channel 4.
47	I	DACK0	DMA acknowledge signal from channel 0.
48	I	DACK7	DMA acknowledge signal from channel 7.
49	I	DACK3	DMA acknowledge signal from channel 3.
50	O	IRQ13	Interrupt request signal when NDP error occurs.
51	I	MASTER	System occupation request signal from the external processor. This signal is active low.
52		KBCCS2	Chip select signal for the external 101 keyboard controller.
53		Vcc	+ 5V
54	I	NDPER	NDP error signal.
55	I	NDPBS	NDP busy signal.
56	O	KBSEL2	This signal indicates which of the two keyboard controllers (the internal one or excternal one) is selected. When this signal is "1", it shows that the external controller is selected.
57	I	SA9	Address line bit 9.
58	O	DMACK	This signal is ORed signal of CPHLDA and MASTER signals. This signal is low except in the DMA mode.
59	O	NDPRST	Reset command to the NDP. This signal is active high.
60	O	PIC2CS	Chip select signal to the slave interrupt controller (U8259A). This signal is active when the I/O port address is 0A*H~0B*H. This is active low.
61	O	DMA2CS	Chip select signal to the master DMAC (U8237). This signal is active when the I/O port address is 0C*H~0D*H. This is active low.
62	O	HCSØ	HDD address decode signal Ø (not used).
63	I	MDSPK	Buzzer sound signal from the MODEM card.

Pin	I/O	Signal Name	Description
64	I	PDINL	Parity error signal from the system memory (low bank).
65		GND	Ground
66	I	PDINH	Parity error signal from the system memory (high bank). This signal is active low. It makes an NMI interrupt signal at the rising edge of the memory read if an error occurs.
67	O	RETIMW	Data write command to the real timer. This signal becomes active when write operation to the I/O port address 071H is executed. This signal is active low.
68	O	STEP	Step signal to the FDD. This signal is active high.
69	I	RWSEK	Seek enable signal to the FDD. When this signal is low, FD seek operation is enabled, and when it is high, FDD read or write operation is enabled.
70	I	FDSTEP	Step signal from the FDC. This signal is active high.
71	O	DMA1CS	Chip select signal to the DMAC (U8237A). This signal becomes active when the I/O port address is 00*H. This signal is active low.
72	O	A23	A23~A17 are used as page address during the DMA operation. The page address from the internal register is output when the DMA acknowledge signal is low. Address line bit 23.
73	O	A22	Address line bit 22.
74	O	A21	Address line bit 21.
75	O	A20	Address line bit 20.
76	O	A19	Address line bit 19.
77	O	A18	Address line bit 18.
78	O	Vcc	+ 5V
79	O	A17	Address line bit 17.
80	I	$14MHZ	Clock signal (14.31818 MHz) to the timer (U8254).
81	I	XA0	Each of XA9~XA0 is X address which is same as the system address. They are used to decode the I/O port address or to specify the DMA page register for read/ write operation to the page address register

Pin	I/O	Signal Name	Description
82	I	XA7	X address line bit 7.
83	I	XA6	X address line bit 6.
84	I	XA5	X address line bit 5.
85	I	XA4	X address line bit 4.
86	I	XA3	X address line bit 3.
87	I	XA2	X address line bit 2.
88	I	XA1	X address line bit 1.
89	I	XA8	X address line bit 8.
90		GND	Ground
91	O	XDREAD	Read enable signal to the peripheral I/O which is connected to the X data bus. This signal is active low.
92	I/O	XD0	Each of XD7~XD0 is X data bus. Read or write operation to the DMA page register and read operation to the system status are performed through this bus. X data bus bit 0.
93	I/O	XD1	X data bus bit 1.
94	I/O	XD2	X data bus bit 2.
95	I/O	XD3	X data bus bit 3.
96	I/O	XD4	X data bus bit 4.
97	I/O	XD5	X data bus bit 5.
98	I/O	XD6	X data bus bit 6.
99	I/O	XD7	X data bus bit 7.
100	I	PDPEN	This signal indicates whether the plasma display panel is open or closed. When this signal is "1", it means that the panel is open, and therefore the plasma display can be used.

B.4 DMA MEMORY ADDRESS

DMA page address is stored in the DMA page address register in the Memory Mapper GA before it is used in the DMA cycle. The DMA page address register has 8 bit length and it is output to the address lines A23 - A17 and PGA16 during the DMA cycle.
Each DMA channel has a DMA page address register and address is assigned as follows.

TABLE B-2 Address Assignment of DMA Address Register

Adress	Channel	DMA
081H	Channel 2	Slave DMA
082H	Channel 3	"
087H	Channel 0	"
089H	Channel 6	Master DMA
08AH	Channel 7	"
08FH	* Refresh	"

To store the DMA page address, the address lines XA are decoded and the data on the XD lines are stored in the selected register.

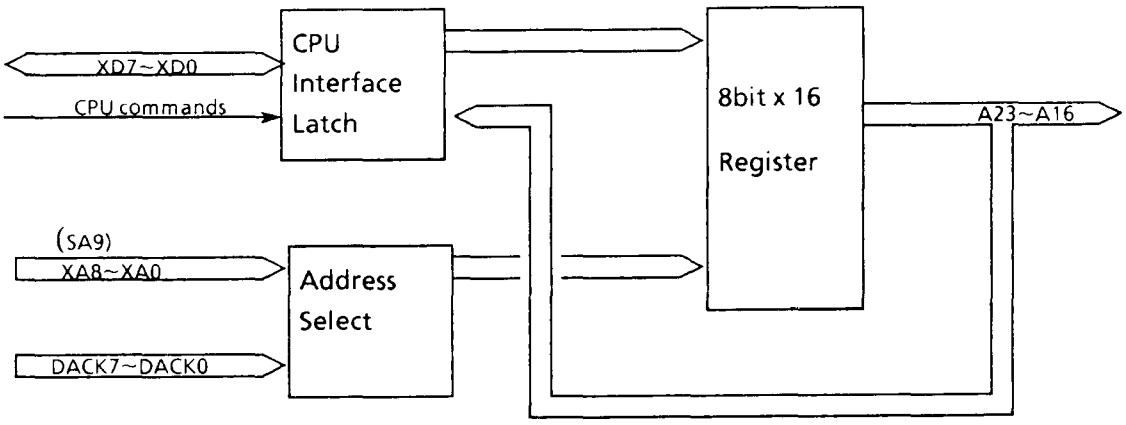


FIGURE B-2 DMA Page Address Register

B.5 I/O Decode Control

Address lines SA9 and SA8-SA5 are used to generate the I/O port select signal.
Address on the XA lines are decoded for I/O port chip select if it is not in the DMA cycle.
The following table shows the address assignment to each I/O port chip.

TABLE B-3 Address Assignment to the I/O Port

Address	Signal Name	Description
00*H~01*H	DMA1CS	Slave DMAC select
02*H~03*H	PIC1CS	Master Interrupt Controller Select
04*H~05*H	PITCS	Timer Chip Select
06*H~07*H	PPICS	Peripheral I/O Select
08*H~09*H	PREGCS	Register Select within the GA
0A*H~0B*H	PIC2CS	Slave Interrupt Controller Select
0C*H~0D*H	DMA2CS	Master DMAC Select
0E*H~0F*H	C287	NDP reset

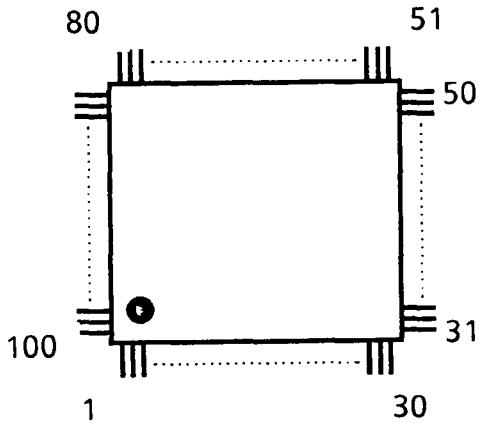
APPENDIX C

DMA GA (Gate Array)

C.1 GENERAL

The DMA Gate Array is a flat package typed chip with 100 lead pins.
The DMA Controller Gate Array has the following functions.

- Clock generator
    - CPU clock
    - DMA clock
    - Keyboard clock
- System timing control
    - Memory control (ROM, RAM)
- DMA control
- Memory refresh control
- DMA ready control
- Command generation



C.2 **BLOCK DIAGRAM**

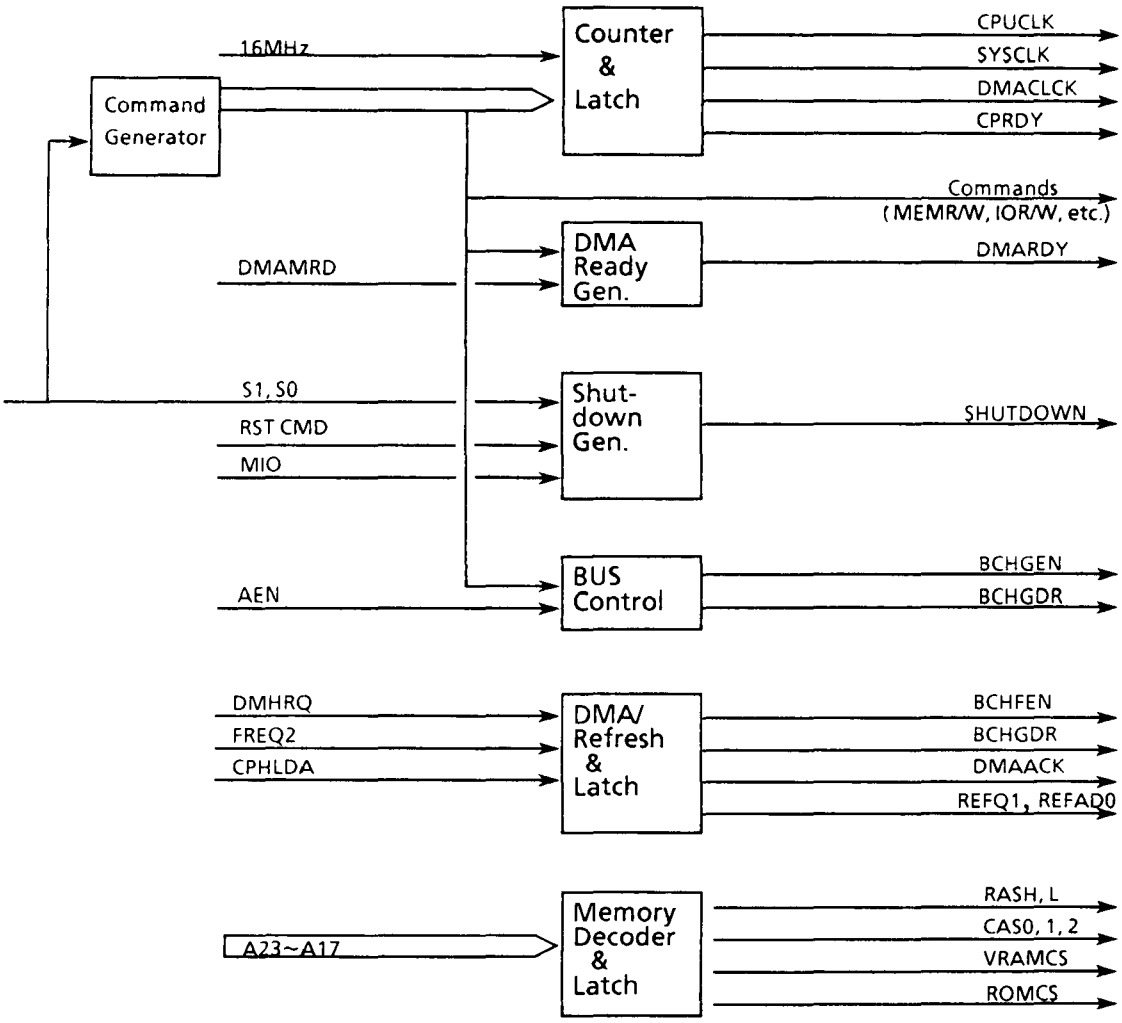


FIGURE C-1 DMA GA Block Diagram

C.3 SIGNAL DESCRIPTION AND PIN ASSIGNMENT

TABLE C-1 Pin Description

Pin	I/O	Signal Name	Description
1	I	CPHLDA	CPU hold acknowledge signal. When this signal is high, the system bus is used by any other controller than the CPU. If this signal is low, the system is used by the CPU.
2	O	ALE	CPU address latch signal. The address data is latched at falling edge of this signal.
3		VCC	+5V
4	I	AEN1	Address enable signal during the slave DMA operation. The DMA address is enabled when this signal is low.
5	I/O	IOR	I/O read command. I/O read operation is executed when this signal is low. In the master mode, this becomes an input signal.
6	I/O	IOW	I/O write command. I/O write operation is executed when this signal is low. This signal is output from the DMAC (U8237) during the DMA operation. In the master mode, this becomes an input signal.
7	I	MIO	Memory I/O select signal. When this signal is high, memory cycle is being executed, and when this signal is low, it is I/O cycle.
8	O	CLK4	12MHz clock (not used).
9	I/O	MEMR *	Memory read command. This signal is also output during the memory refresh operation. Memory read operation is done when this signal is low. In the master mode, this becomes an input signal.
10	I/O	MEMW *	Memory write command. The write operation is done when this signal is low. In the master mode, this becomes an input signal.
11	I	SEL4M	Clock rate select signal. This signal is generated by the keyboard controller to select CPU clock rate. When this signal is low, the CPU clock rate is 12 MHz, and when it is high, the CPU clock rate is 6 MHz.

Pin	I/O	Signal Name	Description
12	I	CPUA20	Output address line from the CPU. This signal is controlled inside the GA, depending on the CPU mode (Real/ Protect). In the real mode, A20 is fixed to low, and in the protect mode, CPUA2 is output to A20.
13	I	RSTCMD	CPU reset command. This signal is effective when it is low, and it outputs the CPU reset signal .
14	I	A0	CPU address line bit 0. This signal generates SA0 inside the GA.
15		GND	Ground
16	O	DIR	This signal shows the direction of data transfer. When reading, this becomes low.
17	O	FREQ	Refresh timing signal (not used).
18	O	BALE	In the CPU mode, this signal functions exactly like ALE. Apart from the CPU mode, it is always high.
19	O	NPCK	Clock signal 8MHz for the NDP (80287).
20	I	AO1	CPU address line bit 1: This signal is used to generate the "shut down" signal.
21	I	A17	CPU/ Memory mapper address. Memory Mapper address is input during the DMA operation. This signal is used to decode each memory size. CPU/ Memory Mapper Address line bit 17.
22	I	A18	Address line bit 18.
23	I	A19	Address line bit 19.
24	I/O	A20	Address line bit 20. This signal is output during the CPU operation, and when used in the real mode, it is fixed to low, while in the protect mode, CPUA2 signal is output. When the CPU is inactivated, this becomes an input signal.
25	I	A21	Address line bit 21.
26	I	A22	Address line bit 22.
27	I	A23	Address line bit 23.
28	I	Vcc	+ 5V
29	I	PAKI	Input PEACK signal from the CPU.

Pin	I/O	Signal Name	Description
30	I	REAL	Real/ Protect mode select signal. When this signal is low, the CPU is in the real mode, and when it is high, the CPU is in the protect mode.
31	O	CLK42	Keyboard controller clock signal (6MHz).
32	O	AS18	Address strobe signal to the real timer (MC146818). This signal is active low.
33	I	$24MHz	System clock signal (24 MHz)
34	O	CPRDY	CPU ready signal. This signal is active low, and is sampled by the CPU at the leading edge of the Tc cycle.
35	O	CPUCLK	CPU clock signal. Either 24 MHz or 12 MHz is output by the clock selection control.
36	I	S1	CPU bus status bit 1.
37	I	S0	CPU bus status bit 0.
38	I	NDPCS	NDP(80287) chip select signal.
39	I	TMIOUT	Memory refresh request signal
40		GND	Ground
41	I	TEST	Test signal for the GA. This signal is active high.
42	I	PPICS	Peripheral I/O select signal. This signal generates real timer address strobe signal. When I/O address is 06*h/07*h, this signal becomes low.
43	I	PUCLR	Power on reset signal. This signal is acitive low.
44	O	DMACLK	DMA clock signal.(4MHz or 2MHz)
45	O	DMARDY	Ready signal to the DMAC. One wait cycle is given in the DMA operation. When this signal is low, it gives the wait cycle, and when it is high, DMA operation is is enabled.
46	O	DMHLDA	Ack hold signal to the external DMAC. When this signal is high, it allows the DMA operation.
47	I	DMHRQ	CPU hold request signal from the external DMAC. This signal is acitve high.
48	I	DMAMRD	Memory read command from the DMAC. This signal is active low.
49	I	DACK4	Slave DMAC cycle signal. This signal is active low. The master DMAC can not output address/ command signal while this signal is active.
50	I	XA4	Address signal. CPU/ DMA address bit 4.

Pin	I/O	Signal Name	Description
51	I/O	XA0	Address signal. This signal is from SA0. It is input during the slave DMAC operation.
52	O	BUSE N	Data Enable Signal: This signal is used to enable data bus.
53		Vcc	+ 5V
54	I	PAKO	PEAK output signal to the NDP: The expanded PAKI (29 pins) signal with one more CPU clock in order to meet the timing specifications of the NDP.
55	O	SMEMR *	Memory read command. This signal is output to the 8-bit expansion bus. It is not output to any address of more than 1 M byte. This signal is active low.
56	O	SMEMW *	Memory write command. The output condition of this signal is same as that of the SMEMR signal.
57	I	IORDY	CPU ready control signal from outside the GA. When this signal is low, a wait cycle can be given.
58	O	DMAAEN	Address enable signal during the DMA operation. This signal is acive low.
59	I/O	SBHE	System bus high enable signal. This signal enables the high bank of the data when it is active. In the master mode, this signal becomes an input signal.
60	I	IO16	This signal defines that 16-bit type of I/O device is serviced in I/O command execution.
61	I	MEM16	16-bit memory access signal. This signal is to indicate that 16-bit type memory is accessed.
62	O	SYSCLK	System clock. One-third of the CPU clock frequency is output.
63	O	DM1HLD	This signal is output when DMA request signal comes from the slave DMAC. When DACK4 is low, this signal becomes active (high). The slave DMAC starts DMA operation by this.
64	I	TEST2	GA test signal: This signal is active high.
65		GND	Ground
66	O	AMEMR	Memory read signal to the T3200 system memory (including expansion memory).
67	I	TEST1	GA test signal: This signal is active low.

Pin	I/O	Signal Name	Description
68	I	REFRSH	Refersh enable signal. When this signal is high, it enbales internal memory refresh circuit.
69	O	INTA	Interrupt vector read signal. When this signal is low, system address (SA0) becomes low.
70	O	XMEMW	Memory write signal output from the DMA. When not in the DMA mode, MEMW signal is output.
71	I/O	SA0	System address. (The lowest bit)
72	I/O	XIOW	I/O write command from the DMA. Active low when CPU mode IOW signal is output.
73	I/O	XIOR	I/O read command from the DMA. Active low when CPU mode IOR signal is output.
74	I	SA16	System address line bit 16. SA16 and SA15 are used to select the video memory chips.
75	I	SA15	System address line bit 15.
76	O	CHK1	Internal monitor signal in the GA. (not used).
77	I	0WAIT	It gives 0 wait during the CPU cycle.
78		Vcc	+ 5V
79	O	CPURST	CPU reset signal. This signal is active high. When switching the power on or off, this signal becomes active.
80	I	AEN2	Address enable signal during the master DMAC operation. This signal is active low.
81	I	AMEMW	Memroy write signal to the T3200 system memory (including expanion memory)
82	I	RAMOP	This signal enables or disables to access sytem memory (512 K~640 Kbytes). When this is "0", access is enabled, and it is always set to "0" in this system.
83	O	CRTMCS	Color graphic video memory select signal. (0B8000H~0BBFFFH)
84	O	RST	System reset. This signal becomes active when the power is switched on.
85	O	REFIN	Memory refresh enable signal. This signal is active high.
86	O	REFQ1	This signal is from the memory refresh control counter. When this signal is low, the refresh address is output.
87	O	REFAD0	Memory refresh address. (The lowest bit)

Pin	I/O	Signal Name	Description
88	O	CNVA0	This signal is dummy address for 2nd byte transfer in 16/8 bit conversion. The 1st byte is latched at raising point of this signal while read operation is being executed.
89	O	BCHGDR	This signal specifies the direction of the 2nd byte transfer in 16/8 bit conversion. When this signal is low; High bank → Low bank When this signal is high; Low bank → High bank
90		GND	Ground
91	O	BCHGEN	This signal is an enable signal for the 2nd byte transfer in 16/8 bit conversion. This signal is active low.
92	O	CPUHRQ	CPU hold request signal. This signal is generated when the DMHRQ signal is high.
93	O	CHK2	Internal monitor signal inside the GA.
94	O	RAM16	System memory (0~640 Kbytes) access signal. This signal is active low. It enables the parity error detection.
95	O	CNVALE	This signal is to latch the dummy address of the 2nd byte transfer in 16/8 bit conversion. This signal is active high.
96	O	LIMSL	Output signal from the EMS GA: This signal indicates that the memory to be accessed is the system memory , and that neither VRAM nor the memory connected to the extended bus is accessed.
97	O	ROMCS	BIOS ROM chip select signal. This signal is active low. The decode ranges of the address are: 0E0000H~0FFFFH FE0000H~FFFFFH
98	O	LATA0	System address inverted signal during the CPU cycle. When this signal is high (SA0 is low), low data bus enable signal is generated.

Pin	I/O	Signal Name	Description
99	I	BHE	High data bus enable signal. When this signal is low, high bank of the data bus is accessed.
100	O	SMMW	Memory write signal supplied to the EGA GA: This signal is active when write access to the memory space between 0~1 Megabyte is executed.

In the CPU mode, signals with the mark * are output, only when VRAM or the memory connected to the expanded bus is accessed.

C.3 **CLOCK GENERATOR**

This circuitry is to generate the following cloks.
The original clock signal is a 24 MHz clock.

		Fast	Slow
CPU Clock	:	24 MHz	12 MHz
System clock	:	8 MHz	4 MHz
DMA clock	:	4 MHz	2 MHz

Following are the timing chart of the clocks.

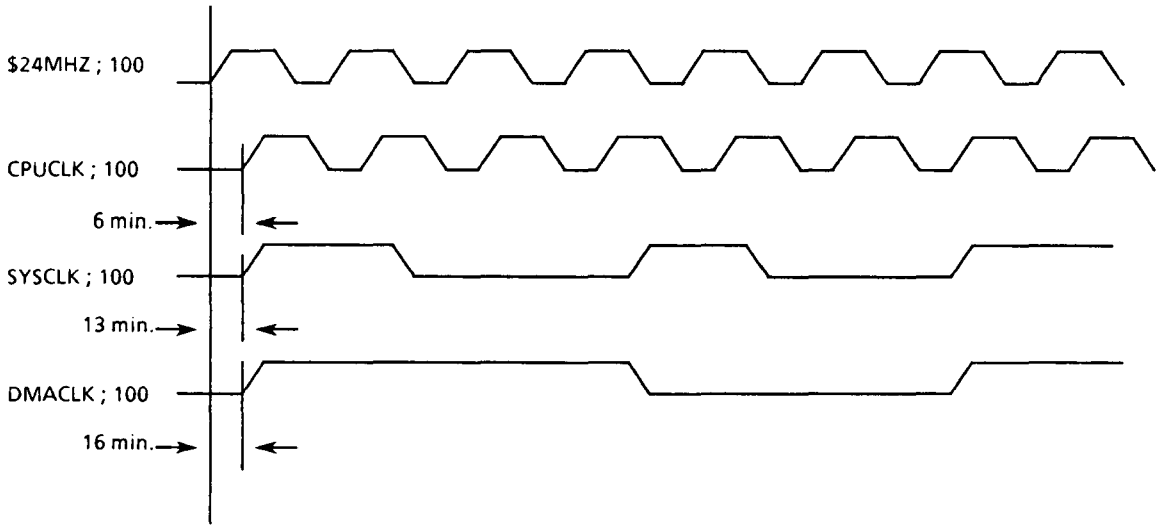


FIGURE C-2 Clock Timing Chart

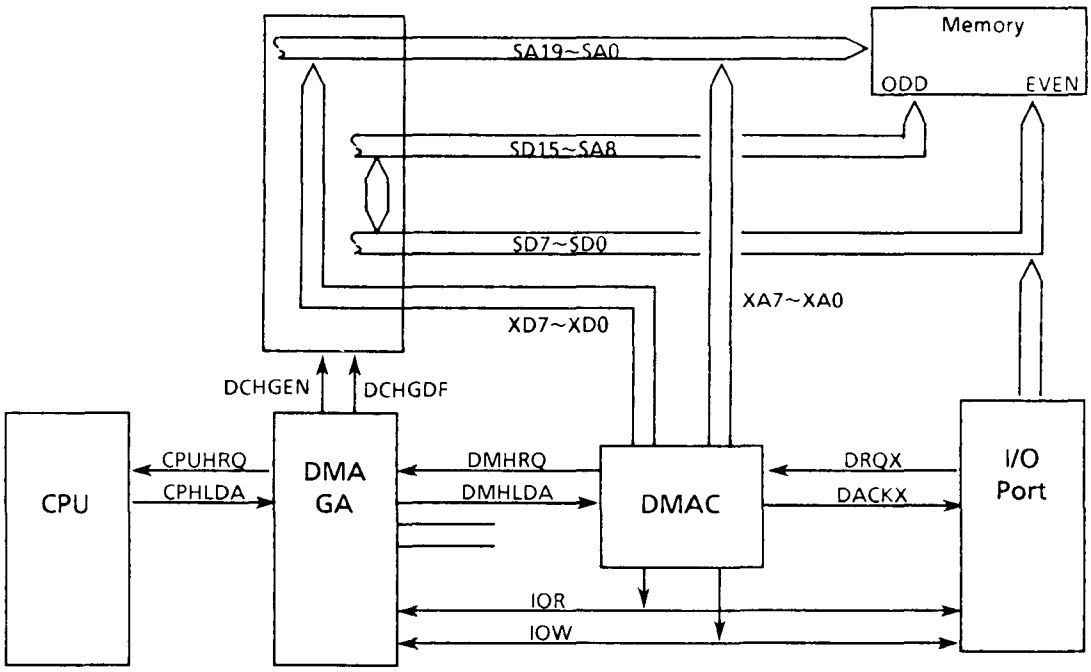


FIGURE C-3 DMA Controller

This circuitry controls the DMA operation.
The DMA GA receives DMHRQ signal from the DMAC, then the GA responds to the CPU with CPUHRQ signal.
After receiving CPHLDA signal from the CPU, the GA responds to the DMAC with DMHLDA signal.
The DMAC starts DMA operation when it receives the DMHLDA.
The DMAC prepares the DMA address on the system address bus and IOR/IOW signal to the DMA GA for the bus control. If the I/O port is byte oriented device, the bus controller GA is used for data bus switching (low bank to high bank or vice versa).

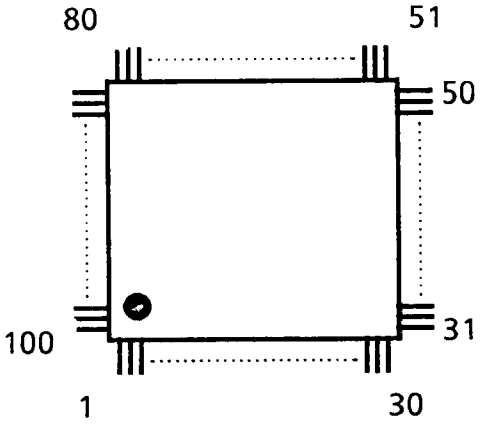
APPENDIX D

I/O CONTROLLER GA (Gate Array)

D.1 GENERAL

The I/O Controller Gate Array is a flat package type chip with 100 lead pins.
This Gate Array has the following functions.

- FDD control
- Printer control



D.2 **BLOCK DIAGGRAM**

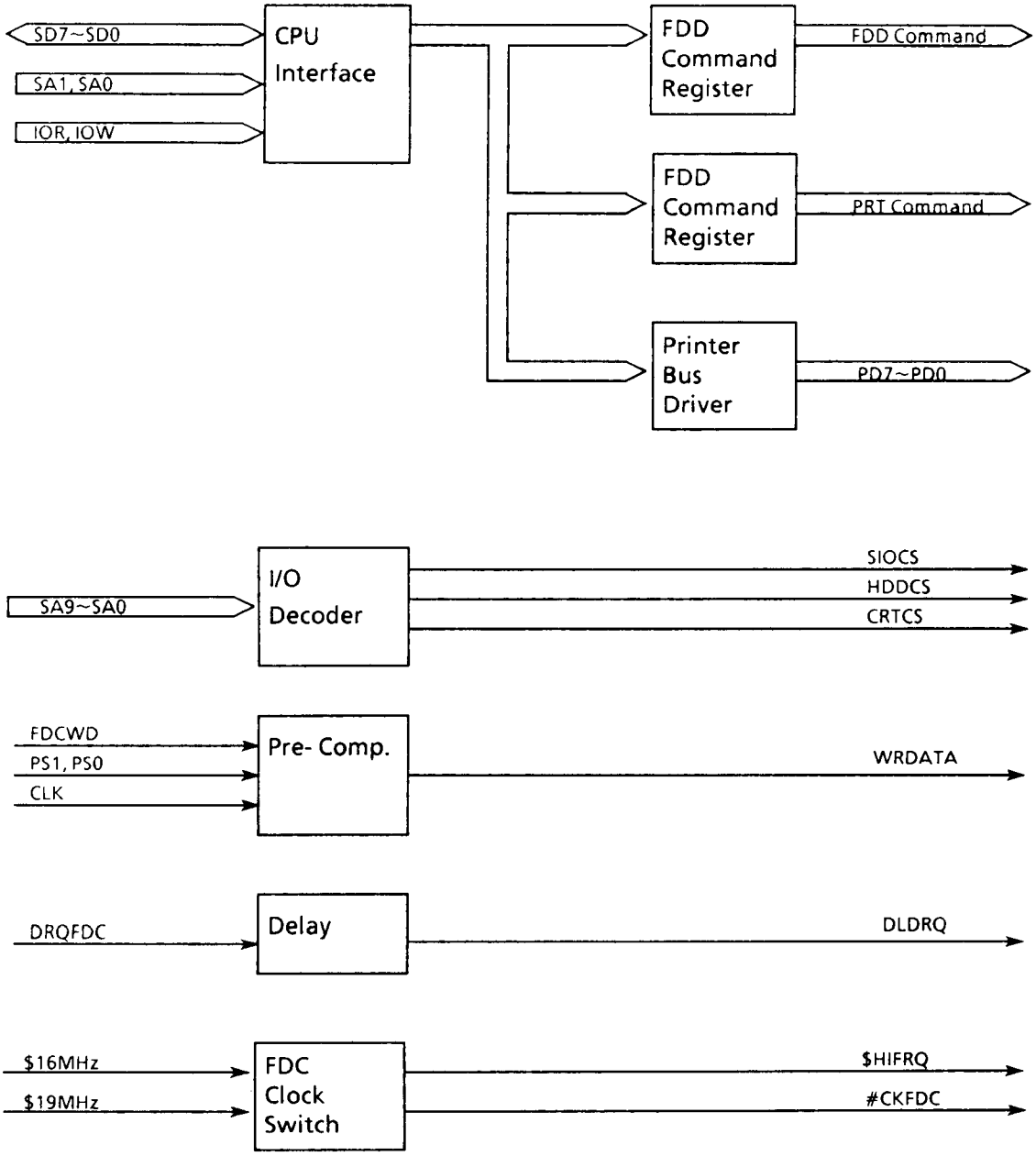


FIGURE D-1 I/O Controller GA Block Diagram

D.3 **SIGNAL DESCRIPTION ADN PIN ASSIGNMENT**

TABLE D-1 Pin Description

Pin	I/O	Signal Name	Description
1	I/O	SD0	Each of SD7~SD0 is system data bus. For printer control, this signal is used; - to output printer data. - to read printer status. - to decode printer command. For FDD control, it is used; - to decode FDD control command. System data bus bit 0.
2	I/O	SD1	System data bus bit 1.
3		Vcc	+ 5v
4	I/O	SD2	System data bus bit 2
5	I/O	SD3	System data bus bit 3
6	I/O	SD4	System data bus bit 4
7	I/O	SD5	System data bus bit 5
8	I/O	SD6	System data bus bit 6
9	I/O	SD7	System data bus bit 7
10	O	CRTCS	I/O port select signal to the color graphics controller. This signal is active (low) when the I/O port address is 3D*H. * = 0~F
11	I	SA2	SA9~SA0 is system address. They are used to decode the I/O port addresses such as; Printer/ FDD/ Color Graphics port/ HDD port/ RS232C System address line bit 2.
12	I	SA3	System address line bit 3.
13	I	SA4	System address line bit 4.
14	I	SA5	System address line bit 5.
15		GND	Ground
16	I	SA6	System address line bit 6.
17	I	SA7	System address line bit 7.
18	I	SA8	System address line bit 8.
19	I	SA9	System address line bit 9.
20	I	SA1	System address line bit 1.
21	I	PDS00	Write precompensation control. This signal is fixed to low in this system.
22	O	DRQ2	DMA cycle request signal from the FDC. This signal is active high.

Pin	I/O	Signal Name	Description
23	I	TC	This signal is a terminal count signal that indicates the end of the DMA data transfer. This signal is active high. It comes from the DMAC (U8237).
24	O	FDAKTC	Terminal count signal to the FDC. This signal is active high. It is generated from the TC signal.
25	O	FDACK	DMA acknowledge signal to the FDC. This signal is active low.
26	I	DRQFDC	DMA cycle request signal from the FDC. This signal generates DRQ2 to be sent to the DMAC. This signal is active high.
27	I	PDS01	Write precompensation ON/ OFF signal. This signal is fixed to high in this system.
28		Vcc	+ 5V
29	O	IRQ6	Interrupt request signal which the FDC outputs at the end of command execution. This signal is active high, and goes to the U8259A.
30	I	DMACK	This signal inhibits output of the I/O port address during the DMA operation. When this signal is low, decoding the address is enabled, and when high, it is disabled.
31	I	DACK2	This is acknowledge signal to DRQ2 which is DMA data transfer request signal. This signal is active low.
32	I	EXTFDD	This signal is to switch the printer port connector to the external FDD. When this signal is low, the connector is for the printer port, and when it is high, the connector is for FDD port.
33	I	$16MHZ	Basic clock to the FDC and VFO. 16 MHz (cycle time is 62.5 ns.)
34	I	$19MHZ	Basic clock to the FDC and VFO. 19.2 MHz (cycle time is 52.08 ns.)
35	O	$CKFDC	FDC clock. Frequency of the clock depends on the data transfer rate. 250 kbps; 8 MHz, 16 MHz 300 kbps; 4.8 MHz, 19.2 MHz 500 kbps; 4 MHz, 16 MHz

Pin	I/O	Signal Name	Description
36	O	$HIFRQ	VFO clock. The clock frequency depends on the data transfer rate. 250 kbps; 8 MHz 300 kbps; 9.6 MHz 500 kbps; 8 MHz
37	O	WINDOW	Window signal generated from the internal circuit. This signal is active high.
38	O	WCLK	FDD data write clock to the FDC. The cycle time of this signal is one-eighth of CKFDC.
39	O	FDCCS	Chip select signal to the FDC (U765). This signal is active (low) when the I/O port address is 3F4H/ 3F5H.
40		GND	Ground
41	I	IOR	I/O read command. This signal is active low.
42	I	IOW	I/O write command. This signal is active low.
43	O	FDSRST	FDC reset command. This signal is active high, and is issued by the command to 3F2H (data is D2).
44	I	FDCWD	Write data from the FDC. This signal is active high.
45	I	FDCINT	Interrupt signal from the FDC. This signal is active high, and generates IRQ6 signal.
46	O	XF7RD	This signal is to read the status of FDD disk change. This signal is active (low) when read address is 3F7H.
47	I	PS1	PS1 and PS0 are precompensation control signals. These signals are output from the FDC. PS0 PS1 Time Low Low No delay Low High 225~250 ns delayed High Low 225~250 ns quickened
48	I	PS0	Precompensation control signal.
49	I	SYNC	This signal is to control the VFO operation mode. When this signal is low, it inhibits the read operation, and when it is high, the read operation is enabled.

Pin	I/O	Signal Name	Description
50	I	FDCWE	Data write enable signal to the FDD. This signal is active high.
51	O	IRQEN	Printer interrupt enable signal. This signal is active low. This signal is issued by the command to 372H.
52	O	CCMICS	RS232C (Primary) select signal. This signal is active (low) when the I/O port address is 3F8H~3FFH.
53		Vcc	+5V
54	O	SWMONA	FDD motor on signal to the 1st FDD. This signal is active high. ON/OFF is controlled by the command to 3F2H.
55	O	SWMONB	FDD motor on signal to the 2nd FDD. This signal is active high. ON/OFF is controlled by the command to 3F2H.
56	O	INDRVB	Internal FDD (2nd FD) select signal. This signal is active high.
57	O	SWFDA	Internal FDD (1st FDD) select signal. This signal is active high.
58	O	XRATE0	This signal defines the FDD transfer rate. When this signal is low; 500 kbps~250 kbps When this signal is high; 300 kbps This signal is issued by the command to 3F7H.
59	I	SELECT	Printer select command. This signal is active low. It can be read from address 3F7H. This signal becomes write gate signal when it is in the external FFD mode.
60	I	BUSY	Printer busy status. This signal is active high. It can be read from the address 371H. This signal becomes motor ON/OFF signal when it is in the external FDD mode.
61	O	CBDIR	Read enable signal to the I/O peripheral which is connected to the external bus. This type of bus does not exist in this system.
62	I	STROBE	Printer strobe signal. This signal is active high. It can be read from address 371H.
63	I	AUTFD	Printer auto-feed command. This signal becomes low density signal when it is in the external FDD mode.

Pin	I/O	Signal Name	Description
64	I	PDS10	FDD precompensation ON/OFF signal. This signal is not used in this system.
65		GND	Ground
66	O	CCM2CS	RS232C (Secondary) select signal. This signal is active (low) when the I/O port address is 2F7H~2FFH.
67	I	PE	Paper end status from the printer. This signal is active high. It can be read from the address 371H. This signal becomes write data signal when it is in the external FDD mode.
68	I	PINIT	Printer initial command. This signal is active high. It can be read from address 372H. This signal becomes direction signal when It is in the external FDD mode.
69	I	SLIN	Printer select command. This signal is active high. It can be read from address 372H. This signal becomes step signal when it is in the external FDD mode.
70	I	ACK	Printer ACK status. This signal is active high. It can be read from address 371H. Select signal is input when it is in the external FDD mode,.
71	I	EROR	Printer error status. This signal is active high. It can be read from the address 371H. This signal becomes SIDE signal when it is in the external FDD mode.
72	O	EXFDWE	Write gate signal in the external FDD mode.
73	O	SWFDB	System FDD (2nd FDD) select signal. This signal is active high..
74	O	DTAREA	Read control signal to the VFO. When this signal is low, read operation is disabled, and when high, it is enabled.
75	O	EN96M	This signal is to change the value of resistance in the VFO circuit when the data transfer rate is 300 kbps. This signal is active high.
76	O	WN	Window signal from the VFO. This signal is active high.

Pin	I/O	Signal Name	Description
77	O	MINI	This signal defines the formatting mode of the disk. When this signal is low; 9 sectors/ track When this signal is high; 15 sectors/ track
78		Vcc	+ 5V
79	O	WRDATA	Write data to the FDD. This signal is active high. The precompensation is given to this write data.
80	O	HDDCS	Select signal to the external HDC. This signal is active (low) when the I/O address is 170H~177H.
81	O	PRTDIR	This signal controls the direction of printer data port. When this signal is low; External → Internal. When this signal is high; Internal → External. This function is ignored when it is in the external FDD mode.
82	I/O	PD7	Each of PD7~PD0 is a printer or parallel data IN bus. When it is in the external FDD mode, each bus is in the high impedance state. When printer is connected, they are in the output mode. Printer data bus bit 7.
83	I/O	PD6	Printer data bus bit 6.
84	I/O	PD5	Printer data bus bit 5.
85	I/O	PD4	Printer data bus bit 4.
86	I/O	PD3	Printer data bus bit 3.
87	I/O	PD2	Printer data bus bit 2.
88	I/O	PD1	Printer data bus bit 1.
89	I/O	PD0	Printer data bus bit 0.
90		GND	Ground
91	O	SLCTIN	Printer select command. This signal is active high. This signal is issued by the command to address 372H.
92	O	AUTFD	Printer auto-feed command. This signal is active high, and is issued by the command to address 372H.

Pin	I/O	Signal Name	Description
93	O	INIT	Printer initial command. This signal is active low, and is issued by the command to address 372H.
94	O	STROBE	Printer strobe command. This signal is active high, and is issued by the command to address 372H.
95	I	DIREN	This signal is to control the direction of the printer data bus. When this signal is low, it is in the parallel IN mode, and when it is high, it is in the printer output mode.
96	O	FDSLSEN	This signal is to read the FDD interface signal as below, when it is in the external FDD mode. INDEX/ TRAWCK 0/ WRITE PROTECT/ READ DATA/ DISK CHANGE/ READY This signal is active low.
97	I	SA0	Address line. This signal is used to generate printer/ FDD control command.
98	I	RST	Initial reset signal. This signal is active low. Internal counters and F/Fs are reset by this signal.
99	I	FSELSW	This signal is to change the drive number of the internal FDD. When this signal is low, the drive number is changed to B, and when high, it is changed to A (Normal).
100		GND	Ground.

APPENDIX E

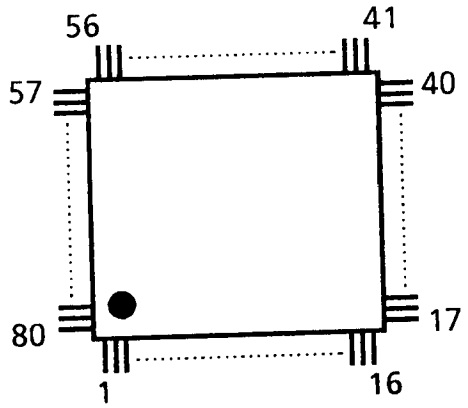
EMS GA (Gate Array)

E.1 GENERAL

This chip allows application programs to access a vast memory space by the bank switching operation, through a certain memory address which is used as a window .

This Gate Array is used for address conversion, and it stores page control registers, map registers, CPU/ DMA address decoder and so on.

The EMS Gate Array is a flat package typed chip, and is composed of 80 lead pins.



E.2 **BLOCK DIAGRAM**

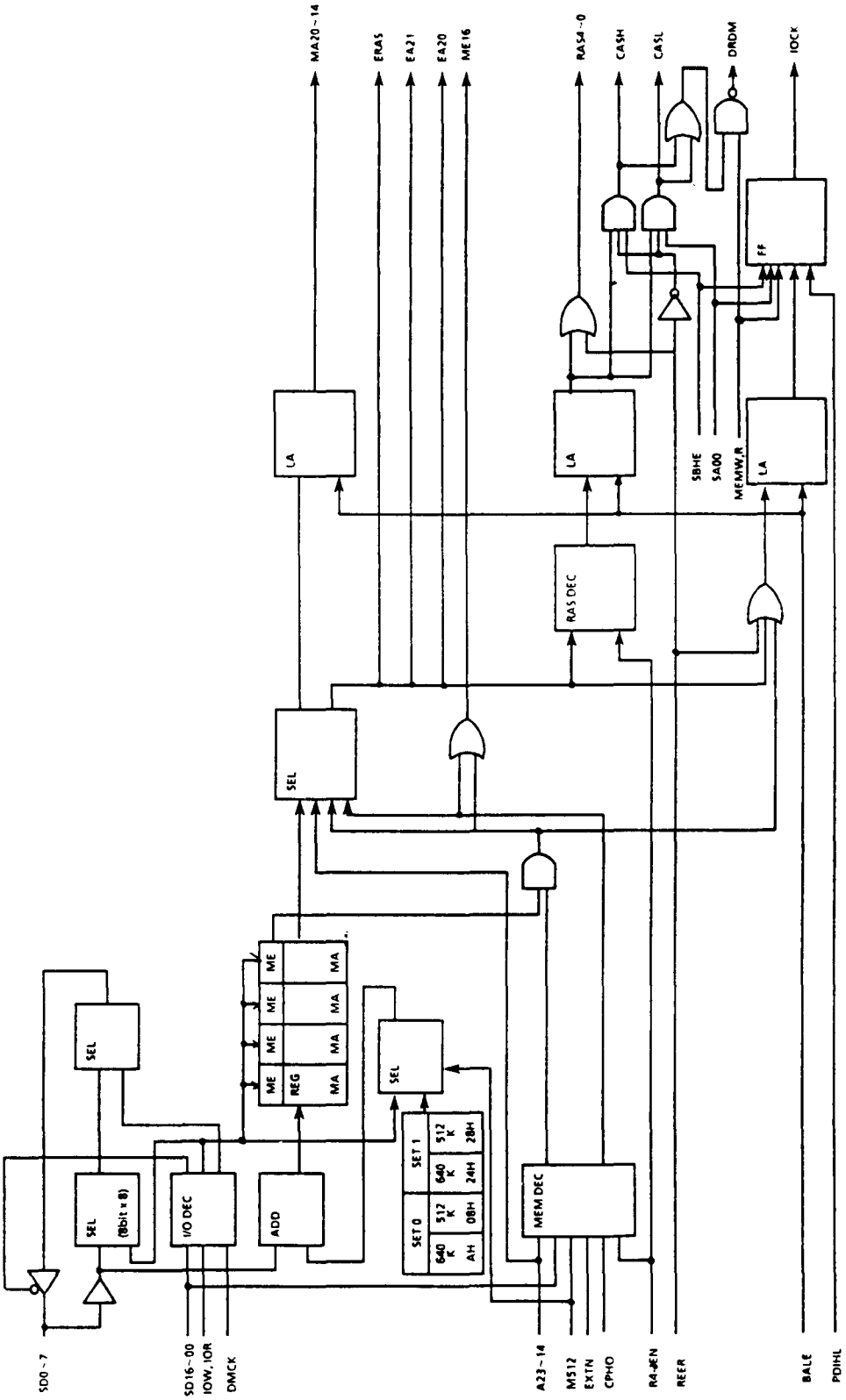


FIGURE E-1 EMS GA Block Diagram

E.3 SIGNAL DESCRIPTION AND PIN ASSIGNMENT

TABLE E-1 Pin Description

Pin	I/O	Signal Name	Description
1	I	RSET	Reset signal. This signal is active high.
2		GND	Ground
3	I	EXTND	Extended memory access disable select.
4	I	M512K	Conventional memory 512 Kbytes/ 640 kbytes select
5	I	SBHE	Bus high enable signal.
6	I	BALE	Address latch enable signal.
7	I	REFRSH	Refresh signal.
8	I	DMACK	DMA acknowledge signal.
9	I	MEMR	Memory read command
10	I	XIOR	I/O read command
11	I	XIOW	I/O write command
12		GND	Ground
13	O	EA20	Unlatched MA20
14	O	EA21	Unlatched MA21
15	I	SA16	Address bus 16
16	I	SA15	Address bus 15
17	I	SA14	Address bus 14
18	I	SA13	Address bus 13
19	I	SA12	Address bus 12
20	I	SA11	Address bus 11
21	I	SA10	Address bus 10
22	I	SA09	Address bus 09
23		GND	Ground
24	I	SA08	Address bus 08
25	I	SA07	Address bus 07
26	I	SA06	Address bus 06
27	I	SA05	Address bus 05
28	I	SA04	Address bus 04
29	I	SA03	Address bus 03
30	I	SA02	Address bus 02
31	I	SA01	Address bus 01
32	I	SA00	Address bus 00
33		Vcc	+ 5v
34	I/O	SD0	Data bus 0
35	I/O	SD1	Data bus 1
36	I/O	SD2	Data bus 2

Pin	I/O	Signal Name	Description
37	I/O	SD3	Data bus 3
38	I/O	SD4	Data bus 4
39	I/O	SD5	Data bus 5
40	I/O	SD6	Data bus 6
41	I/O	SD7	Data bus 7
42		GND	Ground
43	O	MA20	RAM address 20
44	O	MA19	RAM address 19
45	O	MA18	RAM address 18
46	O	MA17	RAM address 17
47	O	MA16	RAM address 16
48	O	MA15	RAM address 15
49	O	MA14	RAM address 14
50	I	PDINH	RAM parity set H
51	I	PDINL	RAM parity set L
52		GND	Ground
53	O	CASLSL	RAM CAS enable L
54	O	CASHSL	RAM CAS enable H
55	O	RAS4SL	RAM RAS enable signal 4
56	O	RAS3SL	RAM RAS enable signal 3
57	O	RAS2SL	RAM RAS enable signal 2
58	O	RAS1SL	RAM RAS enable signal 1
59	O	RAS0SL	RAM RAS enable signal 0
60	I	RAS4EN	RAS4 enable signal
61	I	RAS3EN	RAS3 enable signal
62	I	RAS2EN	RAS2 enable signal
63		GND	Ground
64	I	MEMWE	Memory write command
65	I	A23	Unlatched address bus 23
66	I	A22	Unlatched address bus 22
67	I	A21	Unlatched address bus 21
68	I	A20	Unlatched address bus 20
69	I	A19	Unlatched address bus 19
70	I	A18	Unlatched address bus 18
71	I	A17	Unlatched address bus 17

Pin	I/O	Signal Name	Description
72	I	A16	Unlatched address bus 16
73		Vcc	+ 5v
74	I	A15	Unlatched address bus 15
75	I	A14	Unlatched address bus 14
76	O	ERAS	Unlatched OR of MA22, 23
77	O	MEM16	Memory word transfer signal
78	O	DRMRD	RAM data enable
79	O	IOCHK	RAM parity error
80	I	CPHLDA	CPU hold signal

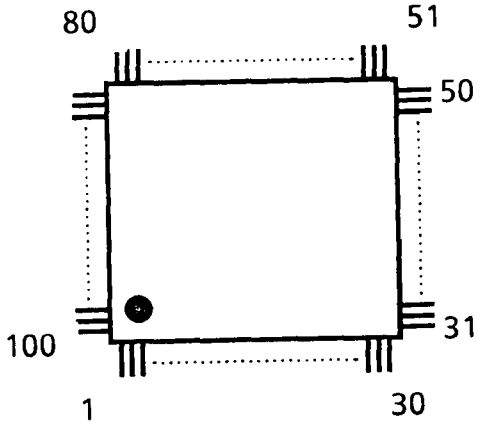
APPENDIX F

AGS.GA (Gate Array)

F.1 GENERAL

AGS stands for Advanced Graphics Subsystem, and is used together with the PEGA2 chip to realize the function of 640 x 400 mode graphics in the CRT or Plasma display.

AGS Gate Array is a flat package typed chip with 100 lead pins in total.



F.2 **BLOCK DIAGRAM**

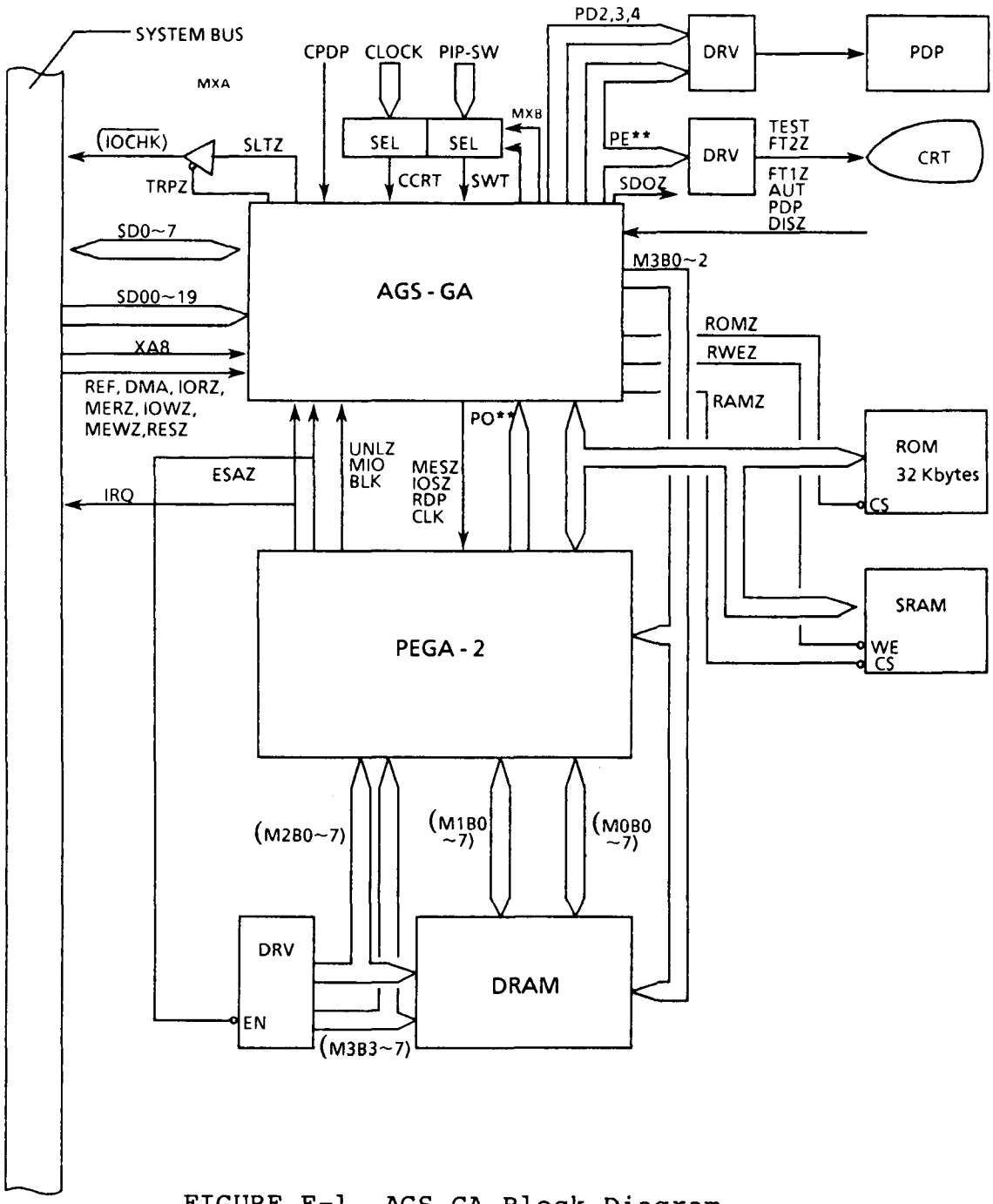


FIGURE F-1 AGS.GA Block Diagram

F.3 SIGNAL DESCRIPTION AND PIN ASSIGNMENT

TABLE F-1 Pin Description

Pin	I/O	Signal Name	Description
1	O	MUXB	Multiplex Select A External Clock/ Dip switch select signal
2	O	MUXA	Multiplex Select B External Clock/ Dip switch select signal
3		Vcc	+ 5V
4	O	RAMCS	SRAM chip select signal
5	O	RAMWE	SRAM write enable signal
6	I	DMACK	System bus address enable signal
7	I	SMEMW	Memory write command
8	I	SMEMR	Memory read command
9	I	IOW	I/O write command
10	I	IOR	I/O read commad
11	I	AUTOSW	This signal is ued to power on the Auto-switch (DIP-SW1) concernig bit 7of the PEGA2 status read port.
12	I	FONT	This signal is used to select double or single FONT (DIP-SW4) concernig bit 5 of the PEGA2 status read port.
13	I	DSPDIS	This signal is used to disable the system
14	I	CGFONT	This signal is used to select Sacandinavian or Normal FONT (DIP-SW6) concernig bit 4 of the PEGA2 status read port.
15		GND	Ground
16	I	REFRSH	System bus memory refresh signal. When this is low, memory access is enabled.
17	I	SWTCH	Status signal from the external 4-bit Display type select switch.
18	I	RESET	System bus reset signal
19	I	IRQ9	CRT interrupt signal. This signal is output from the PEGA2, and can be read at the bit 7 of 3C2 port.
20	I	BLANK	This is the signal to indicate that blanking is being executed.
21	I	MIOSL	This is the signal to select Memory or I/O.
22	I	POVS	CRT display signal from the PEGA2.
23	I	POHS	CRT display signal from the PEGA2.
24	I	POSB	CRT display signal from the PEGA2.
25	I	POSG	CRT display signal from the PEGA2.
26	I	POBL	CRT display signal from the PEGA2.
27	I	POGR	CRT display signal from the PEGA2.

Pin	I/O	Signal Name	Description
28		Vcc	+ 5V
29	I	PORE	CRT display signal from the PEGA2.
30	I	POSR	CRT display signal from the PEGA2.
31	O	READ	PEGA read / write select signal
32	O	IOSEL	I/O select signal
33	O	MEMSL	PEGA memory select signal
34	O	ROMSL	ROM chip select signal
35	I	CLKMUX	Basic clock for CRT display
36	I	PDPSL	Plasma/ CRT select signal
37	I	UNL	This signal is to indicate that the content of the port 3D8 has already been read twice. This is cleared by the next read or write signal.
38	O	CLK	Basic clock for display. This is output to the PEGA.
39	I	CLKPDP	Basic clock for Plasma display
40		GND	Ground
41		GND	Ground
42	O	SRON	This signal is to enable the SR signal. When this is high, CRT output pin No.2 is grounded.
43	O	SLT	NMI generate timing signal
44	O	M3DA2	Address data bit 2 of the DRAM plane 3. In this GA, system address bus is output to the PEGA.
45	O	M3DA1	Address data bit 1 of the DRAM plane 3.
46	O	M3DA0	Address data bit 0 of the DRAM plane 3.
47	I	XA8	I/O port address bit 8 for display When XA8 = SA8, the port 3XX is accessed. " XA8 = SA8, the port 2XX is accessed.
48	I	ESA	PEGA system address input enable signal. When this is low, system address is output to M3 bus.
49	O	TRP	Trap (NMI) generate signal
50	O	PEPD4	Plasma display signal. This signal is active low.
51	O	PEGR	Pins 51, 54, 55, 57, 58, 59, 60, 61 are used for selection of CRT or Plasma display as follows, depending on their combinations. CRT / PDP PEVS (Pin 58) 9Pin VS PEHS (Pin 59) 8pin HS PESB (Pin 54) 7pin PD1 PESG (pin 55) 6pin PS4 PEBL (pin 61) 5pin PS3 PEGR (pin 51) 4pin PS2 PERE (pin 57) 3pin PS1 PESR (pin 60) 2pin SCK

Pin	I/O	Signal Name	Description
52	O	PEPD2	Plasma display signal. This signal is active low.
53		Vcc	+ 5V
54	O	PESB	Refer to the description of the pin 51.
55	O	PESG	Refer to the description of the pin 51.
56	O	PEPD3	Plasma display signal. This signal is active low.
57	O	PERE	Refer to the description of the pin 51.
58	O	PEVS	Refer to the description of the pin 51.
59	O	PEHS	Refer to the description of the pin 51.
60	O	PESR	Refer to the description of the pin 51.
61	O	PEBL	Refer to the description of the pin 51.
62	I	SA8	system address bus bit 8.
63	I	SA7	system address bus bit 7.
64	I	SA6	system address bus bit 6.
65		GND	Ground
66	I	SA5	system address bus bit 5.
67	I	SA4	system address bus bit 4.
68	I	SA3	system address bus bit 3.
69	I	SA2	system address bus bit 2.
70	I	SA1	system address bus bit 1.
71	I	SA0	system address bus bit 0.
72	I/O	SD0	System data bus bit 0.
73	I/O	SD1	System data bus bit 1.
74	I/O	SD2	System data bus bit 2.
75	I/O	SD3	System data bus bit 3.
76	I/O	SD4	System data bus bit 4.
77	I/O	SD5	System data bus bit 5.
78		Vcc	+ 5V
79	I/O	SD6	System data bus bit 6.
80	I/O	SD7	System data bus bit 7.
81	I	SA19	system address bus bit 19.
82	I	SA18	system address bus bit 18.
83	I	SA17	system address bus bit 17.
84	I	SA16	system address bus bit 16.
85	I	SA15	system address bus bit 15.
86	I	SA14	system address bus bit 14.
87	I	SA13	system address bus bit 13.
88	I	SA12	system address bus bit 12.
89	I	SA11	system address bus bit 11.
90		GND	Ground

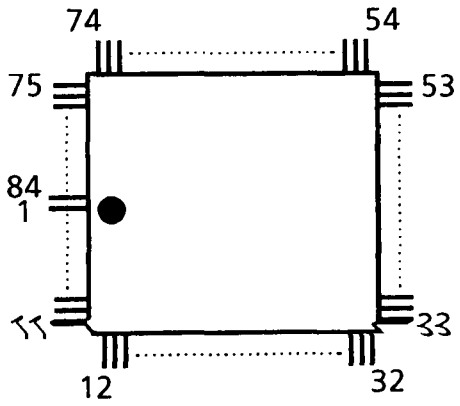
Pin	I/O	Signal Name	Description
91	I	SA10	system address bus bit 10.
92	I	SA9	system address bus bit 9.
93	I/O	LD7	Local data bus 7 among PEGA, ROM, and SRAM.
94	I/O	LD6	Local data bus 6 among PEGA, ROM, and SRAM.
95	I/O	LD5	Local data bus 5 among PEGA, ROM, and SRAM.
96	I/O	LD4	Local data bus 4 among PEGA, ROM, and SRAM.
97	I/O	LD3	Local data bus 3 among PEGA, ROM, and SRAM.
98	I/O	LD2	Local data bus 2 among PEGA, ROM, and SRAM.
99	I/O	LD1	Local data bus 1 among PEGA, ROM, and SRAM.
100	I/O	LD0	Local data bus 0 among PEGA, ROM, and SRAM.

APPENDIX G

PEGA2

G.1 GENERAL

The PEGA2 is a single solution for design of a video controller.
This chip is composed of 84 pins with 40 multiplexed bidirectional signals for handling RAM address and data, CPU address and data, as well as various I/O bits.
Four busses of 8 bits each connect to the four banks of DRAM, and the fifth 8 bits is used for CPU address and data.



G.2 **BLOCK DIAGRAM**

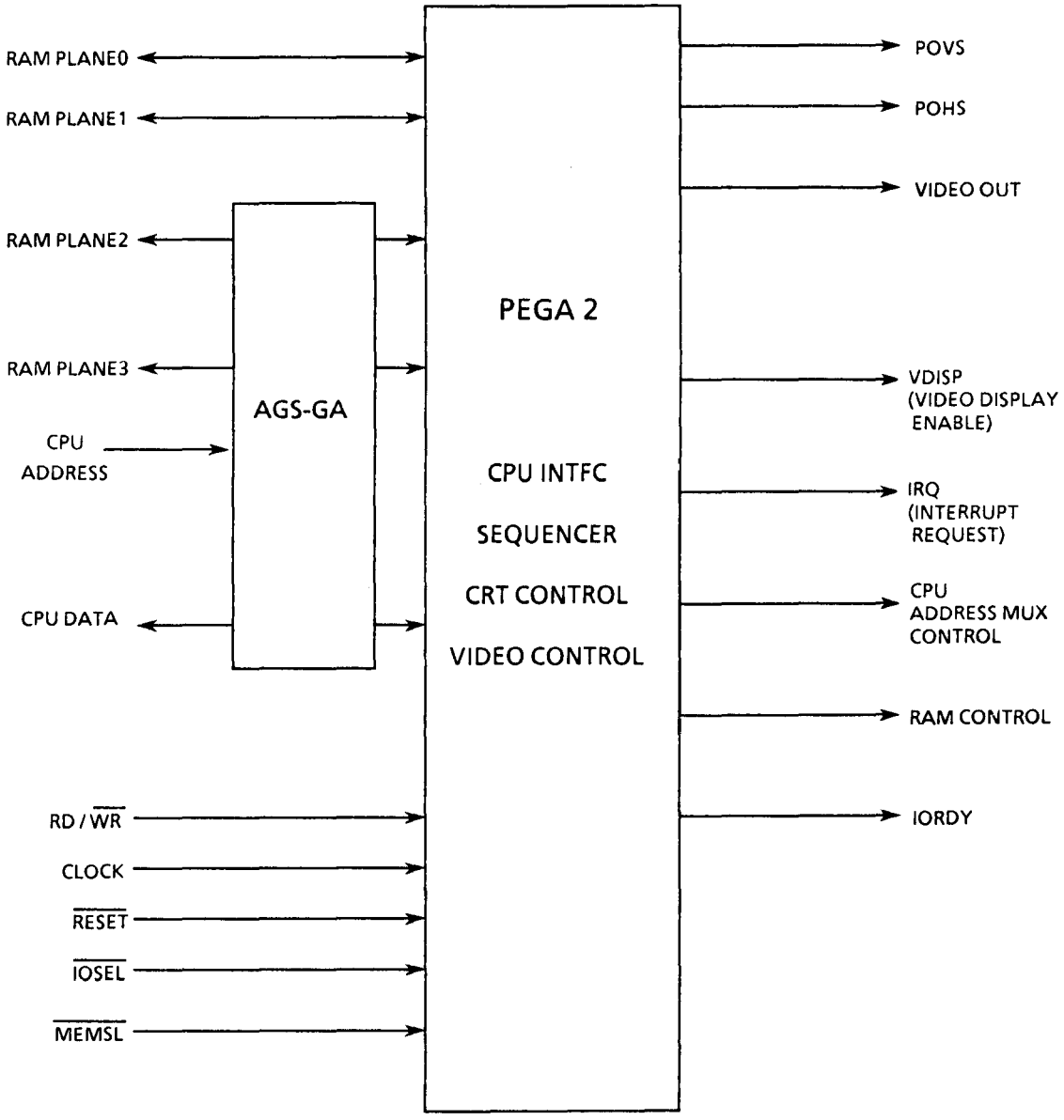


FIGURE G-1 PEGA2 Block Diagram

The PEGA2 uses 64Kx4 DRAMs with one RAM bank consisting of 2 chips. Within a bank, one chip connects 4 data lines to the low 4 bus signals and the other chip connects 5 data lines to the high 4 bus signals.
The RAS, CAS, and OE signals are common to all 4 banks, but each bank uses a separate WE signal.

The signals required for controlling the external bus multiplexers are generated with a minimum of additional logic. External logic as also required for PC bus interface functions, including address decoding, bus direction control and interrupt handling.

The eight video outputs of the PEGA2 are designed to drive a 9-pin monitor cable directly. Switching logic inside the PEGA 2 correctly configures the video data signals (RrGgBb, IRGB or Video/ Intensity) for the particular monitor being driven.

A TTL-compatible clock, up to 26 MHz drives the PEGA2.
A reset pin initializes the chip and a total of 12 pins are used for power and ground connections.

F.3 **SIGNAL DESCRIPTION AND PIN ASSIGNMENT**

TABLE G-1 Pin Description

Pin	I/O	Signal Name	Description
1		GND	Ground
2	I/O	M3DA-4	Memory data and address bit 4, plane 3. CPU address bit 10 at ESAN.
3	I/O	M3DA-5	Memory data and address bit 5, plane 3. CPU address bit 11 at ESAN.
4	I/O	M3DA-6	Memory data and address bit 6, plane 3. CPU address bit 12 at ESAN.
5	I/O	M3DA-7	Memory data and address bit 7, plane 3. CPU address bit 13 at ESAN.
6	I/O	M2DA-0	Memory data and address bit 0, plane 2. CPU address bit 14 at ESAN.
7	I/O	M2DA-1	Memory data and address bit 1, plane 2. LIGHT PEN Switch at ESAN.
8	I/O	M2DA-2	Memory data and address bit 2, plane 2.
9	I/O	M2DA-3	Memory data and address bit 3, plane 2.
10 11	O	FCV0 FCV1	Active low, bits D0 and D1of Figure Control Register at I/O port 3XA; supplied to Feature Connector.
12	I/O	M2DA-4	Memory data and address bit 4, plane 2.
13	I/O	M2DA-5	Memory data and address bit 5, plane 2.
14	I/O	M2DA-6	Memory data and address bit 6, plane 2.
15		GND	Ground
16	I/O	M2DA-7	Memory data and address bit 7, plane 2.
17	I/O	SD0	CPU data bit 1
18	I/O	SD1	CPU data bit 2
19	I/O	SD2	CPU data bit 3
20	I/O	SD3	CPU data bit 4
21		Vcc	+ 5V
22		GND	Ground
23	I/O	SD4	CPU data bit 5
24	I/O	SD5	CPU data bit 6
25	I/O	SD6	CPU data bit 7
26	I/O	SD7	CPU data bit 8
27	I/O	IRQ9	Active high, indicates that an interrupt has been generated. Can be set to high impedance under program control (3X5-11H, bit5). Gets read as STATUS 0, bit 7.

Pin	I/O	Signal Name	Description
28	O	IORDY	Active high, indicates that memory access has been completed. When it is low,it is used to cause wait states to be inserted into the memory access cycles. It is high impedance when memory is not selected.
29		GND	Ground
30	O	COE	Active low, output enable for video planes
31	O	ESA	Active low enable for system address bits (6~13,14) and LPSW multiplexed with memory data/ address bits (see above).
32	O	CCAS	Active low, column address strobe
33	O	MIOSL	Active high, Memory or I/O selected. Controls external data bus driver.
34	O	GRAPH	Active high, indicates that a graphics mode is active; low indicates alphanumeric mode.
35	O	RAS	Active low, row address strobe.
36		CW0	Active low, write signal for video plane 0
37		CW1	Active low, write signal for video plane 1
38		CW2	Active low, write signal for video plane 2
39		CW3	Active low, write signal for video plane 3
40	I	RESET	Active low, master reset supplied by external power on circuitry.
41	I	CLOCK	26.0 MHz max.
42	I	READ	Active high while reading PEGA I/O port or video memory.
43		GND	Gound
44		Vcc	+ 5V
45	I	IOSEL	Active low. I/O select indicates accessing any PEGA I/O port.
46	I	MEMSL	Active low. memory select indicates accessing video memory.
47		Vcc	+ 5V
48	O	POHS	Horizontal Sync Signal
49	O	POVS	Vertical Sync Signal (active low for monochrome monitors and IBM Enhanced Color Display).
50	O	POSR	Secondary Red Output
51	O	POSG	Secondary green output or intensity
52	O	BLANK	Active high, Horizontal or Vertical blanking for use with feature connector.
53	O	ATRSLN	Active low, Attribute/ shift load for use with feature connector.

Pin	I/O	Signal Name	Description
54	O	VDISP	Active high, Video display enable, indicates active video (unblanked, not border).
55	O	POSB	Secondary blue output or monochrome video.
56	O	PORE	Primary red output
57	O	POGR	Primary green output
58	O	POBL	Primary blue output
59	I/O	M1DA0	Memory data and address bit 0, plane 1.
60	I/O	M1DA1	Memory data and address bit 1, plane 1.
61	I/O	M1DA2	Memory data and address bit 2, plane 1.
62	I/O	M1DA3	Memory data and address bit 3, plane 1.
63	I/O	M1DA4	Memory data and address bit 4, plane 1.
64		GND	Ground
65		Vcc	+ 5V
66	I/O	M1DA5	Memory data and address bit 5, plane 1.
67	I/O	M1DA6	Memory data and address bit 6, plane 1.
68	I/O	M1DA7	Memory data and address bit 7, plane 1.
69	I/O	M0DA0	Memory data and address bit 0, plane 0.
70	I/O	M0DA1	Memory data and address bit 1, plane 0.
71		GND	Ground
72	I/O	M0DA2	Memory data and address bit 2, plane 0.
73		M0DA3	Memory data and address bit 3, plane 0.
74		M0DA4	Memory data and address bit 4, plane 0.
75		Vcc	
76	O	UNLOCK	Active low, goes active after two successive reads of the old mode register(3D8 or 3B8). Goes inactive at the end of of the next /O read or write cycle.
77	I/O	M0DA5	Memory data and address bit 5, plane 0.
78	I/O	M0DA6	Memory data and address bit 6, plane 0.
79	I/O	M0DA7	Memory data and address bit 7, plane 0.
80	I/O	M3DA0	Memory data and address bit 0, plane 3. CPU address bit 6 at ESAN
81	I/O	M3DA1	Memory data and address bit 1, plane 3. CPU address bit 7 at ESAN
82	I/O	M3DA2	Memory data and address bit 2, plane 3. CPU address bit 8 at ESAN
83	I/O	M3DA3	Memory data and address bit 3, plane 3. CPU address bit 9 at ESAN
84		Vcc	+ 5V