IM4116/MK4116
16,384 Bit
NMOS Dynamic RAM

FEATURES

- Industry Standard 16-pin configuration
- Standard 10% Supplies (+12V, +5V, −5)
- Low Capacitance TTL Compatible Inputs
- TTL Compatible 3-State Outputs Controlled by CAS
- On-chip Address and Data Latches
- Common I/O Capability Using "Early Write" Cycle
- Read-Modify-Write, RAS-only Refresh, Page Mode Operation
- 128-Cycle RAS-Only Refresh
- Compatible with MOSTEK MK4116
- Read Access

4116-2	150 nS
4116-3	200 nS
4116-4	250 nS

- Page Mode Access

4116-2	100 nS
4116-3	135 nS
4116-4	165 nS

GENERAL DESCRIPTION

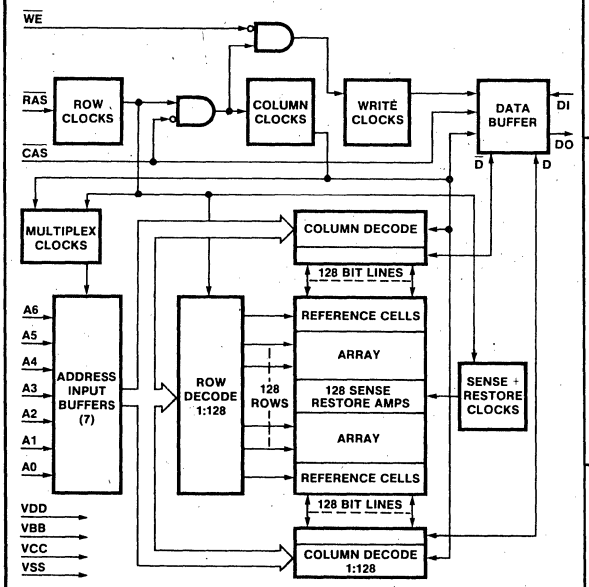
The Intersil IM4116/MK4116 is a 16,384-bit dynamic random access memory employing the latest advances in N-channel silicon-gate MOS technology. The use of double-level poly allows the highest possible density consistent with reliability, high performance and low cost.

The basic memory element is a single transistor which stores charge on a small capacitor. These dynamic memory "cells" are organized into an array of 128 rows by 128 columns. Each of the 128 rows requires refreshing at least every two milliseconds. This refresh may be accomplished on a given row by any read or $\overline{RAS}$-only cycle. A page-mode feature is included which reduces access and/or cycle time when multiple operations are performed within the same row.

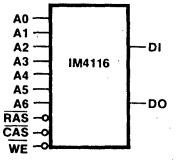
All inputs and outputs are TTL compatible. On-chip address registers and three-state outputs simplify system design and allow for interfacing with common bus structures.

The device is packaged in a standard 16-pin DIP, providing high system bit density and compatibility with automatic testing and insertion equipment.

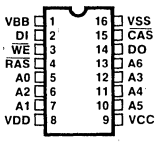
LOGICAL BLOCK DIAGRAM



LOGIC SYMBOL



PIN CONFIGURATION



Top View

ORDERING INFORMATION

ORDER CODE	ACCESS TIME NORMAL	ACCESS TIME PAGE	EQUIPMENT	PACKAGE
IM4116-2CJE	150ns	100ns	MK4116J-2	CERDIP
IM4116-2CDE	150ns	100ns	MK4116P-2	CERAMIC
IM4116-2CPE	150ns	100ns	—	PLASTIC
IM4116-3CJE	200ns	135ns	MK4116J-3	CERDIP
IM4116-3CDE	200ns	135ns	MK4116P-3	CERAMIC
IM4116-3CPE	200ns	135ns	—	PLASTIC
IM4116-4CJE	250ns	165ns	MK4116J-2	CERDIP
IM4116-4CDE	250ns	165ns	MK4116P-2	CERAMIC
IM4116-4CPE	250ns	165ns	—	PLASTIC

PIN NAMES MNEMONIC	PIN NAMES JEDEC	DESCRIPTION
A0-A6	A0-A6	Address Inputs
$\overline{CAS}$	$\overline{CE}$	Column Address Strobe
DI	D	Data In
DO	Q	Data Out
$\overline{RAS}$	$\overline{RE}$	Row Address Strobe
VBB	VBB	Power (−5V)
VCC	VCC	Power (+5V)
VDD	VDD	Power (+12V)
VSS	VSS	Ground
$\overline{WE}$	$\overline{W}$	Write Enable

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
VIN	Voltage on any Pin Relative to VBB	-0.5	+20	V	2, 3
PD	Power Dissipation		1	W	
IOS	Short Circuit Output Current		50	mA	
TSTORE	Storage Temperature	-55	+150	°C	
TA	Ambient Temperature Under Bias	0	+70	°C	

NOTES:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
2. VSS - VBB ≥ 4.5V
3. This device contains internal circuitry to protect against damage due to static charge. Conventional precautions should be observed, however, during storage, handling, and use to avoid exposure to excessive voltages.

OPERATING CONDITIONS[1]

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
VBB	VBB Supply	-4.5	-5.5	V
VCC	VCC Supply	4.5	5.5	V
VDD	VDD Supply	10.8	13.2	V
VSS	VSS Supply	0	0	V
TA	Ambient Temperature Under Bias	0	+70	°C

NOTE: VBB must be applied prior to and removed after other supply voltages.

ELECTRICAL PARAMETERS VDD = +12V ± 10%, VCC = +5V ± 10%, VSS = 0V, VBB = -5V ± 10%, TA = 0° C to +70° C

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
IDD1	Average Operating Supply Currents		35	mA	
ICC1	(RAS, CAS cycling; tRC = tRC (min))				1
IBB1			200	μA	
IDD2	Standby Supply Current		1.5	mA	
ICC2	($\overline{RAS}$ = VIHC)	-10	10	μA	
IBB2			100	μA	
IDD3	Average Refresh Supply Currents		27	mA	
ICC3	($\overline{RAS}$ Cycling, CAS = VIHC; tRC = tRC (Min))	-10	10	μA	
IBB3			200	μA	
IDD4	Average Page Mode Supply Current		27	mA	
ICC4	($\overline{RAS}$ = VIL, CAS cycling; tPC = tPC (min))				1
IBB4			200	μA	
VIH	Input HIGH Voltage (A, DI)	2.4	7.0	V	
VIH1	Input HIGH Voltage ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	2.7	2.7	V	
VIL	Input LOW Voltage	-1.0	+0.8	V	
IIL	Input Leakage Current	-10	+10	μA	
VOH	Output HIGH Voltage	2.4		V	
VOL	Output LOW Voltage		0.4	V	
IOZ	Output Leakage Current	-10	+10	μA	3, 4
CIN	Input Capacitance (A)		5	pF	2
CIN1	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{DI}$, $\overline{WE}$)		10	pF	2
CO	Output Capacitance (DO)		7	pF	2

NOTES: **1.** ICC1 and ICC4 depend upon output loading.
2. These parameters characterized and periodically sampled; not 100% tested.
3. 0V ≤ V_{OUT} ≤ 10V
4. $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}

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TIMING PARAMETERS[1, 2, 3] VDD = +12V ± 10%, VCC = +5V ± 10%, VSS = 0V, VBB = −5V ± 10%, TA = 0°C to +70°C

SYMBOL		DESCRIPTION	MK4116-2		MK4116-3		MK4116-4		UNITS	NOTES
MNEMONIC	JEDEC[8]		MIN	MAX	MIN	MAX	MIN	MAX		
tAR	TRELAX (C)	$\overline{RAS}$ LOW to Column Address Hold Time	95		120		160			
tASC	TAVCEL	Column Address Set-up Time	−10		−10		−10			
tASR	TAVREL	Row Address Set-up Time	0		0		0			
tCAC	TCELQV	Access Time from $\overline{CAS}$		100		135		165		4
tCAH	TCELAX	$\overline{CAS}$ LOW to Column Address Hold Time	45		55		75			
tCAS	TCELCEH	$\overline{CAS}$ Pulse Width	100	10000	135	10000	165	10000		
tCP	TCEHCEL	Page Mode $\overline{CAS}$ Precharge Time	60		80		100			
tCRP	TCEHREL	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20			
tCSH	TRELCEH	$\overline{RAS}$ LOW to $\overline{CAS}$ HIGH Delay	150		200		250			
tCWD	TCELWL	$\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay	70		95		125			5
tCWL	TWLCEH	$\overline{WE}$ LOW to $\overline{CAS}$ HIGH Set-up Time	60		80		100			
tDH	TCELDX or TWLDX	$\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time	45		55		75		nS	6
tDHR	TRELDX	$\overline{RAS}$ LOW to Data In Valid Hold Time	95		120		160			
tDS	TDVCEL or TDVWL	Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Set-up Time	0		0		0			6
tOFF	TCEHQZ	$\overline{CAS}$ HIGH to Output OFF Delay	0	40	0	50	0	60		
tPC	TCELCEL (P)	Page Mode Cycle Time	170		225		275			
tRAC	TRELQV	Access Time from $\overline{RAS}$		150		200		250		4
tRAH	TRELAX (R)	$\overline{RAS}$ LOW to Row Address Hold Time	20		25		35			
tRAS	TRELREH	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000		
tRC	TRELREL	Random Read or Write Cycle Time	375		375		410			
tRCD	TRELCEL	$\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay	20	50	25	65	35	85		7
tRCH	TCEHWX	Read Hold Time	0		0		0			
tRCS	TWHCEL	Read Set-up Time	0		0		0			
tREF		Refresh Interval		2		2		2	mS	
tRMW	TRELREL (RMW)	Read-Modify-Write Cycle Time								
tRP	TREHREL	$\overline{RAS}$ Precharge Time	100		120		150			
tRSH	TCELREH	$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay	100		135		165			
tRWC	TRELREL (R/W)	Read/Write Cycle Time	375		375		515			
tRWD	TRELWL	$\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay	120		160		200		nS	
tRWL	TWLREH	$\overline{WE}$ LOW to $\overline{RAS}$ HIGH Set-up Time	60		80		100			
tT		Transition Time	3	35	3	50	3	50		3
tWCH	TCELWH	Write Hold Time	45		55		75			
tWCR	TRELWH	$\overline{RAS}$ LOW to Write Hold Time	95		120		160			
tWCS	TWLCEL	$\overline{WE}$ LOW to $\overline{CAS}$ LOW Set-up Time	−20		−20		−20			5
tWP	TWLWH	Write Pulse Width	45		55		75			

NOTES:
1. Several cycles are required after power-up before proper device operation is achieved. Any eight cycles which perform refresh are adequate for this purpose.
2. Unless otherwise noted, tRISE = tFALL = 5nS
3. VIHC (min), VIH (min) and VIL (max) are reference levels for timing measurements.
4. Loading equivalent to two TTL inputs +100 pF
5. tWCS, tCWD, and tRWD are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only: for tWCS ≥ TWCS (min), the cycle is an early-write cycle and the data output will remain high-impedance throughout the entire cycle; for tCWD > tCWD (min) and tRWD ≥ tRWD (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.
6. For positive tWCS these parameters are referenced to CAS. For negative tWCS, or read-write cycles these parameters are referenced to $\overline{WE}$.
7. For tRCD ≥ tRCD (max), access time is controlled by tCAC.

FUNCTIONAL DESCRIPTION

Addressing

Fourteen address bits are required to select one of the 4116's 16,384 possible bit locations. These 14 address bits are latched on-chip in two groups of seven bits. The Row Address Strobe ($\overline{RAS}$) latches the 7-bit row address on its falling edge; similarly, the 7-bit column address is latched by $\overline{CAS}$.

The normal sequence of events is as follows: First, the 7-bit row address is applied to the address inputs. At the end of the row address setup time (tASR), $\overline{RAS}$ is brought LOW. After the row address hold time (tRAH) has elapsed, the 7-bit column address is applied and $\overline{CAS}$ is brought LOW.

The column address information is not used internally until tRCD (max) after $\overline{RAS}$-falls. Further, $\overline{CAS}$, is gated with the $\overline{RAS}$ clock generator such that it may occur at any time from tRCD (min) to tRCD (max), without effecting access time. If $\overline{CAS}$ occurs after tRCD (max) the access time will be lengthened by the delay from tRCD (max) to $\overline{CAS}$.

Page Mode Operation

Successive memory cycles accessing the same row in the memory array require the row address and $\overline{RAS}$ to be supplied only once. Further accesses to the same row require only column addresses and $\overline{CAS}$, with $\overline{RAS}$ held LOW.

In addition to savings in access and cycle time, page mode operation results in reduced power consumption since dynamic power due to $\overline{RAS}$ transitions is drawn only once per row address.

Data Input

Data to be written is strobed into the on-chip data latch by a combination of $\overline{CAS}$ and $\overline{WE}$ while $\overline{RAS}$ is active. Whichever of $\overline{CAS}$ and $\overline{WE}$ makes the later negative-going transition serves as the data strobe. Several different write cycles are made possible by this flexibility.

An "early-write" cycle takes place if $\overline{WE}$ goes LOW before $\overline{CAS}$. In the case where data-in (DI) is not valid when $\overline{CAS}$ goes LOW, $\overline{WE}$ must be delayed until after $\overline{CAS}$ falls. In this "delayed-write" cycle, data setup and hold times are referenced to the negative-going edge of $\overline{WE}$, rather than $\overline{CAS}$.

Data Output

The data output (DO) unconditionally assumes the high-impedance state wherever $\overline{CAS}$ is HIGH. For read, read-modify-write, or delayed-write cycles, DO remains high-impedance until access time, at which time it will reflect the logic state of the addressed cell. DO remains high-impedance in an early-write cycle, or in cycles where $\overline{RAS}$ and $\overline{CAS}$ are not both received. Thus, in systems which utilize early-write cycles exclusively, DI, and DO may be connected together with no conflict.

Input/Output Levels

All inputs, including $\overline{RAS}$ and $\overline{CAS}$, are low-capacitance high-impedance, and TTL-level compatible. Special clock drivers are not required, simplifying input driver design.

In order to prevent ringing, signal termination resistors are usually necessary. In general, transmission line techniques must be utilized on signal lines to achieve maximum system speeds.

Refresh

Any cycle in which $\overline{RAS}$ occurs serves to refresh the selected row. However, it is generally more convenient (and requires substantially less power) to perform the refresh operation using the $\overline{RAS}$-only cycle. Each of the 128 rows must be refreshed at least once per two milliseconds.

Power Sequencing

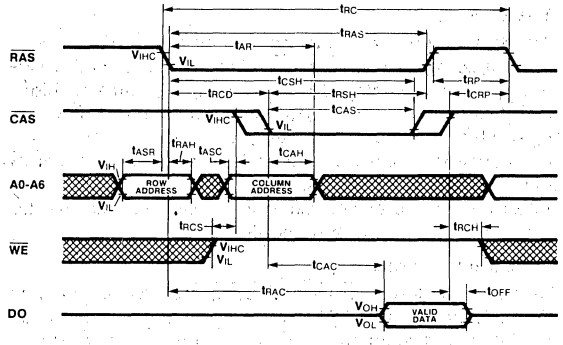
VBB should be applied before and removed after other supply voltages. Under system failure conditions in which one or more supplies exceed the specified limit, significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state.

After power is applied, the MK4116 requires several cycles before proper device operation is achieved. Any eight cycles which perform refresh are adequate for this purpose.

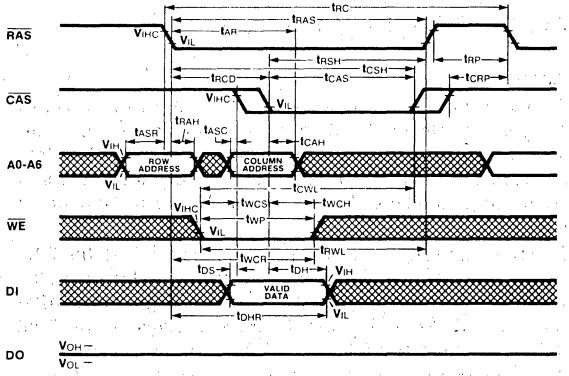
Power Dissipation

Because of the extensive use of dynamic circuitry in the MK4116, most of the dissipated power is as a result of a transition on $\overline{RAS}$ or $\overline{CAS}$. Thus, the dynamic power is primarily a function of operating frequency. Worst case power dissipation is 462 MW at 375nS cycle time.

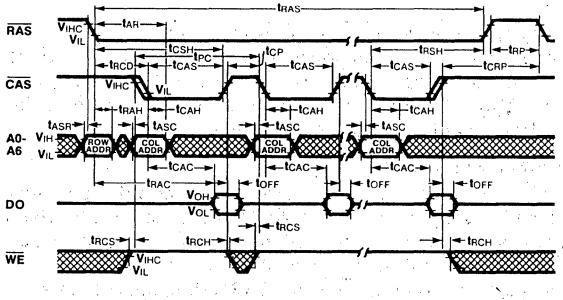
VCC is utilized only to power the output buffer, and is not connected elsewhere; ICC, is thus a function only of output loading. VCC may be left unconnected for battery-backup operation.



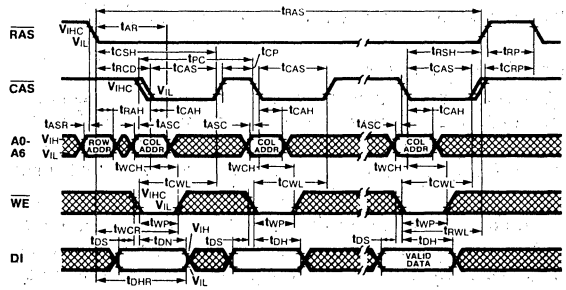
READ CYCLE



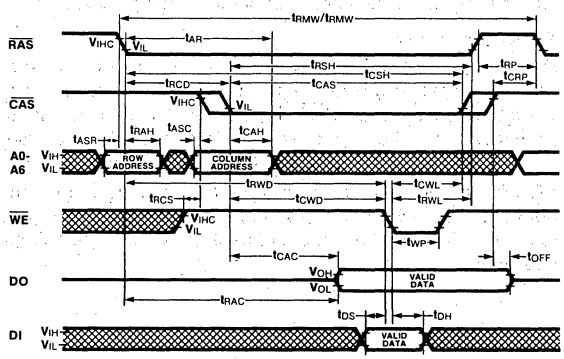
EARLY WRITE CYCLE



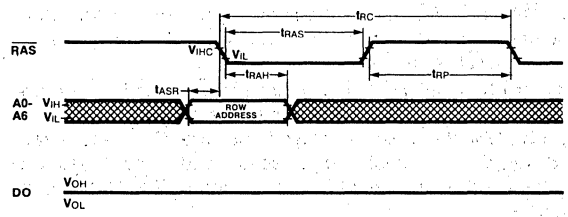
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



READ-WRITE/READ MODIFY-WRITE CYCLE



RAS-only REFRESH CYCLE

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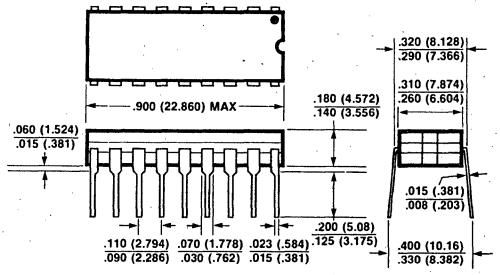
PACKAGE DIMENSIONS

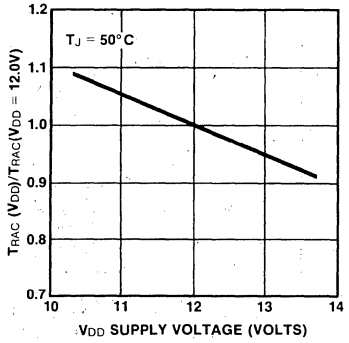
18-pin CERDIP (J)*



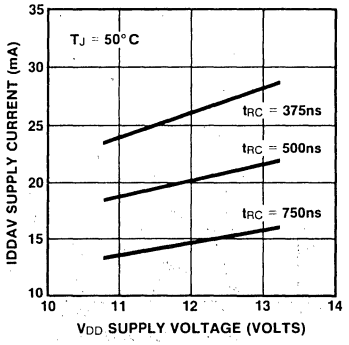
*Hermetic: Maximum leakage rate 5 x 10^{-7} atm. cc/sec.

TYPICAL CHARACTERISTICS

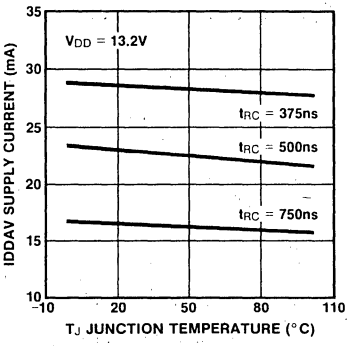
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}



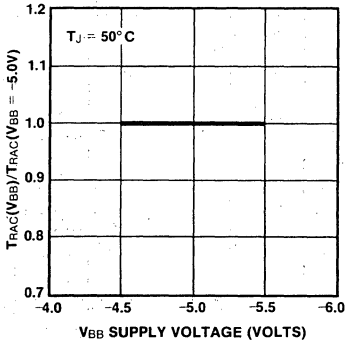
TYPICAL IDDAV vs. V_{DD}



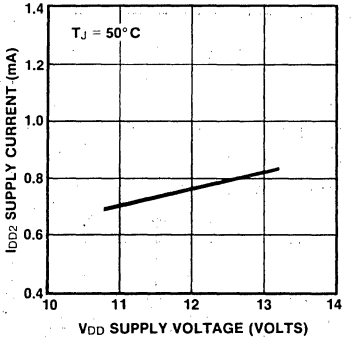
TYPICAL IDDAV vs. JUNCTION TEMPERATURE



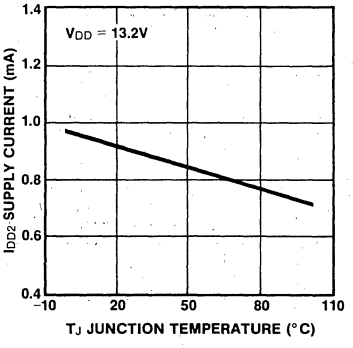
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}



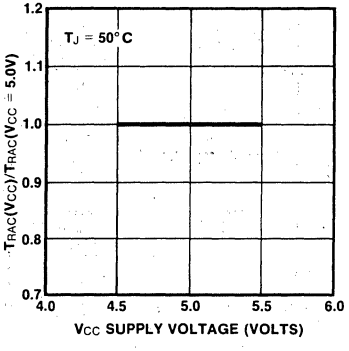
TYPICAL IDDSB vs. V_{DD}



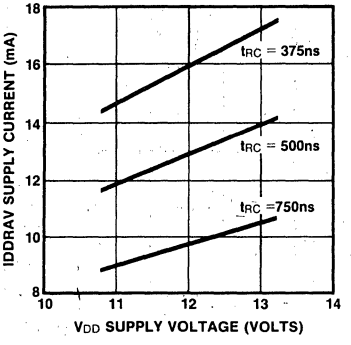
TYPICAL IDDSB vs. JUNCTION TEMPERATURE



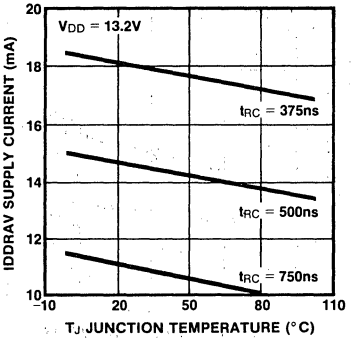
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}



TYPICAL IDDRAV vs. V_{DD}



TYPICAL IDDRAV vs. JUNCTION TEMPERATURE



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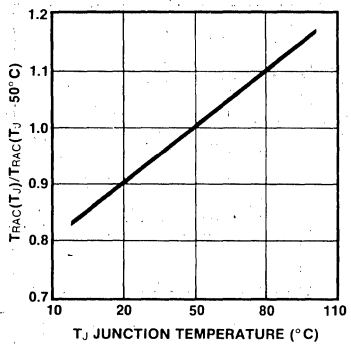
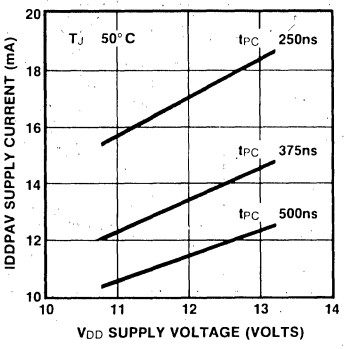
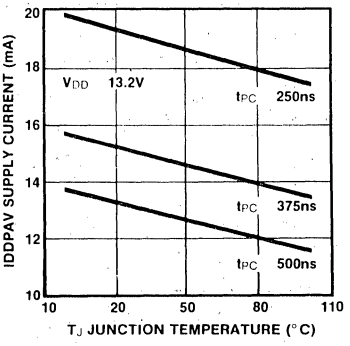
TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE



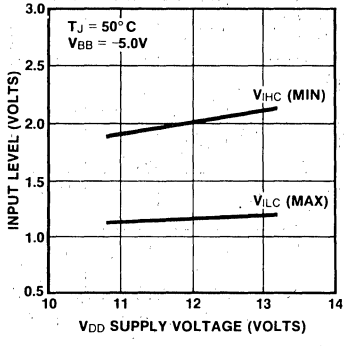
TYPICAL IDDPAV vs. V_{DD}



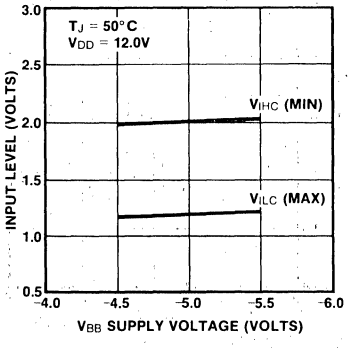
TYPICAL IDDPAV vs. JUNCTION TEMPERATURE



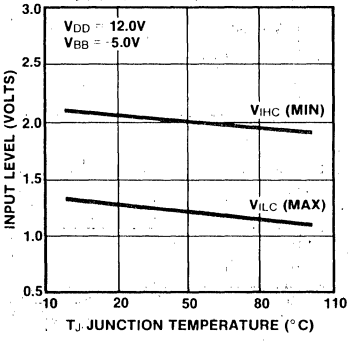
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



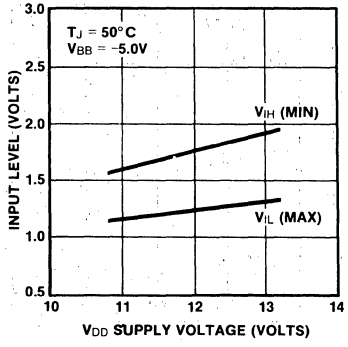
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



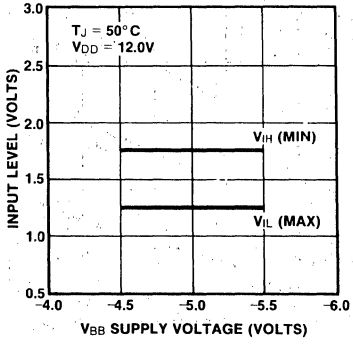
TYPICAL CLOCK INPUT LEVELS vs. T_J



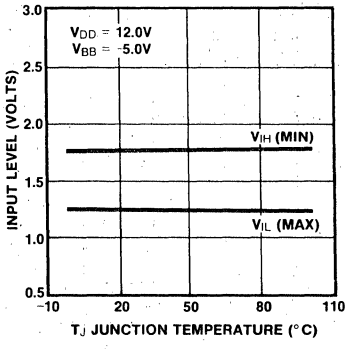
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J



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SYMBOLS AND ABBREVIATIONS

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates HIGH (H), LOW (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

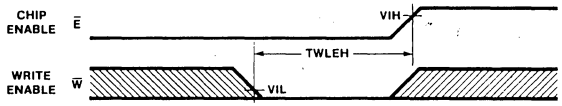
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S Chip Select
G Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows write-pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

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