FUJITSU
MICROELECTRONICS

MB8116E
MB8116H

MOS 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MB8116 is a fully decoded dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB8116 to be housed in a standard 16-pin DIP. Pin-outs conform to the accepted industry standard.

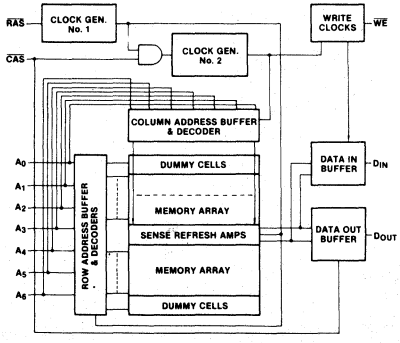
The MB8116 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

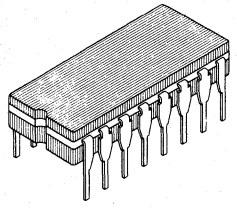
Clock timing requirements are non-critical, and power supply tolerances are 10%. All inputs are TTL compatible; the output is three-state TTL.

FEATURES

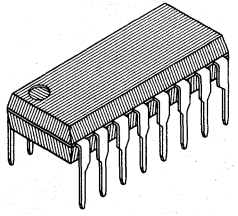
- **16,384 x 1 RAM, 16 pin package**
- **Silicon-gate, double-poly NMOS, single transistor cell**
- **Row access time:**
  200 ns max. (MB8116E)
  150 ns max. (MB8116H)
- **Cycle time:**
  375 ns min.
- **Low power**
  462mW active,
  20 mW standby (max.)
- **±10% tolerance on +12V, ±5V supplies**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **"Gated" $\overline{CAS}$**
- **128 refresh cycles**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-in**
- **Compatible with MK4116**

MB8116 BLOCK DIAGRAM



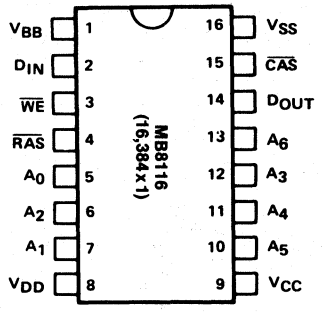


CERDIP PACKAGE
DIP-16C-C03



PLASTIC PACKAGE
DIP-16P-M01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating		Symbol	Value	Unit
Voltage of any pin relative to V_{BB}		V_{IN}, V_{OUT}	−0.5 to +20	V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}		V_{DD}, V_{CC}	−0.5 to +15	V
V_{BB}-V_{SS} (V_{DD}-V_{SS} > 0V)		—	0	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−40 to +125	
Power Dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	NOTES	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	1	V_{DD}	10.8	12.0	13.2	V	0°C to +70°C
	1 2	V_{CC}	4.5	5.0	5.5	V	
	1	V_{SS}	0	0	0	V	
	1	V_{BB}	−4.5	−5.0	−5.5	V	
Input High Voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IHC}	2.7	—	6.5	V	
Input High Voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V_{IL}	−1.0	—	0.8	V	

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	Min	Max	Units
OPERATING CURRENT Average power supply current $\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)		I_{DD1} I_{BB1}	—	35 300	mA μA
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IHC})		I_{DD2} I_{BB2}	—	1.5 100	mA μA
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = min)		I_{DD3} I_{BB3}	— —	25 300	mA μA
PAGE MODE CURRENT Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225ns)		I_{DD4} I_{BB4}	— —	27 300	mA μA
V_{CC} POWER SUPPLY CURRENT (Data out is disabled)	3	I_{CC}	−10	10	μA
INPUT LEAKAGE CURRENT Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ 7V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = −5mA) Output low voltage (I_{OL} = 4.2mA)		 V_{OH} V_{OL}	 2.4 	 0.4	 V V

Notes: 1. All voltages are reference to V_{SS}.

2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in the standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH}(min) specification is not guaranteed in this mode.
3. When Data out is enabled, V_{CC} power supply current depends upon output loading; V_{CC} is connected to the output buffer only.

CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_6$, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	10	pF
Output Capacitance D_{OUT}	C_{OUT}	—	7	pF

DYNAMIC CHARACTERISTICS [NOTES 4, 5, 6]

(Recommended Operating Conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB8116E		MB8116H		Units
			Min	Max	Min	Max	
Time between Refresh		t_{REF}	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	375	—	375	—	ns
Read-Write Cycle Time		t_{RWC}	375	—	375	—	ns
Page Mode Cycle Time		t_{PC}	225	—	170	—	ns
Access Time from $\overline{RAS}$	[7] [9]	t_{RAC}	—	200	—	150	ns
Access Time from $\overline{CAS}$	[8] [9]	t_{CAC}	—	135	—	100	ns
Output Buffer Turn Off Delay		t_{OFF}	0	50	0	50	ns
Transition Time		t_T	3	50	3	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	32000	150	32000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135	—	100	—	ns
$\overline{CAS}$ Precharge Time		t_{CP}	80	—	60	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	10000	100	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	200	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	[10]	t_{RCD}	30	65	25	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	−20	—	−20	—	ns
Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	25	—	20	—	ns
Column Address Set Up Time		t_{ASC}	−5	—	−5	—	ns
Column Address Hold Time		t_{CAH}	55	—	45	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120	—	95	—	ns
Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
Read Command Hold Time		t_{RCH}	10	—	10	—	ns
Write Command Set Up Time	[11]	t_{WCS}	−10	—	−10	—	ns
Write Command Hold Time		t_{WCH}	55	—	45	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	120	—	95	—	ns
Write Command Pulse Width		t_{WP}	55	—	45	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80	—	60	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80	—	60	—	ns
Data In Set Up Time		t_{DS}	0	—	0	—	ns
Data In Hold Time		t_{DH}	55	—	45	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120	—	95	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	[11]	t_{CWD}	95	—	70	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	[11]	t_{RWD}	160	—	120	—	ns

Notes: 4. Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

5. Dynamic measurements assume t_T = 5ns.

6. V_{IHC}(min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

7. Assumes that $t_{RCD} \leq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

8. Assumes that $t_{RCD} \geq t_{RCD}$(max).

9. Measured with a load equivalent to 2 TTL loads and 100pF.

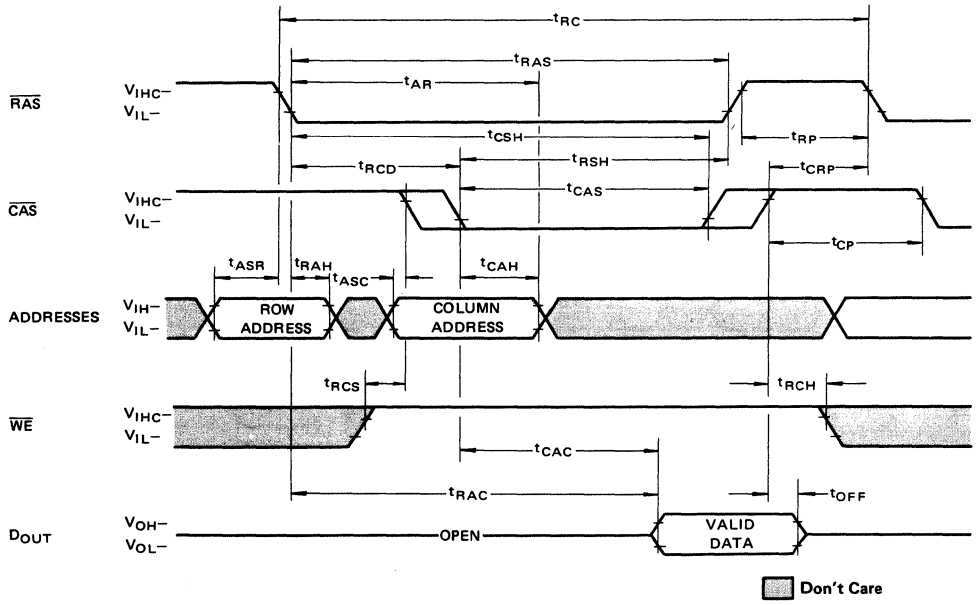
10. Operation within the t_{RCD}(max) limit insures that t_{RCD}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

11. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.

    If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

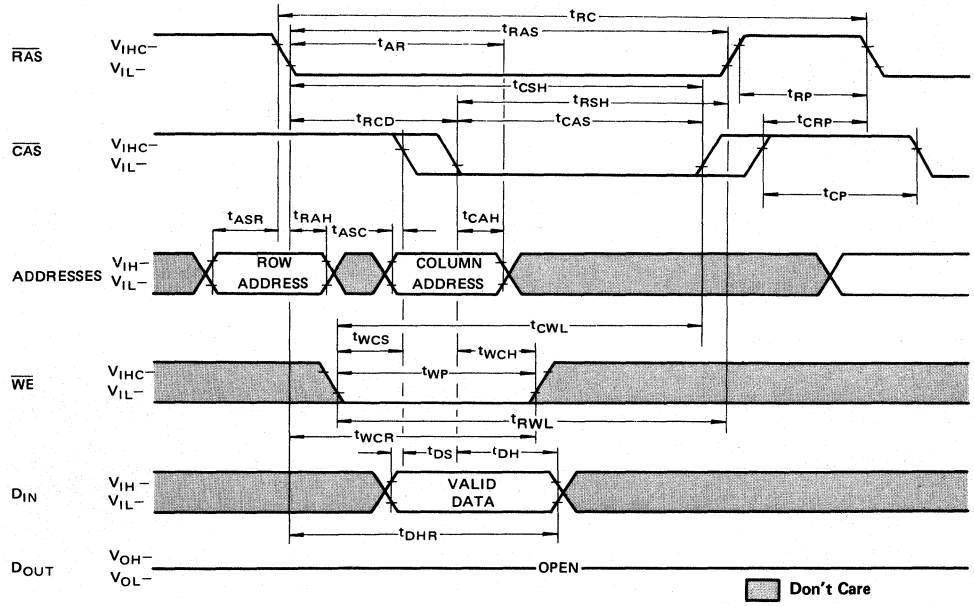
TIMING DIAGRAMS

READ CYCLE

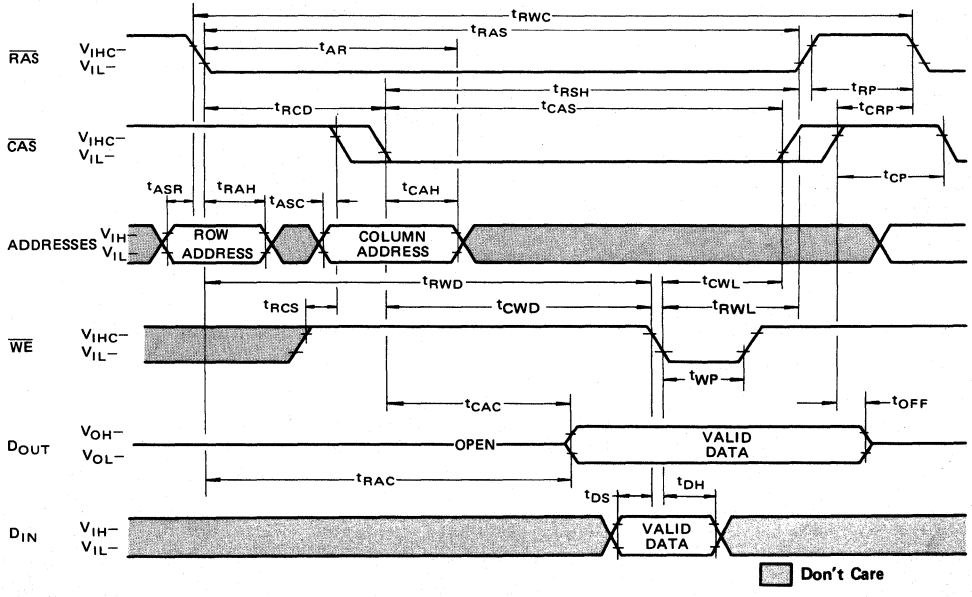


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



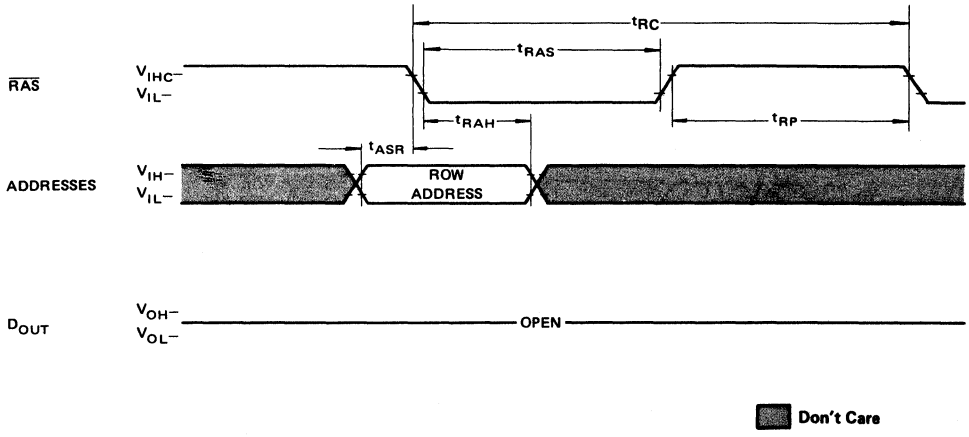
READ-WRITE/READ-MODIFY-WRITE CYCLE



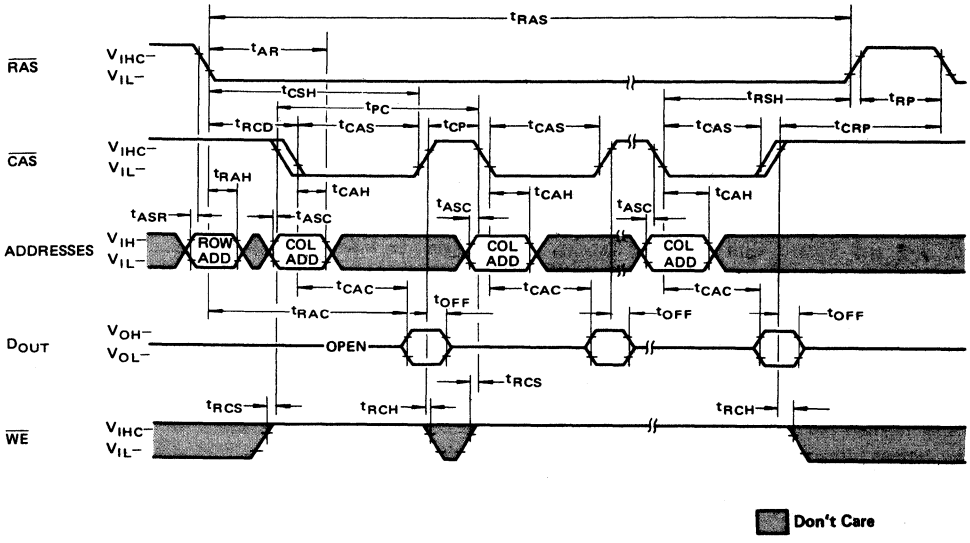
TIMING DIAGRAMS (Continued)

"$\overline{RAS}$-ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = Don't Care

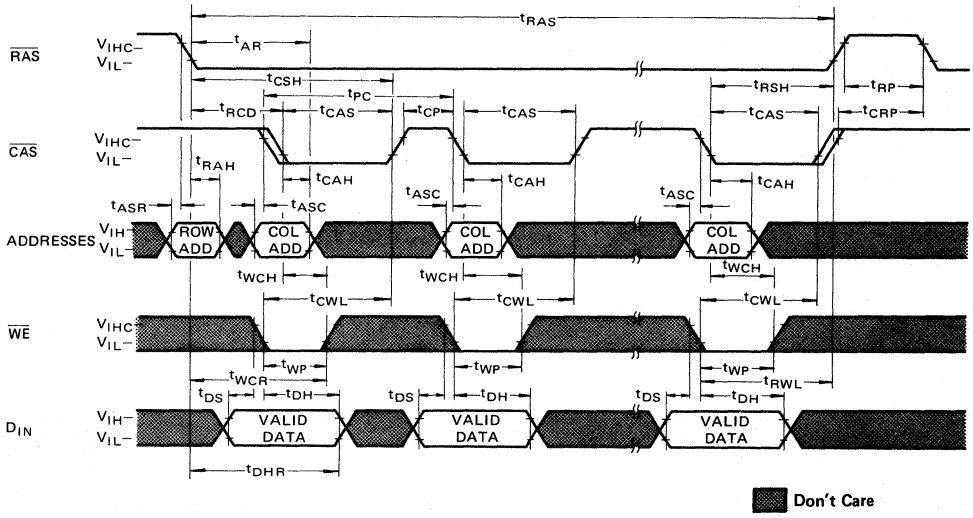


PAGE-MODE READ CYCLE



TIMING DIAGRAMS (Continued)

PAGE-MODE WRITE CYCLE



DESCRIPTION

Address Inputs:

A total of fourteen binary input address bits are required to decode any one of 16,384 storage cell locations within the MB8116. Seven row-address bits are established on the input pins (A_0 through A_6) and latched with the Row Address Strobe ($\overline{RAS}$). The seven column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected. $\overline{WE}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input:

Data is written into the MB8116 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode:

Page-mode operation permits strobing the row-address into the MB8116 while maintaining RAS at a logic low (0) throughout all successive memory operations in which the row address doesn't change. Thus the power dissipated by the negative going edge of RAS is saved. Futher, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-address at least every two milli-seconds. Any operation in which $\overline{RAS}$ transits accomplishes refresh. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substanial reduction in power dissipation.

Power Considerations:

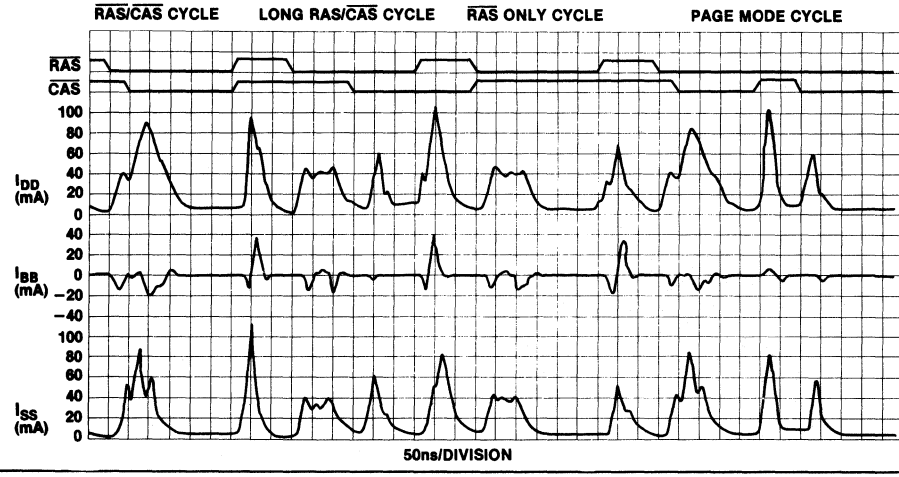
The output buffer of the MB8116 can be powered via V_{CC} from the supply voltage (normally 5 volts) to which the memory is interfaced. In standby operation, V_{CC} may be removed without affecting refresh. Thus standby power is conserved because all the power supplies for the peripheral circuitry with the exception of $\overline{RAS}$ timing and refresh address is turned off. Most of the MB8116 circuitry, including sense amplifiers, is dynamic, and most of the power drain comes from an address strobe ($\overline{RAS}$ or $\overline{CAS}$) edge. Thus, dynamic power dissipation depends mostly on operating frequency.

Power Up:

No particular supply sequencing is required for the MB8116. However, absolute maximum ratings must be adhered to. Thus, V_{BB} should be turned on first and turned off last, and V_{DD} is turned on. After power is applied, several cycles are required before proper operation is assured. About eight refresh cycles should be sufficient to accomplish this.

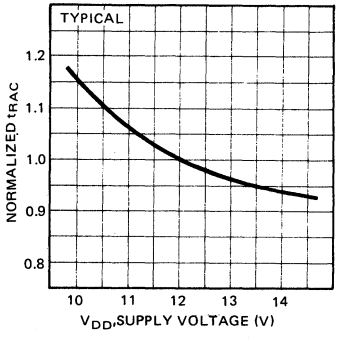
Current Waveforms

NOTE: V_{DD} = 13.2V, V_{BB} = −4.5V, T_A = 25°C

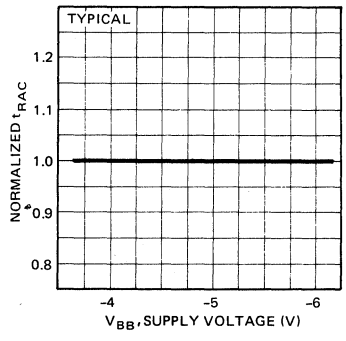


TYPICAL CHARACTERISTICS CURVES

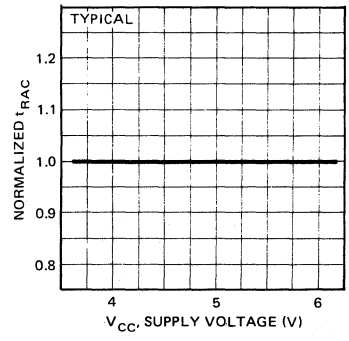
NORMALIZED ACCESS TIME vs V_{DD} SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs V_{BB} SUPPLY VOLTAGE

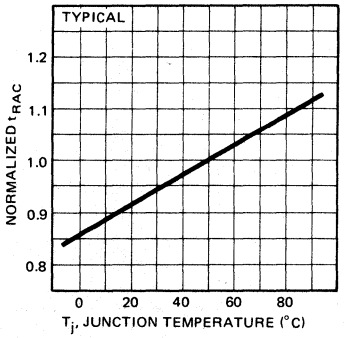


NORMALIZED ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

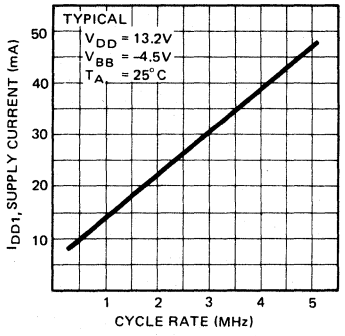


TYPICAL CHARACTERISTICS CURVES (Continued)

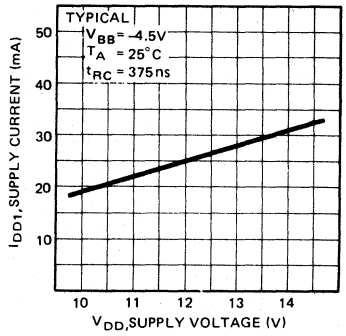
NORMALIZED ACCESS TIME vs T_j JUNCTION TEMPERATURE



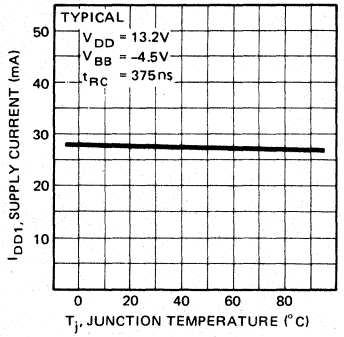
I_{DD1} (AVERAGE) vs CYCLE RATE



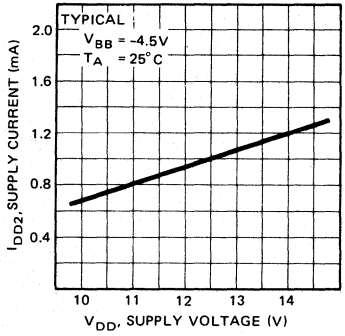
I_{DD1} (AVERAGE) vs V_{DD} SUPPLY VOLTAGE



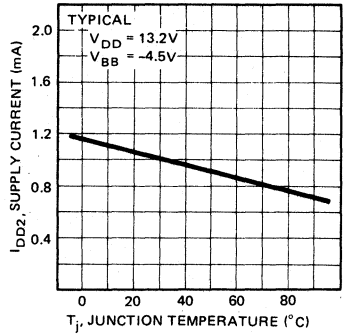
I_{DD1} (AVERAGE) vs T_j JUNCTION TEMPERATURE



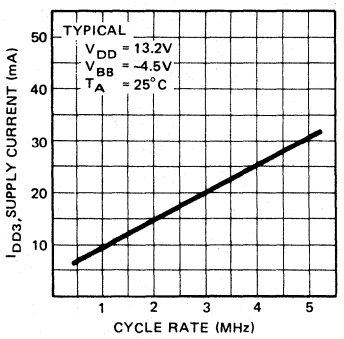
I_{DD2} (STANDBY) vs V_{DD} SUPPLY VOLTAGE



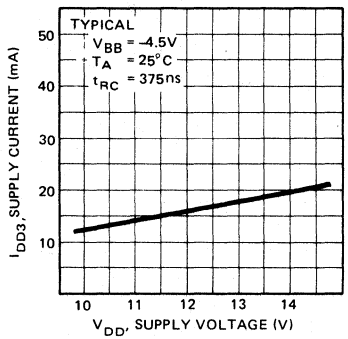
I_{DD2} (STANDBY) vs T_j JUNCTION TEMPERATURE



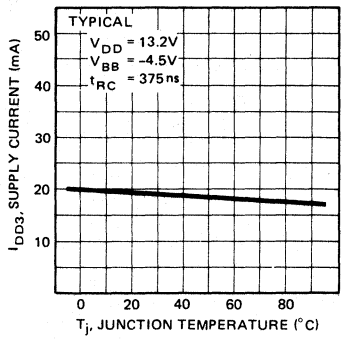
I_{DD3} ($\overline{RAS}$–ONLY) vs CYCLE RATE



I_{DD3} ($\overline{RAS}$–ONLY) vs V_{DD} SUPPLY VOLTAGE

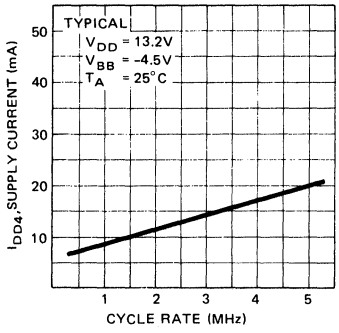


I_{DD3} ($\overline{RAS}$–ONLY) vs T_j JUNCTION TEMPERATURE

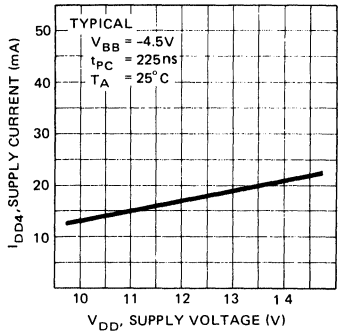


TYPICAL CHARACTERISTICS CURVES (Continued)

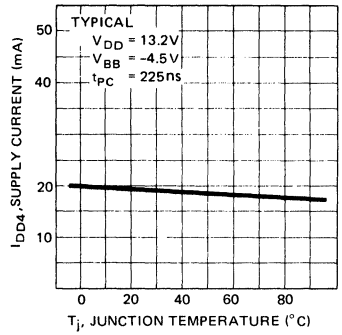
I_{DD4} (PAGE–MODE) vs CYCLE RATE



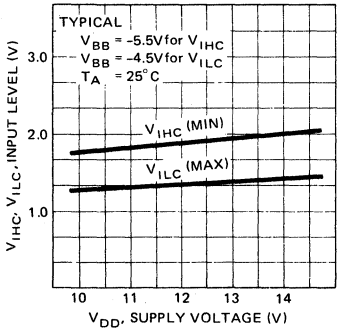
I_{DD4} (PAGE–MODE) vs V_{DD} SUPPLY VOLTAGE



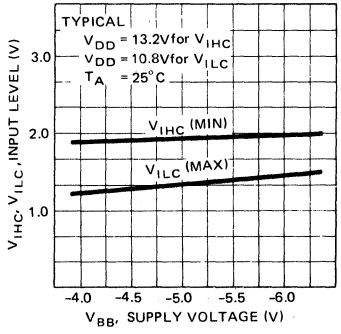
I_{DD4} (PAGE–MODE) vs T_j JUNCTION TEMPERATURE



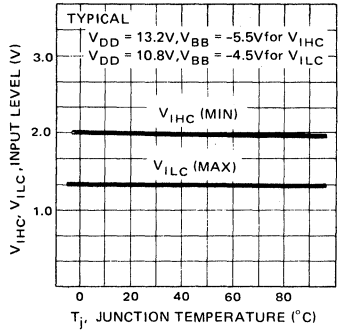
V_{IHC}, V_{ILC} INPUT LEVELS vs V_{DD} SUPPLY VOLTAGE



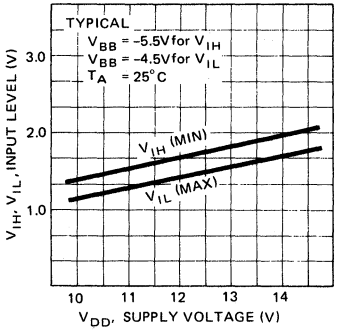
V_{IHC}, V_{ILC} INPUT LEVELS vs V_{BB} SUPPLY VOLTAGE



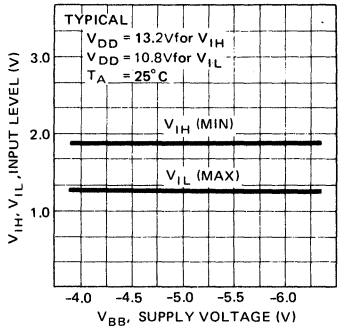
V_{IHC}, V_{ILC} INPUT LEVELS vs T_j JUNCTION TEMPERATURE



V_{IH}, V_{IL} INPUT LEVLES vs V_{DD} SUPPLY VOLTAGE



V_{IH}, V_{IL} INPUT LEVELS vs V_{BB} SUPPLY VOLTAGE



V_{IH}, V_{IL} INPUT LEVELS vs T_j JUNCTION TEMPERATURE