PRELIMINARY

16,384 x 1-BIT DYNAMIC RAM MK4116-53 (N)

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- 200 ns access time, 375 ns cycle
- Low power: 462 mW active, 20 mW standby (max)
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh and Page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles

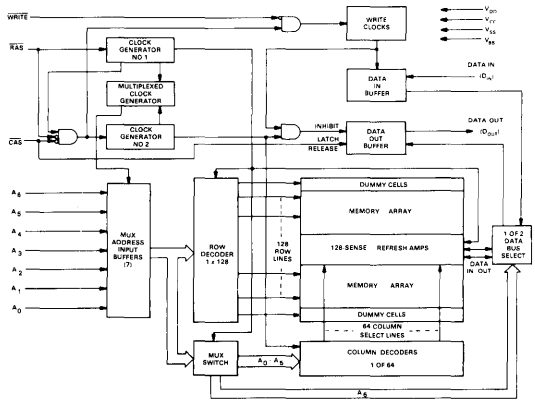
DESCRIPTION

The MK4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in Mostek's high performance MK4027 (4K RAM).

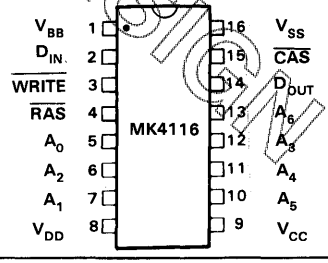
The technology used to fabricate the MK4116 is Mostek's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MK4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_6	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe	V_{BB}	Power (–5 V)
D_{IN}	Data In	V_{CC}	Power (+5 V)
D_{OUT}	Data Out	V_{DD}	Power (+12 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... -0.5 V to +20 V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... -1.0 V to +15.0 V
V_{BB} - V_{SS} (V_{DD} - V_{SS} > 0 V) ..... 0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +55°C
Storage Temperature (Ambient) (Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient) (Plastic) ..... -55°C to +125°C
Short Circuit Output Circuit ..... 50 mA
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 55°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD} V_{CC} V_{SS} V_{BB}	Supply Voltage	10.8 4.5 0 -4.5	12.0 5.0 0 -5.0	13.2 5.5 0 -5.7	V V V V	1 1,2 1 1
V_{IHC}	Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	—	7.0	V	1
V_{IH}	Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2	—	7.0	V	1
V_{IL}	Input Low (Logic 0) Voltage, all inputs	-1.0	—	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 55°C) (V_{DD} = 12.0 V ± 10%; V_{CC} = 5.0 V ± 10%; V_{BB} = -5.0 V ± 10%; V_{SS} = 0 V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1} I_{CC1} I_{BB1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns)		35 200	mA μA	3 4
I_{DD2} I_{CC2} I_{BB2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	 -10	1.5 10 100	mA μA μA	
I_{DD3} I_{CC3} I_{BB3}	REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, CAS = V_{IHC}; t_{RC} = 375 ns	 -10	27 10 200	mA μA μA	3
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input (V_{BB} = -5 V, 0 V ≤ V_{IN} ≤ +7.0 V, all other pins not under test = 0 volts)	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0 V ≤ V_{OUT} ≤ +5.5 V)	-10	10	μA	
V_{OH} V_{OL}	OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = -5 mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	 2.4	 0.4	 V V	 3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [5,6,7]
($0°C \leq T_A \leq 55°C$) (V_{DD} = 12.0 V ± 10%; V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, V_B = -5.0 V ± 10%)

SYM	PARAMETER	MK4116-53**		UNITS	NOTES
		MIN	MAX		
t_{RC}	Random read or write cycle time	375		ns	17
t_{RWC}	Read-write cycle time	375		ns	17
t_{RMW}	Read Modify Write	405		ns	
t_{RAC}	Access time from $\overline{RAS}$		200	ns	8,10
t_{CAC}	Access time from $\overline{CAS}$		135	ns	9,10
t_{OFF}	Output buffer turn-off delay	0	50	ns	11
t_T	Transition time (rise and fall)	3	50	ns	7
t_{RP}	$\overline{RAS}$ precharge time	120		ns	
t_{RAS}	$\overline{RAS}$ pulse width	200	10000	ns	
t_{RSH}	$\overline{RAS}$ hold time	135		ns	
t_{CAS}	$\overline{CAS}$ pulse width	135	10000	ns	
t_{CSH}	$\overline{CAS}$ hold time	200		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	65	ns	12
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	-20		ns	
t_{ASR}	Row Address set-up time	0		ns	
t_{RAH}	Row Address hold time	25		ns	
t_{ASC}	Column Address set-up time	-10		ns	
t_{CAH}	Column Address hold time	55		ns	
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	120		ns	
t_{RCS}	Read command set-up time	0		ns	
t_{RCH}	Read command hold time	0		ns	
t_{WCH}	Write command hold time	55		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	120		ns	
t_{WP}	Write command pulse width	55		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	70		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	70		ns	
t_{DS}	Date-in set-up time	0		ns	13
t_{DH}	Date-in hold time	55		ns	13

**This device can be operated at an ambient temperature of 70°C if the refresh interval is changed to 128 refresh cycles every 1.1 ms.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (5,6,7)

(0°C ≤ T_A ≤ 55°C) (V_{DD} = 12.0 V ± 10%; V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, V_{BB} = -5.0 V ± 10%)

SYM	PARAMETER	MK4116-53**		UNITS	NOTES
		MIN	MAX		
t_{DHR}	Date-in hold time referenced to $\overline{RAS}$	120		ns	
t_{REF}	Refresh Period		2	ms	
t_{WCS}	$\overline{WRITE}$ command set-up time	-20		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	80		ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	145		ns	14

NOTES:

1. All voltages referenced to V_{SS}.
2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} min specification is not guaranteed in this mode.
3. I_{DD1} and I_{DD3} depend on cycle rate. The maximum specified current values are for t_{RC} = 375 ns. I_{DD} limit at other cycle rates are determined by the following equations:
   I_{DD1} (max) [MA] = 10 + 10.25 x cycle rate [MHz]
   I_{DD3} (max) [MA] = 10 + 7 x cycle rate [MHz]
4. I_{CC1} depends upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 typ) to data out. At all other times I_{CC} consists of leakage currents only.
5. Eight cycles are required after power-up or prolonged periods (greater than 2 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
6. AC measurements assume t_T = 5 ns.
7. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
14. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
15. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV=3 volts and power supplies at nominal levels.
16. CAS = V_{IHC} to disable D_{OUT}.
17. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 55°C) is assured.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 55°C) (V_{DD} = 12.0 V ± 10%, V_{SS} = 0V; V_{BB} = -5.0 V ± 10%)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_6), D_{IN}	4	5	pF	15
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	15
C_O	Output Capacitance (D_{OUT})	5	7	pF	15,16

DESCRIPTION (Continued)

System oriented features include direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The MK4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK4116 is capable of delayed write cycles, and $\overline{RAS}$-only refresh. Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, and two dimensional chip selection.