FUJITSU
MICROELECTRONICS

MB8264-15
MB8264-20

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

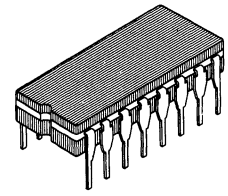
DESCRIPTION

The Fujitsu MB8264 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB8264 to be housed in a standard 16-pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MB8264 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is ±10%. All inputs/outputs are TTL compatible.

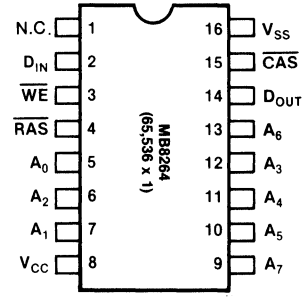


CERDIP PACKAGE
DIP-16C-C04

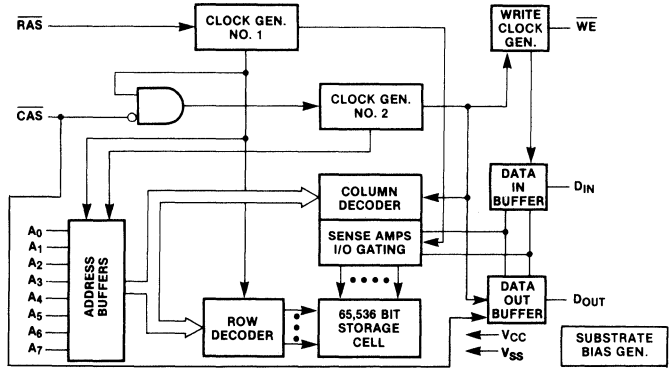
FEATURES

- **65,536 x 1 RAM, 16-pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Row access time:**
  150ns Max (MB8264-15)
  200ns Max (MB8264-20)
- **Cycle time:**
  270ns Min (MB8264-15)
  330ns Min (MB8264-20)
- **Low power:**
  22 mW Max Standby
  275 mW Max Active (MB8264-15)
  248 mW Max Active (MB8264-20)
- **±10% tolerance on +5V Supply**
- **On-chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **"Gated" $\overline{CAS}$**
- **128 refresh cycles**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-in**
- **Hidden Refresh Capability**
- **Pin compatible with HM4864, MK4164, TMS4164, MCM6665, μPD4164 and IMS2600**

PIN ASSIGNMENT



MB8264 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A_0 ~ A_7, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT*	MB8264-20	I_{CC1}		45	mA
Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB8264-15		—	50	mA
STANDBY CURRENT		I_{CC2}			
Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})			—	4	mA
REFRESH CURRENT*	MB8264-20	I_{CC3}		36	mA
Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min)	MB8264-15		—	42	mA
PAGE MODE CURRENT *					
Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)		I_{CC4}	—	34	mA
INPUT LEAKAGE CURRENT					
Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V)		I_{IL}	−10	10	μA
Input pins not under test = 0V, V_{CC} = 5.5V, V_{SS} = 0V					
OUTPUT LEAKAGE CURRENT					
(Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
OUTPUT LEVEL					
Output low voltage (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V
OUTPUT LEVEL					
Output high voltage (I_{OH} = −5mA)		V_{OH}	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS Notes [1,2,3]

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8264-20			MB8264-15			Unit
			Min	Typ	Max	Min	Typ	Max	
Time between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	330	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	375	—	—	300	—	—	ns
Page Mode Cycle Time		t_{PC}	225	—	—	170	—	—	ns
Access Time from $\overline{RAS}$	[4] [6]	t_{RAC}	—	—	200	—	—	150	ns
Access Time from $\overline{CAS}$	[5] [6]	t_{CAC}	—	—	135	—	—	100	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	50	0	—	40	ns
Transition Time		t_T	3	—	50	3	—	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120	—	—	100	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	—	10000	150	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135	—	—	100	—	—	ns
$\overline{CAS}$ Precharge Time (Page Mode Only)		t_{CP}	80	—	—	60	—	—	ns
$\overline{CAS}$ Precharge Time (All Cycles Except Page Mode)		t_{CPN}	30	—	—	25	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	—	10000	100	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	200	—	—	150	—	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	[7] [8]	t_{RCD}	30	—	65	25	—	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	20	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	55	—	—	45	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120	—	—	95	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time	[10]	t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	[9]	t_{WCS}	−10	—	—	−10	—	—	ns
Write Command Hold Time		t_{WCH}	55	—	—	45	—	—	ns
Write Command Hold Time Reference to $\overline{RAS}$		t_{WCR}	120	—	—	95	—	—	ns
Write Command Pulse Width		t_{WP}	55	—	—	45	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80	—	—	60	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80	—	—	60	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	55	—	—	45	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120	—	—	95	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	[9]	t_{CWD}	95	—	—	70	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	[9]	t_{RWD}	160	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	[10]	t_{RRH}	25	—	—	20	—	—	ns

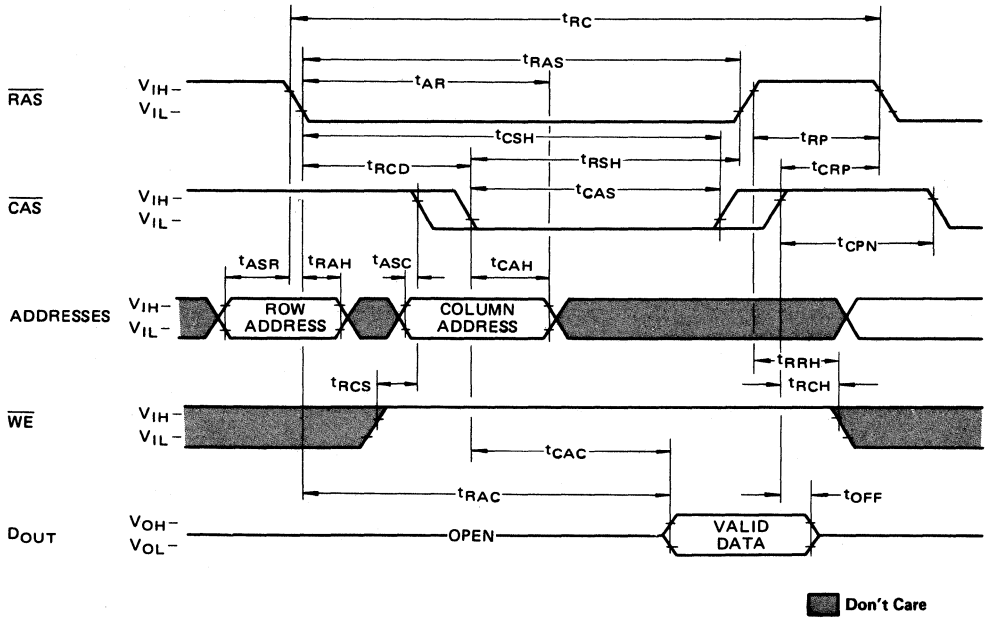
Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. $t_{RCD}(min) = t_{RAH}(min) + 2t_T (t_T = 5ns) + t_{ASC}(min)$.
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.

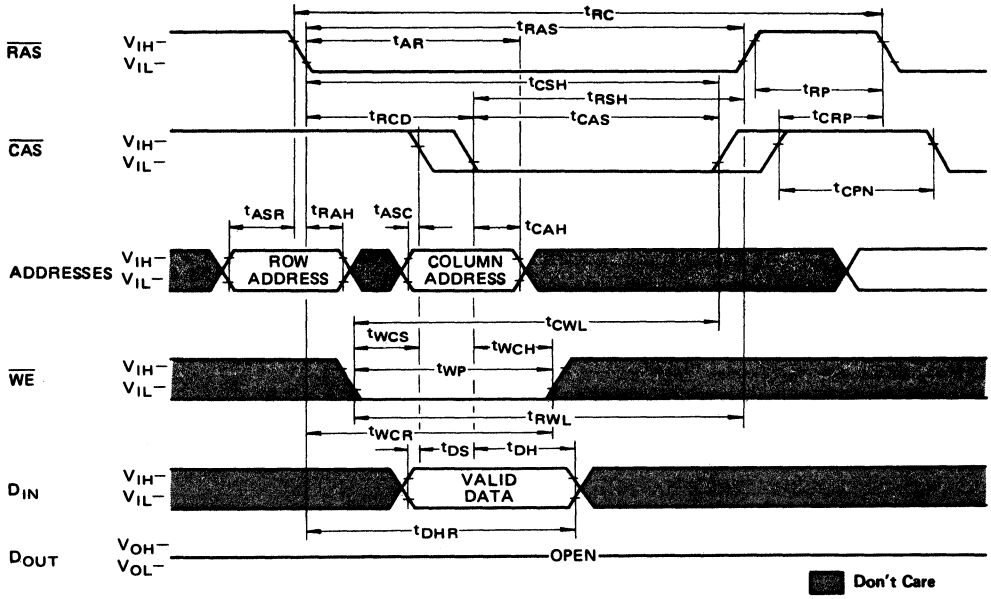
   If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

TIMING DIAGRAMS

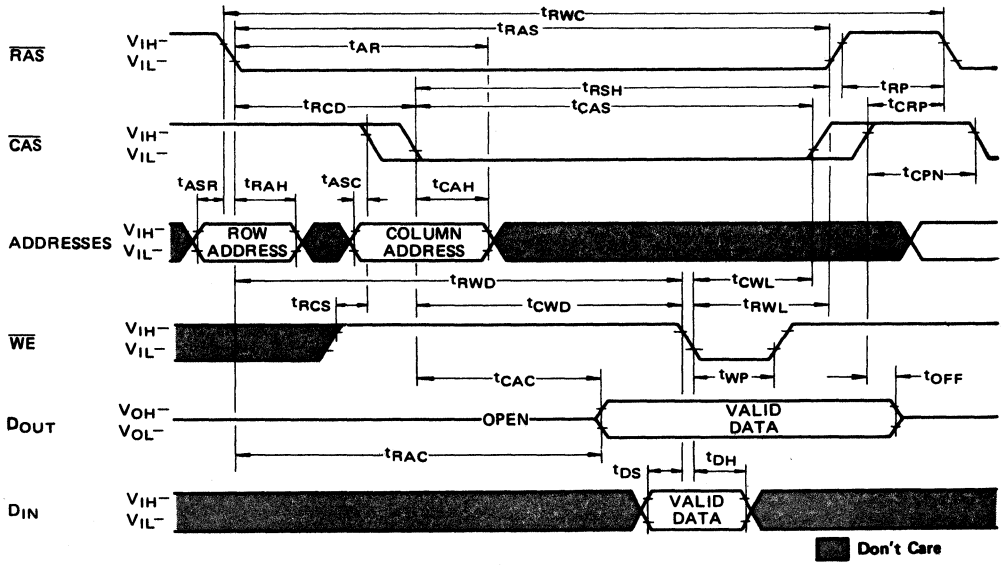
READ CYCLE



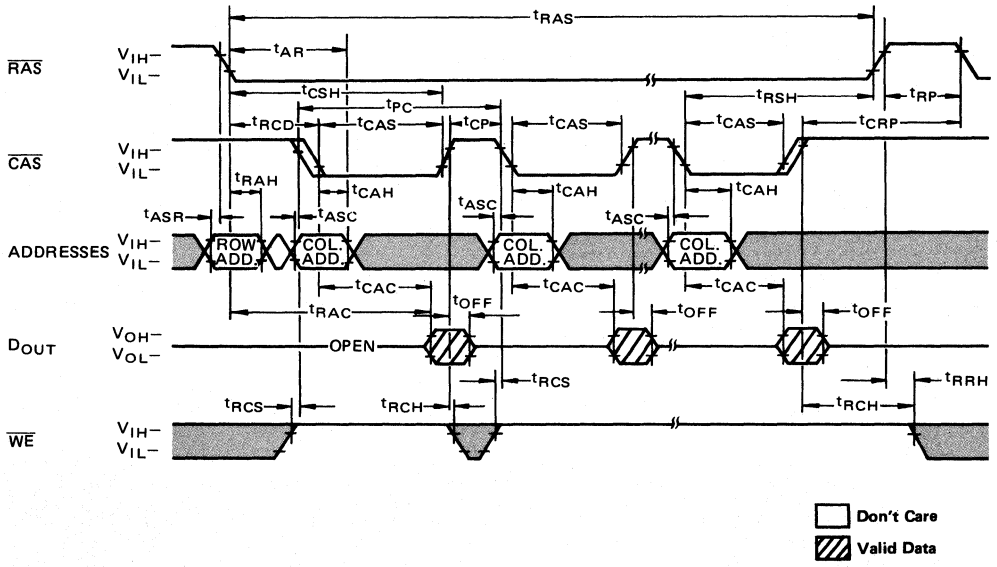
WRITE CYCLE (EARLY WRITE)



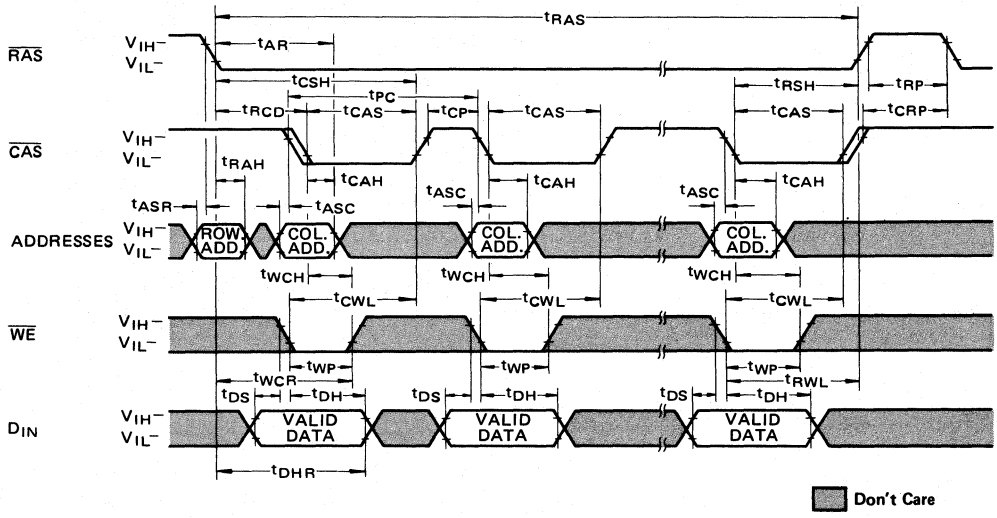
READ-WRITE/READ-MODIFY-WRITE CYCLE



PAGE-MODE READ CYCLE

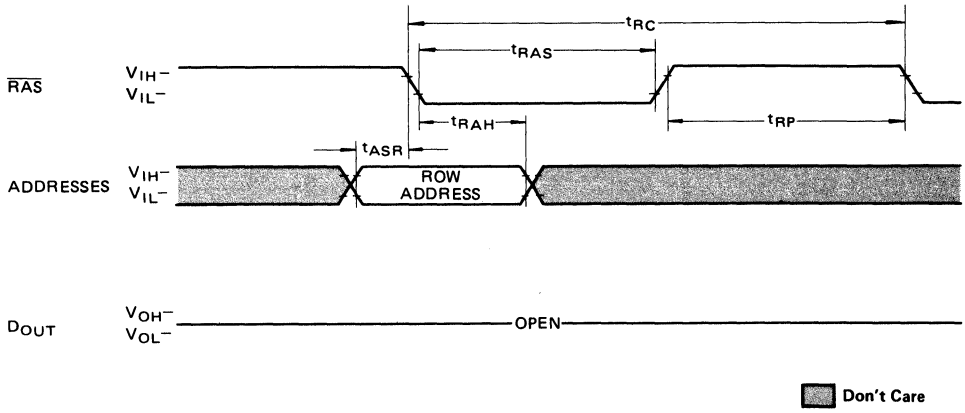


PAGE-MODE WRITE CYCLE

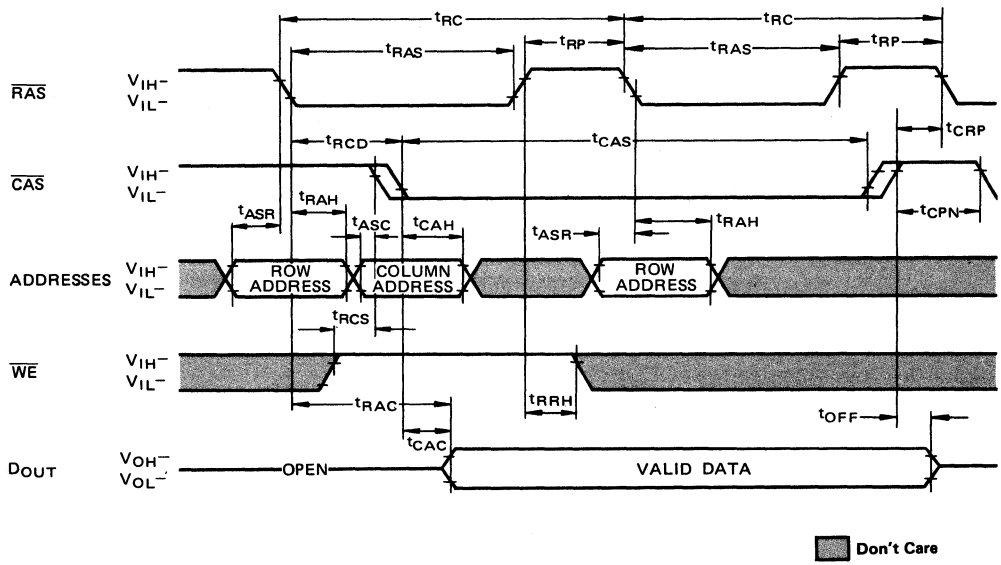


"$\overline{RAS}$-ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't care



HIDDEN "$\overline{RAS}$-ONLY" REFRESH CYCLE



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB8264. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). Then eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8264 during a write or read-write cycle. The last falling-edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits strobing the row-address into the MB8264 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

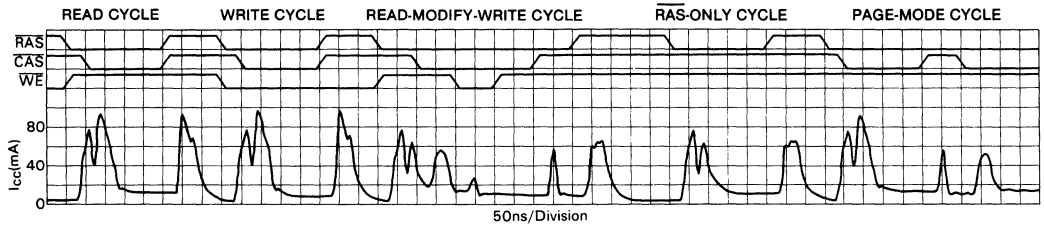
Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh

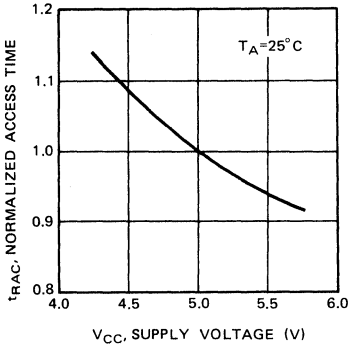
$\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

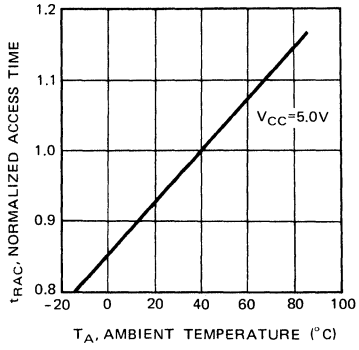


TYPICAL CHARACTERISTICS CURVES

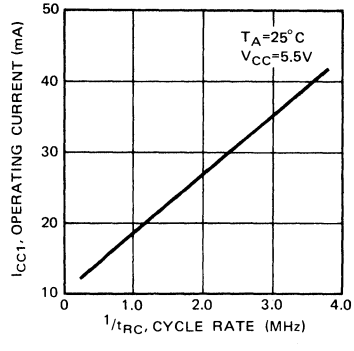
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



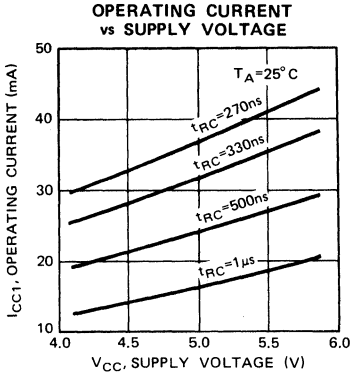
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



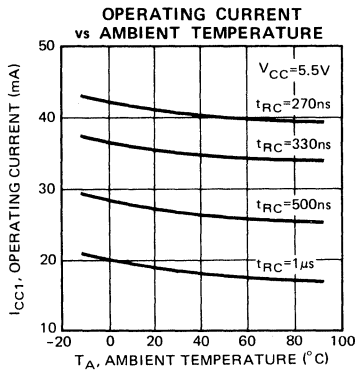
OPERATING CURRENT vs CYCLE RATE



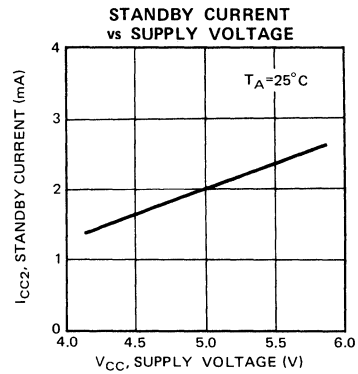
OPERATING CURRENT vs SUPPLY VOLTAGE



OPERATING CURRENT vs AMBIENT TEMPERATURE

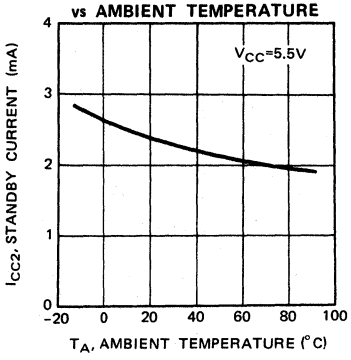


STANDBY CURRENT vs SUPPLY VOLTAGE

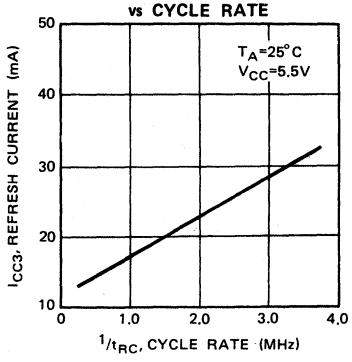


TYPICAL CHARACTERISTICS CURVES (Continued)

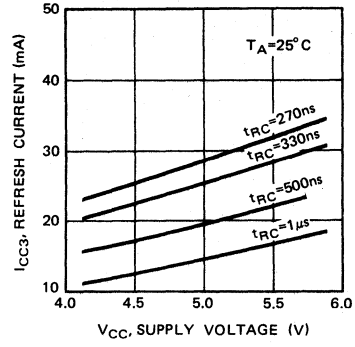
STANDBY CURRENT vs AMBIENT TEMPERATURE



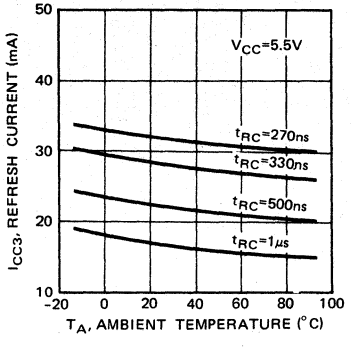
REFRESH CURRENT vs CYCLE RATE



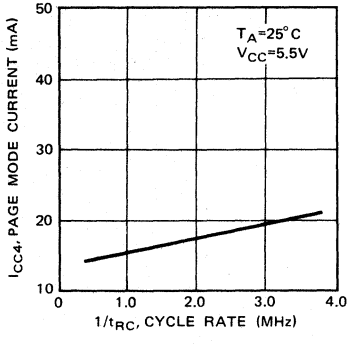
REFRESH CURRENT vs SUPPLY VOLTAGE



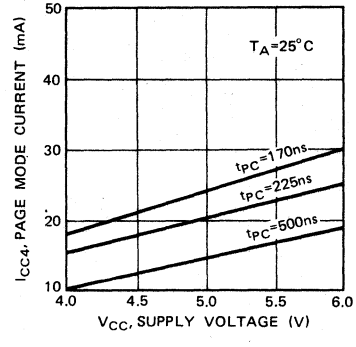
REFRESH CURRENT vs AMBIENT TEMPERATURE



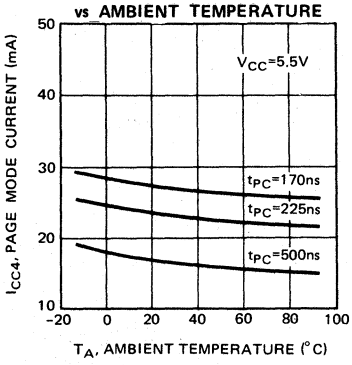
PAGE MODE CURRENT vs CYCLE RATE



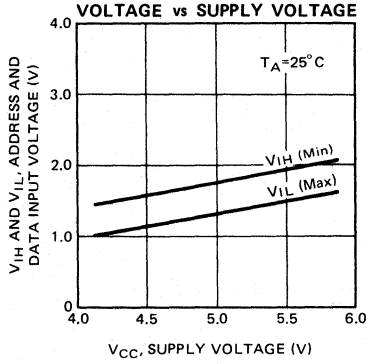
PAGE MODE CURRENT vs SUPPLY VOLTAGE



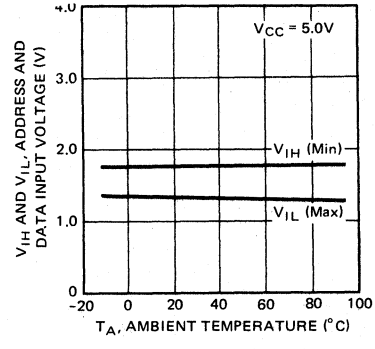
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

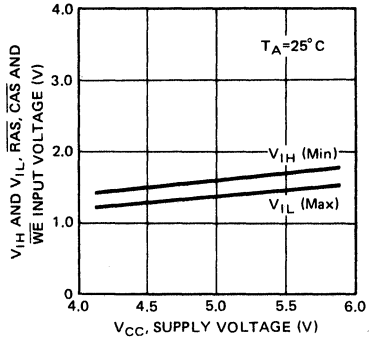


ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

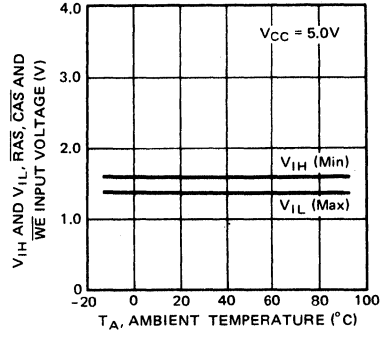


TYPICAL CHARACTERISTICS CURVES (Continued)

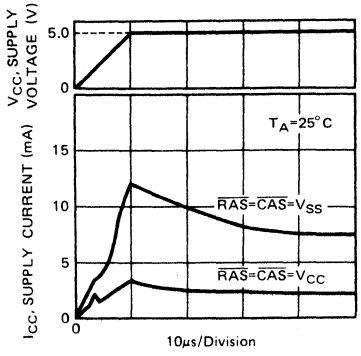
RAS, CAS AND WE INPUT VOLTAGE vs SUPPLY VOLTAGE

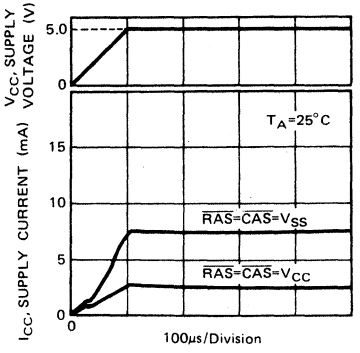


RAS, CAS AND WE INPUT VOLTAGE vs AMBIENT TEMPERATURE

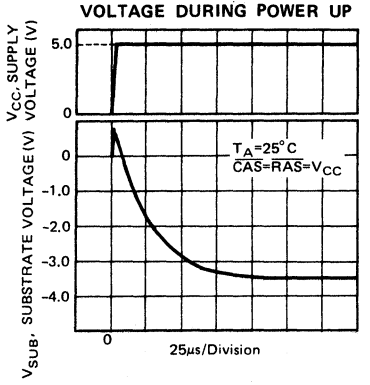


TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP





SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE DURING POWER UP



SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP (ON MEMORY BOARD)